Editors' Suggestion

Conditional Dispersive Readout of a CMOS Single-Electron Memory Cell

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Quantum computers require interfaces with classical electronics for efficient qubit control, measurement, and fast data processing. Fabricating the qubit and the classical control layer using the same technology is appealing because it will facilitate the integration process, improving feedback speeds and offering potential solutions to wiring and layout challenges. Integrating classical and quantum devices monolithically, using complementary metal-oxide-semiconductor (CMOS) processes, enables the processor to profit from the most mature industrial technology for the fabrication of large-scale circuits. We demonstrate a CMOS single-electron memory cell composed of a single quantum dot and a transistor that locks charge on the quantum-dot gate. The single-electron memory cell is conditionally read out by gate-based dispersive sensing using a lumped-element LC resonator. The control field-effect transistor (FET) and quantum dot are fabricated on the same chip using fully depleted silicon-on-insulator technology. We obtain a charge sensitivity of $\delta q = 95 \times 10^{-6} e\,\mathrm{Hz}^{-1/2}$ when the quantum-dot readout is enabled by the control FET, comparable to results without the control FET. Additionally, we observe a single-electron retention time on the order of a second when storing a single-electron charge on the quantum dot at millikelvin temperatures. These results demonstrate first steps towards time-based multiplexing of gate-based dispersive readout in CMOS quantum devices opening the path for the development of an all-silicon quantum-classical processor.

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I. INTRODUCTION

Multiple quantum computing platforms have already reached the level of few-qubit demonstrators [1,2] and are addressing the challenges of scaling up to larger arrays in order to implement error-correction protocols [3–5] and tackle practical problems. Besides the challenge of scaling up quantum devices reliably, a key area is the development of the interface between isolated quantum devices and the classical control and readout technology (which may include optics, microwaves, or dc electronics, depending on the technology platform) to perform control and readout of the quantum state of the system [6]. This quantum-classical interface ranges from low-level operations for implementing feedback and error correction up to high-level operations to run the quantum algorithm.

Amongst the most promising candidates for large-scale quantum computing are electron spins in semiconductor devices, particularly in isotopically purified silicon [7–10]. Silicon is attractive as a host material, as it offers long coherence times [9,11,12] and a variety of qubit implementations and coupling geometries [9–11,13–22]. Silicon-based qubit implementations have advanced to a level which could allow fabricating of complex quantum circuits. These advances are reflected by the amount of recent architectural proposals addressing the challenges towards a fault-tolerant, large-scale, spin-based quantum computer, which include the development of a quantum-classical interface [23–29]. Silicon-based approaches can all, to varying degrees, leverage nanofabrication techniques used in the semiconductor industry, and they can make use of CMOS technology as the basic platform for qubit devices [13,16]. The small footprint of the qubit nanostructures themselves would allow for high-density integration of the qubits [14]; however, exploiting this potential to scale up to a large number of densely packed qubits brings formidable challenges in qubit addressing.

CMOS technologies provide a natural route towards tackling challenges in qubit addressing and the integration of control and readout electronics for large-scale quantum processors [30]. A recent proposal by Veldhorst *et al.* considers on-chip integration of quantum and classical hardware, with a CMOS-based quantum processor relying on quantum-dot spin qubits and transistor-based control circuits combined with charge storage and a scalable

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gate-based readout scheme [24]. The architecture has similarities with the floating memory gates found in modern dynamic random-access memory (DRAM) chips [31]. In both cases, a key concept which underpins scalability is multiplexing: the ability to address arrays of 2^n (qu)bits using $O(n)$ leads. If, ultimately, 10^8 qubits will be necessary to solve practical problems in a fault-tolerant quantum computation protocol [32], then multiplexing would alleviate the prohibitively large number of lines needed to address each qubit independently.

On-chip multiplexing circuitry to address elements of an array of gate-defined quantum devices has been demonstrated in GaAs [33,34] [256 quantum point contacts (QPCs)] and Si/SiGe [35] (four quantum-dot devices). Similarly, a switching matrix for a high-frequency transmission line has been realized [29] showing routes towards controlling large-scale devices. In addition to device control, high-fidelity readout is an essential requirement, and for quantum-dot devices readout is commonly achieved by using nearby electrometers [36–38]. Gate-based readout [39–41] provides a more scalable alternative, taking the gate(s) that define the quantum dot and using them additionally as a sensor. For both separate and gate-based qubit readout, sensitivity and speed are improved by using radio-frequency (rf) techniques: coupling the sensor to a rf lumped-element resonant circuit. Recently, gate-based approaches have reached a sensitivity of $37 \times 10^{-6} e\,\mathrm{Hz}^{-1/2}$ [42], comparable to rf electrometers [37,43,44].

Frequency-domain multiplexing using multiple lumped-element circuits is a useful method to read out multiple sensors simultaneously; however, the scalability of this approach is limited by the accessible bandwidth of such circuits [45]. Time-based multiplexing allows for the subsequent readout of multiple gate-based sensors limited by the retention (refresh) time of individual cells and requires only a single resonant circuit tackling challenges towards readout of dense quantum-dot arrays.

In the context of circuit quantum electrodynamics transmission-line resonators are used to achieve strong coupling between photons and a superconducting artificial atom [46]. Recently, these approaches have been adapted to silicon-based quantum-dot devices achieving strong coupling [15,47–49] and dispersive readout [50] (with an increased accessible bandwidth due to operation at a few gigahertz), representing an alternative to rf electrometers and gate-based readout using lumped-element circuits.

II. EXPERIMENTAL SETUP

As envisioned by Veldhorst *et al.* [24], both the quantum-dot device and the control field-effect transistor (FET) are fabricated using the same CMOS process and realized on the same chip (see Appendix A for details). The role of the FET is to retain a voltage at the quantum-dot gate in the *off* state (charge storage) in order to keep the number of electrons in the dot constant. Moreover it allows selective rf readout of the dot's charge state; i.e., gate sensing can be performed only when the FET is in the *on* state. The configuration presented here resembles that of a single DRAM cell in which the role of the charge-storage capacitor is now played by the quantum device, realized in a nanowire transistor (60-nm-wide channel, 30-nm gate), while the "access FET" in DRAM has the role realized by a micronwide channel transistor ("control FET") and the readout electronics is represented by the *LC* resonator. The measurement setup (see Appendix B for details) is depicted in Fig. 1(a), including SEM micrographs of both devices. The connection between the devices is made on chip using a short bond wire. Our experiment realizes a first step towards an integrated time-based multiplexing of gate-based reflectometry readout by demonstrating sensitive readout through the control FET in the *on* state combined

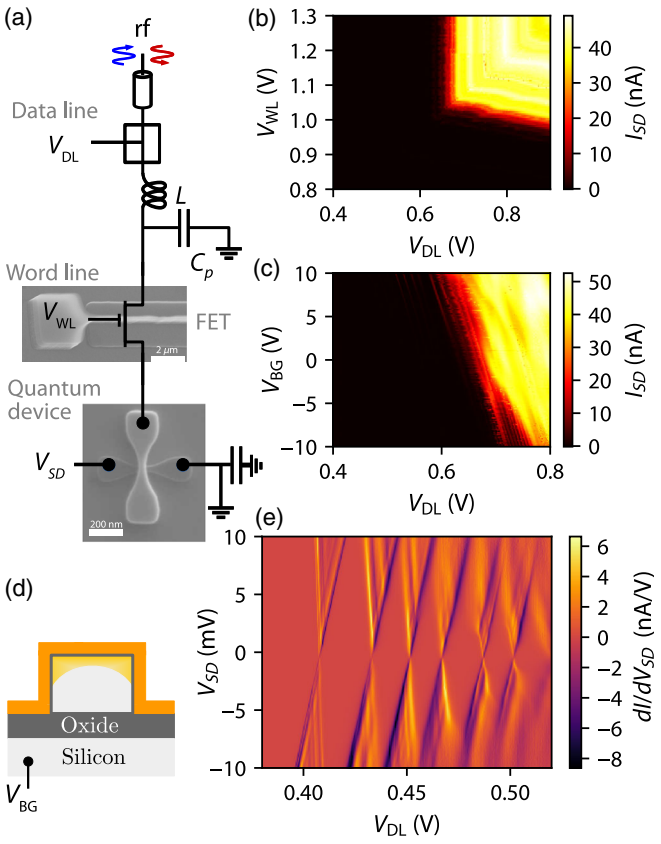

FIG. 1. Experimental setup and dc transport measurements: (a) Measurement circuit schematic, including SEM micrographs of the control FET and quantum device. Control and measurement signals are sent to the quantum device via the channel of a control FET. (b) Transport through the quantum device as a function of V_{DL} and V_{WL} yielding the threshold voltage of the control FET and quantum device at $V_{\mathrm{BG}} = 0$ V. (c) Turn-on characteristic of the quantum device as a function of V_{BG} when the FET is biased well above threshold at $V_{\mathrm{WL}} = 1.3$ V. (d) Cross-section illustration of the nanowire-based quantum device under high back-gate bias and near-threshold top-gate bias, such that a single quantum dot forms. (e) Coulomb diamonds indicating a single quantum dot in the quantum device at $V_{\mathrm{BG}} = 10$ V.

with floating-gate charge storage in the *off* state. Multiplexing can then be achieved by connecting additional cells consisting of a single switching FET and a quantum device (as the one demonstrated here) to the same high-frequency line sharing one single resonant and bias circuit.

In the nanowire transistor, we expect formation of quantum dots in the upper corners at cryogenic temperature due to an enhanced field effect under the gate [51]. At large positive back-gate voltage, the wave function of electrons in the corners is expected to extend farther into the center of the wire, resulting in a single extended quantum dot [see Fig. 1(d)] [52].

The combined quantum-classical CMOS circuit presented here has two primary inputs which, in analogy to a multiplexer or memory device, we refer to as the word and data (bit) line. The word line is connected to the gate of the control FET, while the data-line signal passes through the channel of the control FET and is applied to the gate of the quantum device. Source-drain transport through the quantum device can be measured directly and readout based on rf reflectometry can be performed (when the control FET gate voltage V_{WL} is above threshold) by applying rf modulation via the data line [using an on–printed circuit board (PCB) bias tee] to an LC resonant circuit made from a surface mount inductor and the parasitic capacitance of the device C_p. The LC resonator response is amplified at multiple stages, followed by in-phase and quadrature demodulation (see Appendix B and Ref. [41] for details), from which the amplitude and phase of the reflected signal are obtained. The phase Φ of the reflected signal is sensitive to small changes ΔC in the capacitance of the quantum device, associated, for example, with the tunneling of single electrons: $\Delta\Phi \approx 2Q\Delta C/C_T$ [53], with Q being the quality factor of the resonator and C_T being the total capacitance of the circuit, which includes the parasitic capacitance in parallel with the device capacitance.

III. dc CHARACTERIZATION

First, we characterize the quantum device and the control FET through transport measurements. We measure the source-drain current through the quantum device as a function of V_{DL} and V_{WL}, at a source-drain bias of $V_{SD} = 1$ mV, observing the turn-on of the FET and quantum device in Fig. 1(b). When the control FET is operated below threshold (the *off* state), the gate of the quantum device is isolated from the signal on the data line. In this state of the circuit, the quantum device gate floats, allowing it to retain its charge over a timescale of a second, as we explore later on. For measurements where V_{WL} is ramped slowly [as in Fig. 1(b)], the quantum device gate voltage tends to 0 V when the control FET is *off*. Once the control FET is operated well above threshold, the transfer curve of the quantum device transistor can be measured, while a transition region is also apparent where the control FET is still strongly resistive. From Fig. 1(b), we estimate the threshold voltage of the quantum device $V_{\mathrm{th}}^{Q} = 0.63$ V and the FET $V_{\mathrm{th}}^{\mathrm{FET}} = 0.37$ V (at $V_{\mathrm{BG}} = 0$ V). The control FET threshold voltage is calculated as $V_{\mathrm{th}}^{\mathrm{FET}} = V_{\mathrm{WL}} - V_{\mathrm{DL}}$ at $(V_{\mathrm{WL}}, V_{\mathrm{DL}}) = (1.02, 0.65)$ V and additionally depends on V_{BG} (not shown).

An additional tuning parameter for the quantum device used here is the back-gate voltage V_{BG} applied to the substrate, which affects both the control FET and quantum device, as they are realized on the same chip.

In Fig. 1(c), we show the quantum-dot source-drain current as a function of V_{DL} and V_{BG} with the control FET biased at $V_{\mathrm{WL}} = 1.3$ V. While the quantum-dot device shows no transport at small V_{DL}, we see a turn-on at high V_{DL}. We observe that the turn-on threshold reduces as V_{BG} is increased. Close to threshold, we observe Coulomb oscillations which look very regular at large V_{BG}. Additionally, we note that the circuit RC time remains shorter than the acquisition time (20 ms) for all shown back-gate voltages.

Finally, in Fig. 1(e), we confirm the formation of a single few-electron quantum dot under the gate of the quantum device by measuring Coulomb diamonds at $V_{\mathrm{BG}} = 10$ V and $V_{\mathrm{WL}} = 1.3$ V. We observe a first addition energy of about 16 meV, showing strong confinement compatible with previous measurements [13,51].

IV. rf CHARACTERIZATION

We now move on to performing a gate-based rf readout of the quantum dot and evaluating the achievable charge sensitivity, considering the potential impact of the additional parasitic capacitance and dissipation from the control FET circuit.

A. rf readout

First, we characterize the LC resonant circuit by measuring reflection (S_{11}) as a function of V_{WL} [see Fig. 2(a)]. We observe a lowering of the resonance frequency when the control FET is operated above threshold ($V_{\mathrm{WL}} > 0.63$ V) due to the additional capacitance of the FET circuit that appears in parallel to C_p. Figure 2(b) shows the total capacitance C_T (assuming the nominal inductance $L = 390$ nH) and quality factor Q of the LC circuit obtained from Fig. 2(a). We estimate the contribution of the FET circuit at 105 fF. Additionally, we observe a reduction of Q when the FET is in the *on* state. The quality factor and capacitance play an important role in the phase response ($\Delta\Phi \approx 2Q\Delta C/C_T$) [53] and sensitivity of gate-based dispersive readout, which is addressed later in this article.

Next, we examine the phase response of the resonant circuit as a function of the gate voltage on the control FET [see Fig. 2(c)], using rf modulation at frequency $f_{\mathrm{rf}} = 313$ MHz and power $P_{\mathrm{rf}} = -88$ dBm. Starting with the control FET well above threshold ($V_{\mathrm{WL}} = 1.3$ V), in the strong accumulation regime, we observe three principal

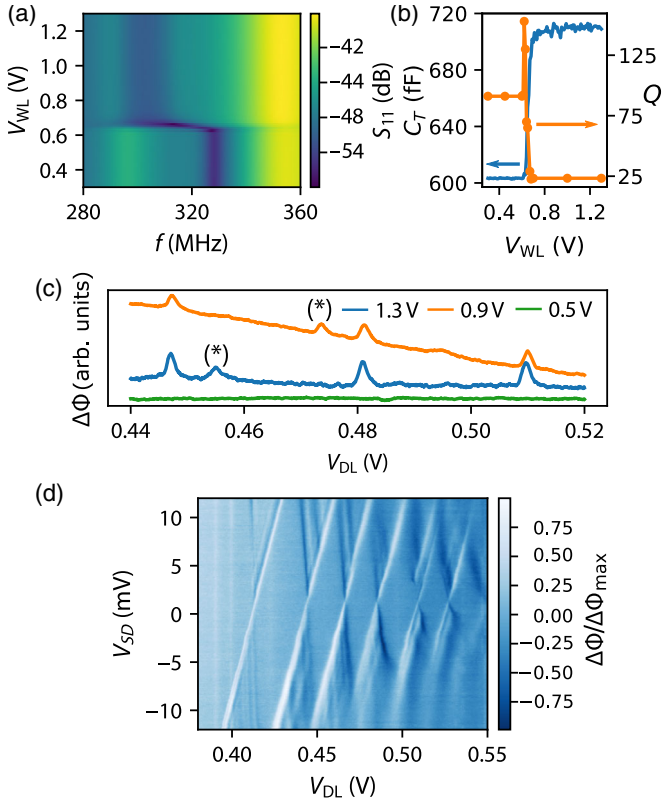

FIG. 2. rf characterization and charge sensitivity: (a) S_{11} of the rf circuit as a function of V_{WL} (with $V_{DL} = 0.4$ V and $V_{BG} = 10$ V). (b) Total resonator capacitance C_T (with $L = 390$ nH) and quality factor Q as a function of V_{WL}. (c) Change in phase response for different V_{WL} values showing three Coulomb oscillations only when the control FET is operated above threshold. Features originating from charge transitions within the control FET itself are indicated (as asterisk). (d) Coulomb diamonds measured in the phase response ($V_{BG} = 10$ V and $V_{WL} = 1.3$ V), which is normalized with respect to the maximal change.

Coulomb peaks when ramping V_{DL} [the blue trace in Fig. 2(c)]. The peaks remain initially visible as V_{WL} is reduced, though a background signal begins to dominate as the control FET enters the weak-inversion regime, where the FET gate capacitance strongly depends on $V_{WL} - V_{DL}$. Since V_{DL} is modulated by the rf signal, this dependency is picked up in the dispersive response of the resonator as an additional change in capacitance and, in turn, produces an additional phase shift that depends on V_{DL}. Eventually, when $V_{WL} < 0.5$ V, the control FET is below threshold and the dispersive response vanishes [the green trace in Fig. 2(c)]. We note the appearance of additional features in the scan (indicated by asterisks), which we identify with single-electron tunneling events in the control FET due to their V_{WL} dependence. These features become more apparent when operating the control FET close to threshold. Figure 2(d) shows rf measurements (with the control FET well above threshold) demonstrating Coulomb diamonds of the quantum dot in the same voltage region as the transport measurements in Fig. 1(e). The correspondence between both sets of measurements shows that, in the strong accumulation regime, the FET channel has a negligible impact on the rf readout.

B. Charge sensitivity

To measure the charge sensitivity of the gate-based sensor with a control FET, we apply a small-amplitude signal of frequency $f_s = 303$ Hz (in addition to the rf modulation at f_{rf}) onto the data line and monitor the signal-to-noise ratio (SNR) in decibels of the sidebands appearing in the frequency spectrum at $f_{rf} \pm f_s$. The peak amplitude of the signal (0.2 mV) corresponds to a change of $\Delta q_{rms} = 0.005\,78e$ in the charge on the quantum dot, where e is the charge of the electron. A typical spectrum in shown is Fig. 3(a). We optimize the sideband SNR by tuning the circuit parameters V_{DL}, f_{rf}, and P_{rf} as seen in Figs. 3(b)–3(d), respectively. First, we find the maximum sensitivity at the point of maximum slope in the response of the resonator, $V_{DL} = 0.525$ V. The rf dependence, in Fig. 3(c), reveals a maximum at $f_{rf} = 313$ MHz and a 3-dB measurement bandwidth of 13 MHz, which translates into a loaded Q of 24 in the *on* state of the control FET, which is compatible with estimations obtained from Fig. 2(a). The optimal value for the rf power P_{rf} is found

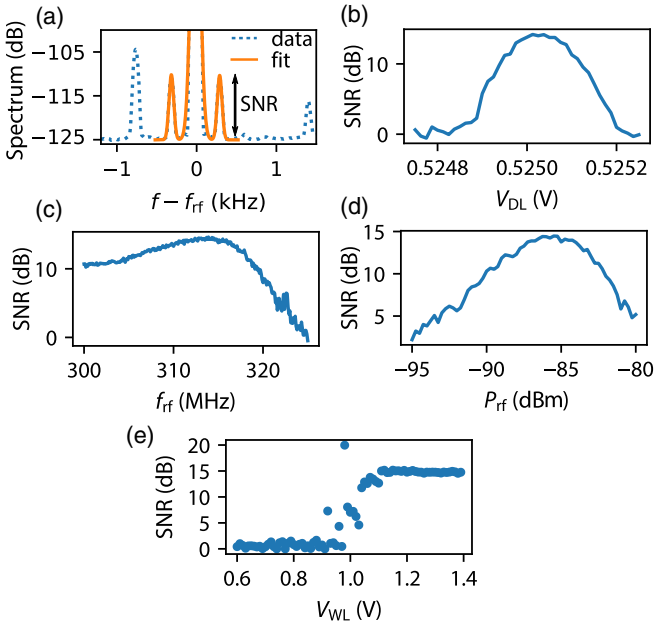

FIG. 3. Charge sensitivity of the gated rf readout: (a) Sidebands in the spectrum when operating at the point of maximum slope of a Coulomb oscillation with an equivalent excitation of $0.005\,78e$ at 303 Hz superimposed on the data line. Signal-to-noise ratio (SNR) as a function of (b) data-line dc voltage V_{DL}, (c) carrier frequency f_{rf}, (d) carrier power P_{rf}, and (e) FET gate voltage V_{WL}. When not being swept, the following parameter values are used: $V_{WL} = 1.3$ V, $V_{DL} = 0.525$ V, $f_{rf} = 312$ MHz, $P_{rf} = -85$ dBm.

to be −86 dBm. Finally, observing the SNR as a function of V_{WL} [Fig. 3(e)], we identify two plateaus corresponding to the *on* and *off* states of the control FET. In the approximately linear transition between the plateaus, we observe multiple scattered data points, which we attribute to transitions in the weak-inversion regime of the FET [see the starred features in Fig. 2(c)]. Overall, using optimized circuit parameters, we obtain a SNR of 15.6 dB, which translates into a charge sensitivity of $\delta q = \Delta q_{\mathrm{rms}}/(\sqrt{2B_{\mathrm{SA}}} \times 10^{\mathrm{SNR}/20}) = 95 \times 10^{-6} e\,\mathrm{Hz}^{-1/2}$ for the chosen spectrum analyzer bandwidth $B_{\mathrm{SA}} = 50$ Hz. We study the impact of the control FET resistance (R_{FET}) on sensitivity in Appendix D.

In this experiment, the bandwidth of the charge sensitivity measurements is limited to 500 Hz due to low-pass filtering of the line used to deliver the sinusoidal signal f_s. However, the bandwidth of gate-based reflectometry is limited by the LC resonator bandwidth, which is about 10 MHz when the resonator is coupled to the quantum device.

The charge sensitivity obtained in this experiment is lower than typical rf-QPC devices [44] and demonstrates more than a factor of 50 improvement compared to GaAs-based gate sensors [39], and it is only a factor of 2.5 higher than previously reported in a similar device without a transistor circuit [42].

V. CHARGE STORAGE

For multiplexing of the quantum device gate signal to be effective, the gate must be able to store the charge for a time which is long compared to the inverse of the refresh rate. To measure the electron retention time in our circuit, we study the dynamics of the quantum device when switching the control FET on and off. Measurements are performed in a different pair of devices, with nominally identical dimensions to those used above. In Fig. 4(a), we present the equivalent circuit of the charge memory node, similar to a voltage divider for the data-line voltage V_{DL} with the variable channel resistance of the FET, R_F, and gate leakage resistance, R_G, which represents dielectric losses through the gate oxide. Both resistances determine the voltage $V_G = [R_G/(R_F + R_G)]V_{\mathrm{DL}}$ appearing on the gate of the quantum device; the capacitance of this gate, represented by C_G, can be obtained from the gate-voltage spacing ΔV_{DL} between consecutive Coulomb blockade oscillations plotted in Fig. 4(d). Using $C_G^{n,n+1} = e/\Delta V_{\mathrm{DL}}^{n,n+1}$, where n is the number of electrons in the dot with respect to an unknown offset N, we obtain $C_G^{0,1} = 6.2$ aF and $C_G^{1,2} = 7.0$ aF. In Fig. 4(b), we show the voltage division V_G/V_{DL} obtained by tracking the position of the Coulomb peak as a function of $(V_{\mathrm{WL}} - V_{\mathrm{DL}})$. We conclude that, at $V_{\mathrm{WL}} < 0.5$ V, the resistance of the control FET channel becomes greater than the gate leakage in the quantum device.

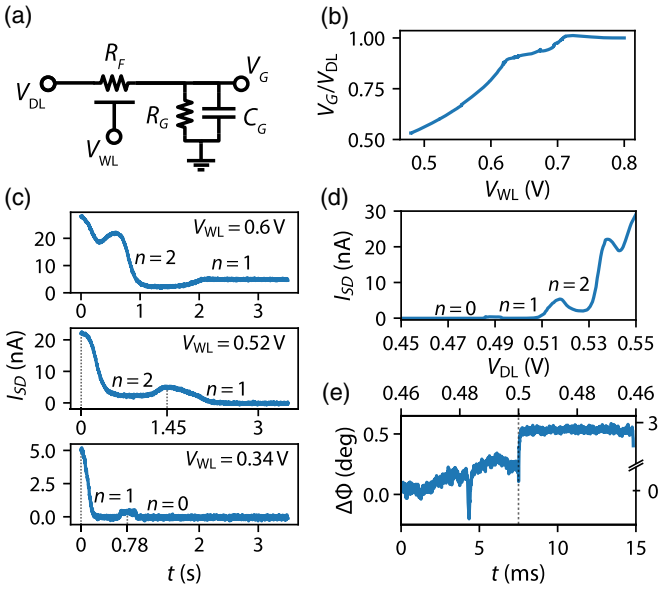

FIG. 4. Charge retention time and fast switching: (a) Equivalent circuit consisting of the variable control FET resistance R_F and quantum device gate leakage R_G and capacitance C_G. (b) Voltage divider characteristic of this circuit. (c) Demonstration of charge locking for different FET *off* states. Slow leakage of quantum-dot gate charge is observed. (d) Quantum device transfer characteristic. (e) Demonstration of rf sensing combined with fast switching of the control FET. Initially, the FET is biased above threshold and V_{DL} is ramped from 0.46 to 0.50 V. Tunneling of the first electron onto the quantum dot is observed (left axis). After 7.5 ms, the FET is biased below threshold, leading to a large jump in phase due to the change in resonance frequency (right axis), while V_{DL} is ramped back down. In the *off* state, no electron tunneling is observed.

The charging dynamics of the device is determined by the circuit RC time constant $\tau = [(C_G R_G R_F)/(R_G + R_F)]$. By switching the control FET from an *on* state to different *off* states and monitoring the resulting source-drain current through the quantum device, we study the dynamics of our circuit [see Fig. 4(c)]. In each case, V_{DL} is kept constant at 0.6 V. By comparing the transient response with the quantum device transfer characteristic [Fig. 4(d)], we see that $I_{SD}(t)$ reproduces the Coulomb oscillations, with the steady-state current determined by the voltage divider and V_{DL}. For $V_{\mathrm{WL}} = 0.6$ V as the *off* state, $R_F < R_G$, the discharging of the gate capacitor, occurs mainly through the control FET channel. For a more resistive *off* state of the control FET, as given by $V_{\mathrm{WL}} = 0.34$ V, discharging of the gate capacitor occurs mainly through gate leakage since $R_F > R_G$ and the steady-state voltage on the quantum device gate V_G approaches zero.

Using the observed time dynamics of the current in Fig. 4(c), we characterize the single-electron retention time of the storage node through time lapses $\Delta t^{n,n+1}$ between successive Coulomb oscillations, obtaining $\Delta t^{1,2} = 1450$ ms and $\Delta t^{0,1} = 780$ ms. These retention times can

be used to estimate the following circuit parameters: $R_F(V_{WL}=0.52\,V)=3.1\times10^{18}\,\Omega$, $R_F(V_{WL}=0.34\,V)=4.7\times10^{18}\,\Omega$, and $R_G=3.5\times10^{18}\,\Omega$. For the RC time constant, we find $\tau^{1,2}$, $\tau^{0,1}\approx12$ s. These results provide valuable information to assess the suitability of time-multiplexing dispersive readout for large-scale quantum computing. First of all, these values compare quite favorably to state-of-the-art DRAM cells, which show a leakage resistance on the order of $10^{15}\,\Omega$ [54] and a refresh time of 64 ms [55]. Moreover, the retention times reported here are well above the typical expected readout times of 100 ns of gate-based reflectometry [42] and the single-qubit coherence time of 28 ms in ^{28}Si substrates [9]. Considering typical operation times of spin qubits in silicon (1 μs), this retention time will allow the addressing of 10^6 qubits before the voltage on one node needs to be refreshed.

As a demonstration towards time-multiplexed dispersive readout, we perform a rf reflectometry measurement followed by fast switching of the control FET [shown in Fig. 4(d)]. In the first part of the measurement cycle, V_{DL} is ramped from 0.46 to 0.50 V while the control FET gate is *on* ($V_{WL}=1.2$ V), leading to a tunneling of the first electron onto the quantum dot. Then, after 7.5 ms, the control FET is switched to the *off* state ($V_{WL}=0.3$ V) and V_{DL} is ramped down to 0.46 V. As expected, no dispersive response from the quantum dot is measured during this time period, which can instead be used to measure another quantum device connected to the same data line via a different control FET. In this way, multiple qubits can be measured sequentially within the retention time of the charge-storage circuit. Considerations on the heat dissipation of this sequential approach are discussed in Appendix A.

VI. CONCLUSION

In conclusion, we demonstrate in this paper the integration of three elements likely to play key roles in a large-scale spin-based quantum computer: a quantum device (quantum dot), a classical control device (field-effect transistor), and sensitive charge readout (electrical resonator). Two of these are fabricated on the same chip using CMOS technology, and there is the potential for the LC resonator to be made in a CMOS process [45,56]. High quality factors can be achieved by using superconducting TiN, which is already found in the gate stack of current CMOS transistors. Overall, we demonstrate a first step towards time-based multiplexing of gate-based radio-frequency reflectometry by demonstrating controlled rf readout of a single quantum dot with a charge sensitivity of $\delta q=95\times10^{-6}e\,\mathrm{Hz}^{-1/2}$, combined with single-electron charge storage on the order of 1 s, providing motivation for further experiments on multiqubit circuits.

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APPENDIX A: FABRICATION DETAILS

The CMOS transistors used in this work are fabricated on SOI substrates with a 145-nm buried oxide. The silicon layer is patterned to create the nanowires by means of optical lithography, followed by a resist trimming process. The gate stack consists of 1.9-nm HfSiON capped by 5 nm TiN and 50 nm polycrystalline silicon leading to a total equivalent oxide thickness of 1.3 nm. The Si thickness under the HfSiON/TiN gate is 11 nm. After gate etching, a SiN layer (10 nm) is deposited and etched to form a first spacer on the sidewalls of the gate. 18-nm-thick Si raised source and drain contacts are selectively grown before the source-drain extension implantation and activation annealing. A second spacer is formed followed by source-drain implantations, activation spike anneal, and salicidation [(Ni,Pt)Si].

APPENDIX B: MEASUREMENT SETUP

Measurements are performed at the base temperature of a dilution refrigerator (40 mK). Low-frequency signals (V_{SD}, V_{DL}, V_{WL}) are delivered through filtered cryogenic loom, while a radio-frequency signal for gate-based readout is delivered through an attenuated and filtered coaxial line which connects to a on-PCB bias tee combining the rf modulation with V_{DL}. The resonator is formed from a 390-nH inductor and the sample's parasitic capacitance to ground in parallel with the device. The inductor consists of a surface mount wire-wound ceramic core (EPCOS B82498B series), and the PCB is made from 0.8-mm-thick Rogers RO4003C laminate with an immersion silver finish. The reflected rf signal is amplified at 4 K (QuinStar QCA-U350-30H) and room temperature, followed by quadrature demodulation (Polyphase Microwave AD0105B), from which the amplitude and phase of the reflected signal are obtained.

APPENDIX C: HEAT DISSIPATION

Although integration of quantum and classical CMOS devices promises major advantages in practical quantum computing architectures—for example, in addressing wiring challenges—this integration comes at a cost of managing the dissipation of heat from the classical control

circuits. We estimate the heat dissipation per device in our experiments, based on the dynamic power produced by the control FET, which is given by $P = C_{\mathrm{FET}} f_{\mathrm{op}} \Delta V^2$. We estimate C_{FET}, the FET capacitance, to be $C_{\mathrm{FET}} = 13$ fF, given the FET dimensions (50 nm × 10 μm gate and 1.3 nm equivalent oxide thickness). The operation frequency f_{op} is limited by readout time, typically $t = 1$ μs for rf sensors, which determines the maximal frequency of 1 MHz. The largest voltage difference between the *on* and *off* states of the FET chosen in this experiment comes close to $\Delta V = 1$ V. From this voltage change, we estimate a power dissipation of $P = 13$ nW per device, which can be treated as an upper bound as the dimensions, and thus the capacitance of the FET, the operation frequency, and the voltage difference ΔV can all be reduced. Nevertheless, assuming a cooling power of 400 μW at 100 mK, as is achieved in current dilution refrigerators, operation of at least 30 000 transistors would be possible at this temperature.

APPENDIX D: IMPACT OF CONTROL FET RESISTANCE

In this appendix, we calculate the impact of the control FET resistance on the gate-sensor sensitivity. We consider the circuit in Fig. 5(a). It schematically represents a single-electron memory cell embedded in an LC resonator. Here, L represents a surface mount inductor, and C_p is the parasitic capacitance to ground of the cell. R_{FET} represents the source-drain resistance of the control FET. The parallel RC circuit after the FET represents the high-frequency equivalent circuit of the quantum-dot device, as seen from the gate electrode. The circuit consists of a constant geometric capacitor C_G combined with a variable capacitance C_t representing gate-voltage-dependent tunneling contributions and a resistor R_G^{rf} that parametrizes high-frequency dielectric losses. The reflection coefficient of this circuit is given by

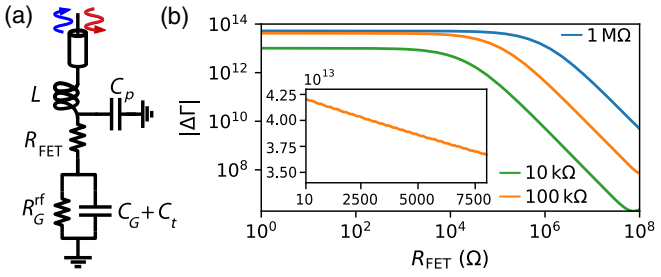

FIG. 5. Impact of FET resistance on the sensitivity to device capacitance changes: (a) Equivalent circuit with the FET resistance R_{FET}, parasitic and FET capacitance C_p, and quantum device with losses R_G^{rf}, capacitance C_G, and variable tunneling capacitance C_t. (b) Reflection coefficient sensitivity to capacitance changes as a function of R_{FET} for different values of R_G^{rf} (logarithmic scale). (Inset) Linear scale of region of low resistance.

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}, \tag{D1}$$

where Z is the impedance of the circuit and Z_0 the coaxial-line impedance of 50 Ω.

Gate-based sensors are sensitive to capacitance changes associated with single-electron tunneling [59]. In our particular case, single-electron tunneling manifests as a variable capacitor C_t. We model the sensor's reflection sensitivity to changes in C_t,

$$|\Delta\Gamma| = \left| \frac{\partial \Gamma}{\partial C_t} \Delta C \right|, \tag{D2}$$

and study the dependence on R_{FET} and R_G^{rf}. We see that $|\Delta\Gamma|$ does not change drastically until the FET resistance becomes comparable to R_G^{rf} (note the logarithmic scale). At large R_{FET}, $|\Delta\Gamma|$ drops rapidly and the gate sensor becomes insensitive to changes in C_t. A small R_{FET} value is desired to maximize the sensitivity, as highlighted in the inset of Fig. 5(b), which shows a linear decrease of sensitivity of the reflection coefficient to capacitive changes (for $R_G^{\mathrm{rf}} = 100$ kΩ). The *on* state dc resistance of the control FET used in this experiment is on the order of 20 kΩ.

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