# Thin Ge buffer layer on Silicon for Integration of III-V on Silicon

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*Abstract* — **Development of Si-based lasers is considered as the key to the realization of fully integrated Si photonic circuits. Monolithic growth of III-V lasers on Si substrates is one of the most promising solutions for developing a commercially viable Si-based laser. However, the performances of current devices are still hindered by defects, hence the optimisation of crystal quality of the laser structures is of paramount importance. This paper reports on growth optimisation of thin Ge buffer layers on Si as an alternative to thick GaAs buffer layers. This method reduces the overall thickness and lowers the threading dislocation density in III-V semiconductors integrated on silicon platform.**

*Keywords—III-V-Silicon integration, Ge buffer layers, Si photonics*

## 1. Introduction

Silicon-based photonic integrated circuits promise low-cost, low-power and high-bandwidth solutions for high-speed interconnects and optical communication systems thanks to the maturity of CMOS processing technology [1, 2]. However, the lack of a reliable silicon based light source prevents full optical integration hence realizing a silicon laser has been considered the "Holy Grail" for silicon photonics [2-5]. Due to its indirect bandgap property, bulk silicon material is very inefficient at emitting light. In contrast, III-V semiconductors with direct bandgaps have superior light emission efficiencies [6-8]. The epitaxial growth of III-Vs on Si substrates has been regarded as one of the best ways of realizing a high-performance light source for Si-based photonic integrated circuits. Such a solution faces several challenges due to large material dissimilarities between the III-V and group-IV semiconductors. The large lattice mismatch, different polarities and thermal expansion coefficients between impede efficient operation of the devices by introducing threading dislocations (TDs), anti-phase boundaries (APBs) and thermal cracks [9-12].

Various techniques, including growing thick III-V buffer layers with dislocation filter layers (DFLs) have been used to improve the material quality of the III-V photonic devices on Si [13-15]. Implementing quantum confined materials, such as quantum wells and quantum dots (QDs) [16-19], has allowed for further improvements in the devices quality and realization of the first functional lasers [20]. Recently, a long lifetime electrically-pumped continuous-wave III-V quantum dot laser monolithically grown on silicon has been successfully demonstrated by Chen *et al* [7]. Such a laser can be successfully integrated with the silicon photonic components to create high-performance wafer-scale fully photonic circuits. The use of thick GaAs buffer layers, however, has several drawbacks. Firstly, the thick III-V layers can lead to crack for releasing the built-up thermal strain. Furthermore, the thick buffer layer increases both the cost and growth time of such devices, as well as introducing difficulties for optical coupling to a waveguide, making integration of III-V lasers on SOI more challenging. In this paper, we propose to replace the thick GaAs buffer layers with

significantly thinner Ge ones. Since Ge (5.658Å) and GaAs (5.653Å) have almost identical lattice constants, no significant strain is introduced when a GaAs-based III-V laser structure is grown on Ge, compared with GaAs directly grown Si substrate [8]. Combing thin Ge buffer layer with superior light emitting properties of III-V QD laser structures could enable next generation of high-performance CMOS-compatible light sources, suitable for photonic integrated circuits.

## 2. Methods and results

Simple two-step Ge buffer layers were grown on N-type (100) silicon substrates using a solid-source molecular beam epitaxy (MBE) system. The crystallographic properties of the grown samples were studied by X-ray diffraction (XRD), electron channeling contrast imaging (ECCI) [21], and transmission electron microscopy (TEM). The surface morphology was analysed with atomic force microscopy (AFM). Due to a relatively large (4.18%) lattice mismatch between the Ge and Si lattices, the formation of dislocations is inevitable. Minimizing the threading dislocation density (TDD) whilst obtaining smooth surfaces has been the priority for this study. The impact of annealing temperatures and the use of dopants on the quality of the Ge buffer layers have been investigated. The correlation between the thickness of the buffer layer and the TDD have also been analysed.

### 2.1 Effects of annealing

The first part of the study focused on optimizing annealing temperatures for highest quality buffer layers. A total of four 270 nm-thick samples have been grown, as shown in Fig. 1. First, a low-temperature (LT) layer of 30 nm of Ge was grown at substrate temperature of 250°C. Then, the substrate temperature was increased to 500°C and a further 180 nm of high-temperature (HT) Ge has been grown, followed by an in-situ 30-minute annealing step. Finally, the substrate temperature was reduced to 600°C and a 60-nm-thick Ge cap was grown. The four samples have been annealed at temperatures of 750, 800, 850 and 900°C respectively.
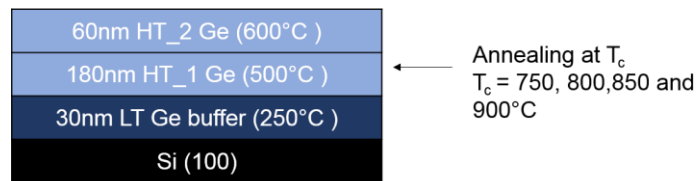


Fig. 1. Schematic structure of Ge buffer layers.

The ECCI and TEM results for those samples are shown in Fig. 2. A reduction in TDD has been observed for samples annealed at temperatures of 850 and 900°C. A high density of misfit dislocations can be observed at the Ge/Si interface, many of them propagating further as TDs and some of them penetrating the whole structure. Due to the low total thickness of the buffer layers (270 nm), the dislocations have limited space in which to annihilate before they reach the surface.
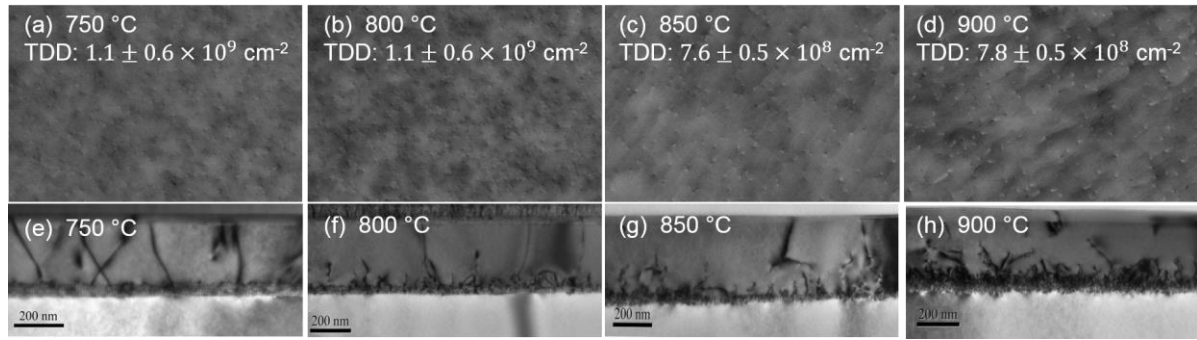
Fig. 2. Upper: ECCI and lower: TEM micrographs of Ge buffer layers annealed continuously for 30 minutes at (a) 750, (b) 800, (c) 850 and (d) 900°C, showing the threading dislocations on the surface (a-d) and across the sample thickness (e-h).

Surface analysis of the samples (Fig. 3) shows that the root-mean-square (RMS) roughness of the buffer layers increases slightly with increasing annealing temperatures. However, the surface of the sample annealed at 900°C is significantly rougher than that of the other samples as the temperature approaches melting point of Ge and 3D structures are formed. Considering both TDD and RMS toughness of samples annealed at different temperatures, as shown in Fig. 4, it suggests that 850°C is the optimal annealing temperature to lower the TDD whilst retaining a smooth surface.
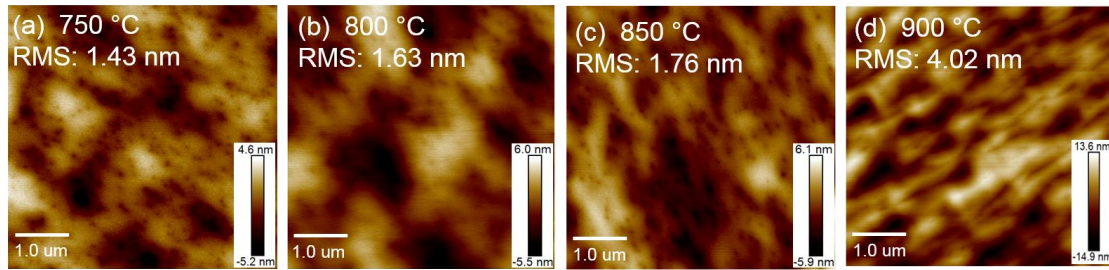


Fig. 3. 5μm×5μm AFM images of the surfaces of the buffer layers (270nm) annealed continuously for 30 minutes at 750, 800, 850 and 900°C.
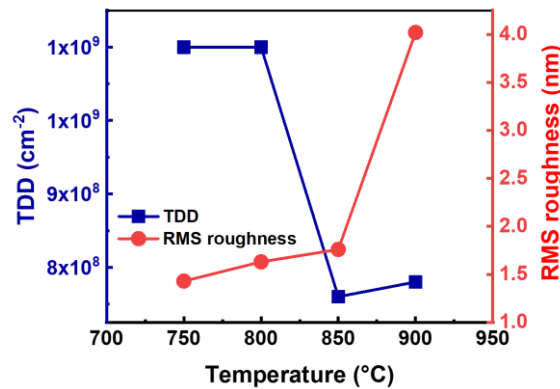


Fig. 4. Summary of TDD and RMS roughness for buffer layers (270nm) annealed continuously for 30 minutes at 750, 800, 850 and 900°C.

The composition of the samples was analyzed using an XRD method. The black line in Fig. 5 represents XRD measurement of the sample annealed at 750°C where two peaks can be clearly distinguished, the one on the left related to the Ge buffer layer, and the one on the right to the Si substrate. A third peak becomes visible just to the right of the Ge one when the annealing temperature is increased from 750 to 900°C. This peak can be attributed to GeSi alloy formed at the interface between Ge and Si due to Si

diffusion into Ge at high temperature. As can be seen from the green line, the third peak becomes comparable in strength to the Ge one after annealing at 900°C, which suggests significant diffusion of Si deep into the Ge buffer layer. Composition analysis of the sample estimates around 10% Si content in the GeSi layer.
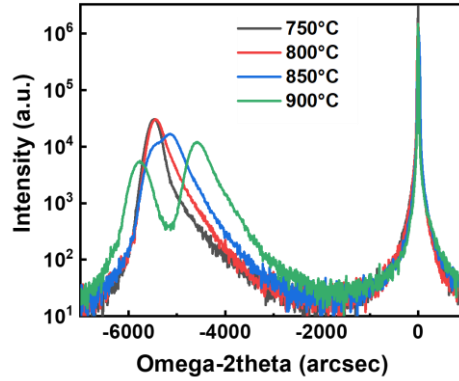


Fig. 5. XRD results for samples annealed at 750, 800, 850 and 900°C.

The next part of the annealing study focused on the impact of replacing the continuous 30 min annealing cycle with a periodic one consisting of five 5-minute anneals between high temperature ($T_H$) of 850°C and low temperature ($T_L$) of 450°C. The TEM results show a further small reduction in TDD which attributes to the TD glide and annihilation caused by thermal stress when cooling down and heating up [22, 23]. The AFM images also show a slight improvement in the surface smoothness of the sample. Hence all the following samples in this study have been annealed using a 5×5minute cycle between $T_H$= 850°C and $T_L$= 450°C.
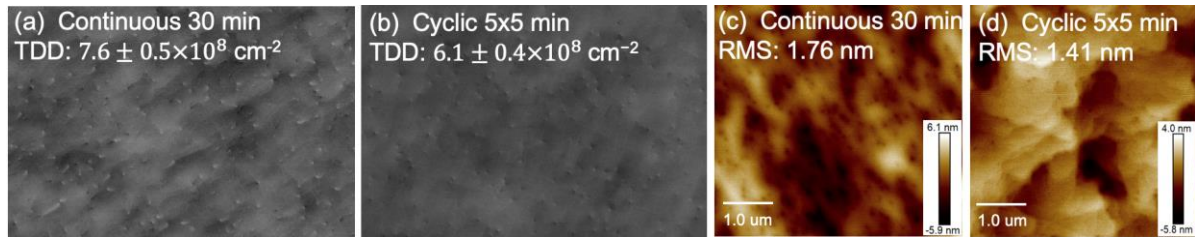


Fig. 6. A comparison between the continuous and cyclic annealing methods with ECCI showing threading dislocations and AFM images (5μm×5μm) showing surface roughness.


*2.2 Effects of thickness*

The second part of the study investigated the correlation between the thickness of the Ge buffer layers and TDD in order to evaluate the optimal thickness of the replacement buffer layer with best TDD/thickness reduction trade-off. A buffer layer sample has been grown based on Fig. 1 with increasing thickness of HT_2 layer and the total thicknesses reaching 500 nm. Fig. 7 shows surfaces of the 270 and 500nm samples observed with AFM and ECCI. The RMS roughness of the 500nm sample is slightly reduced compared to the 270-nm-thick buffer layer, however, a large number of dislocations can be noticed on the surface. These observations have been confirmed by ECCI imaging and TDD count. The dislocation density for the 270-nm-thick buffer layer is relatively high at around $6.1 \pm 0.44 \times 10^8/cm^2$. Increasing the thickness of the buffer layers to 500 nm helped to reduce the TDD to around $3.6 \pm 0.33 \times 10^8/cm^2$. These results supports the theory that the TDD is proportional to the inverse of the

film thickness [24]. The most optimal TDD/thickness trade-off is achieved for the thinner buffer layers and the small reduction in TDD of the thicker buffer layers does not justify adding the extra thickness.
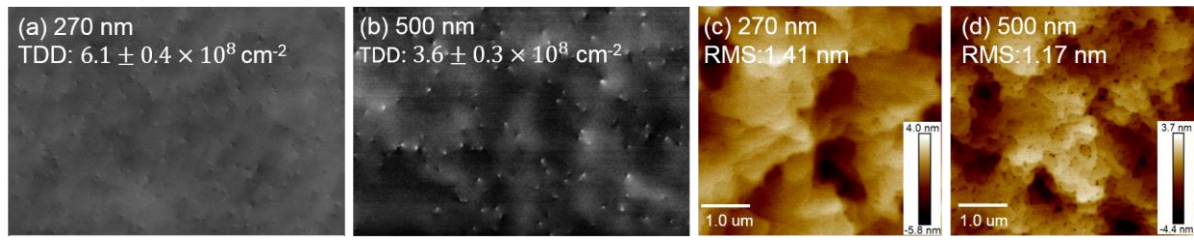


Fig. 7. A comparison of RMS roughness and TDD of 270 and 500nm Ge buffer layers on Si substrates.

*2.3 Effects of doping*

Use of dopants in the growth of buffer layer layers have been shown to reduce the number of threading dislocations and improve crystal quality [25, 26]. Therefore, the last part of this study investigated the impact of dopants on roughness of the samples and TDD. Another two samples have been grown, which were *in situ* doped with $5\times10^{18}$/cm$^3$ Baron (B) and Antimony (Sb), respectively, in the low temperature (LT) part of the buffer layer.
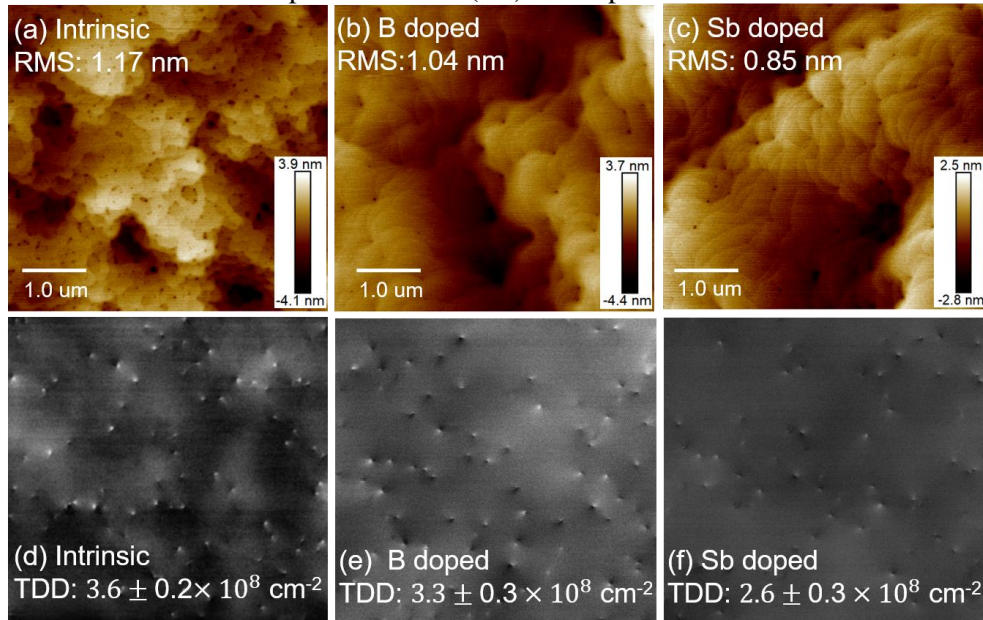


Fig. 8 shows a comparison of surface roughness and threading dislocations between the fully intrinsic, p-type doped (B) and n-type doped (Sb) samples. Comparing the RMS roughness of the three buffer layers (Fig. 8. (a)-(c)), Sb, which acts as surfactant, provide smother surface for the Sb-doped sample than the intrinsic and B doped ones. Also, an obvious reduction of TDD has been observed for Sb-doped one. The implement of Sb enhance the motion of TDs and thus increases the possibility that TDs with opposite Burger vector sign can meet and antihate each other [26, 27]. These results suggest that use of Sb dopants could improves the crystal quality of the Ge buffer layers.
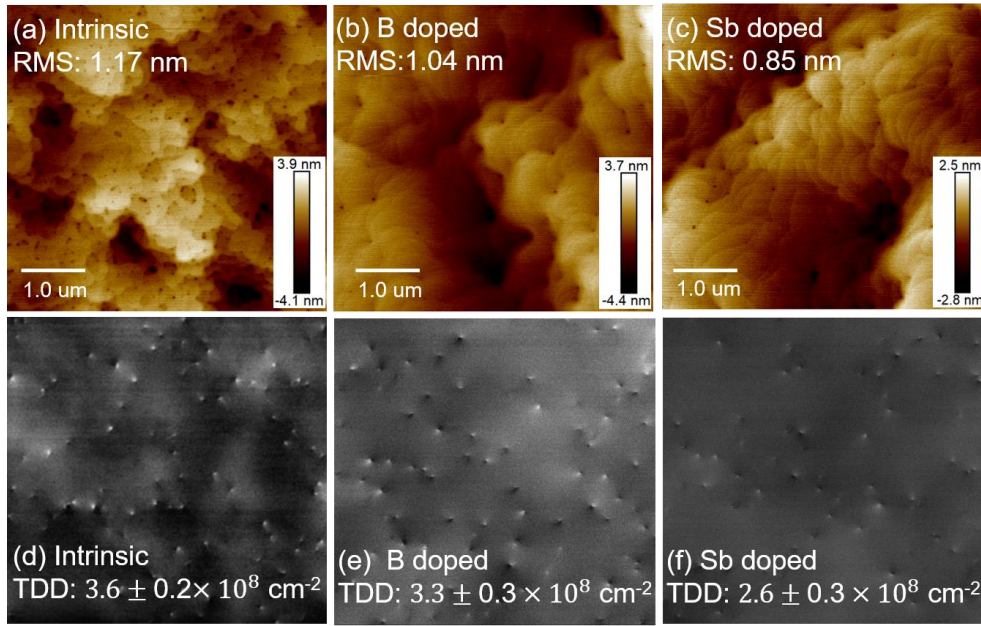
Fig. 8. A comparison of surface roughness and threading dislocation densities of intrinsic, p-doped and n-doped Ge buffer layer samples.

### 2.4 InAs/GaAs QD grown on Si substrate with Ge buffer layer layer

The thin Ge buffer layer is proposed to replace part of the thick GaAs buffer without introducing more defects. The GaAs-based buffer layer consisting of a 1-μm-thick bulk GaAs layer followed by three periods of dislocation filter layers was used for the growth of III-V QD laser [7]. When the GaAs buffer layer is approximately 1400 nm thick, including one dislocation filter layer, the TDD is estimated at around $5.9{\times}10^8/\,\mathrm{cm}^2$, which is comparable with the TDD in the 270-nm-thick Ge buffer layer $(6.1{\times}10^8/\mathrm{cm}^2$, Fig. 6.(b)). This means that the total thickness of the buffer layer can be reduced by at least 1μm without changing the TDD of the active layers if that part of the buffer layer is replaced by 200-300 nm of Ge

In order to confirm high quality of the Ge buffer layer obtained in this work and to demonstrate the possibility of replacing a part of the GaAs buffer layer with a thinner Ge one, a multi-layer self-assembled InAs QD structure was grown. The thin Ge buffer layer used for this sample was 270-nm-thick and annealed at 850°C in a 5x5min cycle. A Si (100) substrate with a 4° offcut was used to prevent APBs-related defects. The room-temperature PL of this QD sample is shown in Fig. . The peak wavelength of room temperature PL is at 1297nm with full-width at half-maximum (FWHM) equal to 35.7meV. In addition, a 1μm×1μm AFM image of InAs QDs is shown in the top left of Fig. , and a QDs density of about $3.5{\times}10^{10}/\mathrm{cm}^2$ is obtained.
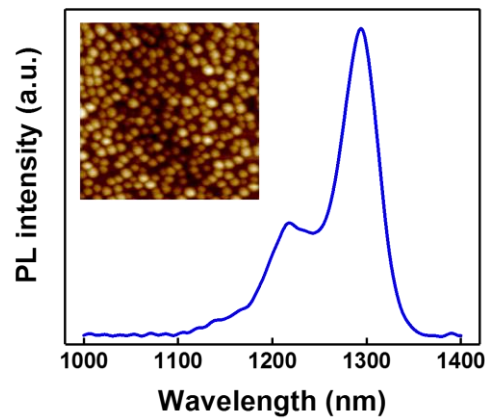
Fig. 9. Room-temperature PL result. inset: 1μm×1μm AFM image of InAs QDs.

## 3. Conclusion

Reducing the total thickness of the buffer layer should help eliminate the wafer cracking problem while keeping the TDD and crystal quality of the III-V active layers at a suitable level. The growth optimisation study described in this paper shown that the TDD density in 270-nm-thick Ge buffer layers on Si can be reduced to $6.2\times10^8$/cm$^2$. This has been achieved with an *in-situ* cyclic annealing method where the buffer layers were heated up to 850°C for 5 min in 5 cycles. Comparison with typical GaAs buffer layer shown that the same TDD can be achieved with 1300 nm of GaAs. These results confirm that the proposed replacement of a large part of the GaAs buffer layer with a significantly thinner Ge one is a viable solution. The overall thickness of the samples can be reduced by least 1μm without any negative impact on the quality of the active layers. Moreover, the reduction in thickness can be traded for further reduction of TDD as thinner core buffer layer achieved with Ge allows for additional dislocation filter layers whilst keeping the total thickness within reasonable limits.

## Author information

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