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Design of a Fully Tunable GaAs MESFET OTA-C Integrator Suitable For High-Precision Continuous-Time Filtering

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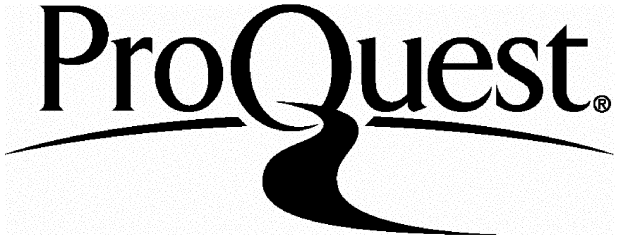
Thesis submitted to the University of London
for the degree of Doctor of Philosophy

May 1997



Abstract

The Operational Transconductance Amplifier-C (OTA-C) integrator has become the favoured building block for the implementation of integrated Continuous Time (CT) filters by many researchers around the world. The use of an OTA-C integrator for the realisation of an integrated CT filter does however, require full tunability, since the integrator time constants are dependent on absolute fabricated component values which are subject to process tolerances. In addition, the OTA may be used as a linear tunable resistor providing filter Q control. Integrated CT filters using OTA-C integrators have been implemented in Si CMOS, bipolar and GaAs MESFET technologies, with demonstrated operating frequencies ranging from 10s of KHz to 2GHz.

This thesis describes a novel circuit for the realisation of an OTA-C integrator to be used for the implementation of a bandpass CT filter. The new OTA-C integrator, which has been fabricated in 0.5μm GaAs MESFET technology, features *independently* tunable *intrinsic* output conductance, and transconductance. Thus additional OTAs configured as *extrinsic* linear resistors to provide Q-control are not required. A novel method of transconductance tuning is described which offers the widest tuning range reported in this technology, without varying any DC conditions and which preserves a good level of linearity. In addition, a single geometry device is used throughout the design, operating, with the exception of two triode region devices, under common bias conditions, well into the saturated region with no reliance on *early saturation* effects for gain enhancement. Using this approach a fully tunable 2nd order bandpass filter featuring independent control of centre frequency, Fo and Q has been fabricated using only *two* OTA-C integrators. The bandpass filter transfer function has been demonstrated with an accuracy of 1.5% both in amplitude and group delay operating at a filter complexity (FoQ) of 1.5GHz.

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To my Grandmother
Maria Cristina Bastianelli
1906 - 1991

"He who stands aloof runs the risk of believing himself better than others and misusing his critique of society as an ideology for his private interest. While he gropingly forms his own life in the frail image of true existence, he should never forget its frailty, nor how little the image is a substitute for true life."

Theodor Adorno, MINIMA MORALIA

Acknowledgment

There is no doubt in my mind that this thesis would not have been written if it were not for the help and support of others. I would firstly like to sincerely thank Professor Garath Parray of Oxford University, without who's encouragement this thesis would have remained half written. I would also like to thank Professor Chris Todd and Dr Mic Flanagen who's support and patience never wavered.

In addition, many thanks go to Dr David Haigh and to my supervisor Dr John Taylor. Firstly, for giving me the opportunity of joining the staff at UCL to undertake this very interesting research project; for many hours of technical discussions and for giving me the unforgettable experience of presenting my work to an international audience. Few things fill me with more terror. I'm also very grateful to David for steering me through the numerous pitfalls that are encountered when writing a thesis. Thank you for your time.

I would like to thank Kevin Lee and Tony Rivers of UCL for expert bonding of the IC's for testing. To Lola Christodoulou and Jill Curly, although employed as secretaries became more like therapists as time went on, many thanks to you both.

I would also like to take the opportunity to thank all the members of the DTI collaborate team. Joe Rodriguez of Bradford University for providing modelling information, Vic Potter and Tom Goodman of Cossor Electronics Ltd., for their technical assistance and use of their facilities, and of course for providing such a challenging filter to design. Many thanks to Roger Chalton and Garith Lloyd of GEC-Marconi Material Technology Ltd., for providing the design rule verification of the filter layout and final IC fabrication. I am also very grateful for the financial support from the DTI.

In addition, I would like to express my gratitude to my current employer, Nortel Semiconductors for allowing me access to computer and printing

facilities, allowing me to finish this thesis. Particular thanks go to George Swanson for his support and understanding during the final stages of writing up. I would also like to thank Alasdair Bruce for some very useful technical advice.

During my time at UCL I can honestly say that I met a variety of characters, none so colourful as the PhD students occupying room 621. Richard Mason, cool and unruffled, was always able to get the right information from megabits of data buried deep within the computer, unwilling to release its pearls to me. Thank you for all your help during my time at UCL. Hassan Shaffeeu, who seemed to have a gift, enabling him to log-on to any sun workstation, any were in the world from his hand held calculator, and Dave Grant who is capable of drinking entire breweries of Guinness in an evening, a dangerous man to know! All three were always willing to go for a beer and a curry. To this date, I still don't know the way to the Sun Inn from UCL! With these friends, my stay at UCL became unforgettable.

I wish also to thank my family for support while I embarked on my PhD. In particular to my brother, Lorenzo for helping me financially during my time at UCL and afterwards, without whom I would surly have sunk!

Finally, saving the most important until last, I wish to thank my partner, Teresa for her patience, support and understanding during my time at UCL and particularly since leaving when most of my spare time was spent writing up this thesis. We can finally enjoy a holiday together.

Abbreviations

Ao	Voltage Gain at DC
A(s)	Frequency Dependant Voltage Gain
B(s)	Frequency Dependent Feedback Gain
β	Transistor Gain Constant
CL	Load Capacitance
C	Capacitance
Cp	Parasitic Capacitance
CT	Continuous Time
C_{gs}	Gate Source Capacitance
C_{gd}	Gate Drain Capacitance
C_{gso}	Gate Source Capacitance at Zero Volts DC
C_{gdo}	Gate Drain Capacitance at Zero Volts DC
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
DTI	Department of Trade and Industry
D-MESFET	Depletion Mode Metal Semiconductor Field Effect Transistor
E-MESFET	Enhancement Mode Metal Semiconductor Field Effect Transistor
eV	Electron Volt
FET	Field Effect Transistor
Fo	Centre Frequency
FoQ	Bandpass Filter Complexity
ft	Unity Current Gain Frequency of a Transistor
FTI	Fully Tunable Integrator
Fu	Unity Voltage Gain Frequency of an OTA
Fp1	Cut Off Frequency due to Output Conductance of an OTA
Fp2	Cut Off Frequency due to Transconductance of an OTA
f1	Lower -3dB frequency for IMD Measurements
f2	Upper -3dB frequency for IMD Measurements
GaAs	Gallium Arsenide
GEC	General Electric Company

Gm	Forward Transconductance of an OTA
Gmo	Maximum Forward Transconductance of an OTA
Gms	Minimum Forward Transconductance of an OTA
Go	Total Output Conductance of OTA
GoA	Output Conductance of OTA
GoL	Output Conductance of OTA Load
Gm/Go	Voltage Gain of an OTA
gm	Small Signal Transconductance of a Transistor
go	Small Signal Output Conductance of a Transistor
gm/go	Intrinsic Small Signal Voltage Gain of a Transistor
HBT	Hetrojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
H(s)	Filter Transfer Function
H21	Transistor Frequency Dependant Current Gain
I	Current
i	Small Signal Current
IC	Integrated Circuit
Id	DC Drain to Source Current of a Transistor
IF	Intermediate Frequency
Idss	Saturated Drain to Source Current of a Transistor
IMD	Intermodulation Distortion
i_{bp}	Small Signal Current with Bandpass Response
j	Complex Operator
JFET	Junction Field Effect Transistor
K	Gain Sensitivity Constant
L	Inductance
LC	Inductor Capacitor
L20	GEC-Marconi, Low Threshold, GaAs MESFET Foundry Process
λ	Early Voltage of a Transistor
MESFET	Metal Semiconductor Field Effect Transistor
MISFET	Metal Insulated Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

OTA	Operational Transconductance Amplifier
OTA-C	Operational Transconductance Amplifier Capacitor Integrator
PCB	Printed Circuit Board
PLL	Phase Locked Loop
p-p	Peak to Peak Signal
$\varnothing$	Excess Phase Shift in an OTA
Q	Quality Factor
R	Resistance
RF	Radio Frequency
RLC	Resistor Inductor Capacitor
Rp	Parasitic Resistance
R1	Reference Input of the Spectrum Analyser
s	Laplace Operator
SC	Switched Capacitor
SFG	Signal Flow Graph
Si	Silicon
SM	Surface Mounted
SMA	Subminiature Connector, Type A
SPICE	Simulation Program with Integrated Circuit Emphasis
SSR	Secondary Surveillance Radar
STANAG	Standardisation Agreement
S1	Frequency Sweeping Source
S_y^x	Sensitivity of x to y
THD	Total Harmonic Distortion
Ti(s)	2nd order Transfer Function, Section i
T1	Test Input of the Spectrum Analyser
τ	Time Constant
UCL	University College London
V	Voltage
v	Small Signal Voltage
V_{bi}	Built In Voltage of a Transistor
V_{cf}	DC Frequency Control Voltage
V_{cq}	DC Q Control Voltage
V_{dg}	Drain Gate DC Voltage of a Transistor

V_{ds}	Drain Source DC Voltage of a Transistor
V_{gs}	Gate Source DC Voltage of a Transistor
V_{to}	Threshold Voltage of a FET
v_{ds}	Small Signal Drain Source Voltage of a Transistor
v_{gd}	Small Signal Gate Drain Voltage of a Transistor
vi_{bp}	Small Signal Voltage Representing Bandpass Current Response
ω_o	Centre Frequency ($2\pi Fo$)
Y_{ideal}	Ideal Input Admittance (Excluding Parasitic Phase Shifts)
yin	Small Signal Input Admittance
$Y_{practical}$	Input Admittance Including Parasitic Phase Shifts
Z	Impedance

CHAPTER 1

Introduction

1.1 Background

The widespread use of filters in telecommunications and instrumentation systems is well established [1,2], indeed it is difficult to name an electrical system without some form of signal filter. The technology employed to realise a particular filter is predominantly determined by the frequency of operation, however considerations of cost, size, capability for total integration and the nature of the response are all influencing factors.

In the 1920s to the late 1960s the majority of voice frequency filters were realised as discrete RLC networks. It was the recognition in the 1950s that reduction of size and ultimately cost could be potentially achieved by replacing the large and costly inductors with an active network. This active network consisted of resistors, capacitors and transistors configured to resonate as a tuned network. These active RC [2] networks remained essentially a research curiosity until the mid 1960s when good quality active components such as the Operational Amplifier (Op-Amp) became a reliable and inexpensive fundamental analogue building block.

In the early 1970s the potential for smaller size and lower cost for active RC filters was realised with the introduction of thin-film Integrated Circuits (IC). These thin film IC filters were composed of thin-film capacitors and resistors and a silicon Op-Amp as the active building block. These circuits however still required component trimming to achieve an accurate filter transfer function. The total integration of the filtering function onto the silicon IC however, was still the goal in achieving greater reduction in size and cost. The realisation of an active RC filter on a single IC required the process concerned to support the formation of resistive and capacitive layers. However, to achieve accurate and stable filter transfer functions there remains the problem that the integrated resistors and capacitors are subjected to independent process parameters during fabrication and temperature during operation. Thus, the filters transfer function can be

accurately determined by ratios of similar component values but not as products of component values.

This problem was overcome with the emergence of the Switched Capacitor (SC) technique in the late 1970s which first suggested the possibility of monolithic realisation of high-precision filters [3-6]. The use of the SC technique allowed the filter transfer function to be determined by the ratio of two integrated capacitors and the frequency of an external reference clock. As such, SC filters have been successfully applied in many applications and are routinely realised in analogue CMOS circuits. However, the ever increasing demands for higher frequency filtering functions posses a problem for SC filters, since the clock frequency is usually several times the passband frequencies of interest. Occasionally SC filters have been reported with passband frequencies greater than 1MHz [7], however these circuits are difficult to design, consume a large amount of power and generate clock noise. The requirements for higher passband frequencies in the 10s of MHz region has been demonstrated using SC filters realised in GaAs technology [8,9]. This solution however, is expensive both in cost and power consumption per pole of filtering function [10].In addition, this solution does not lead itself readily for total 'system on a chip' integration.

Subsequently, integrated Continuous Time (CT) filter methods were proposed [11,12] which overcame certain problems inherent in the SC approach. Since this method of filtering function is dependent upon the absolute values of integrated components, some form of tuning is required. However, CT filters avoid the over sampling requirement of SC systems and hence utilise the inherent bandwidth of the technology more fully. Thus the potential for total system integration is more readily achievable. The CT filtering method has been demonstrated in a variety of technologies and operating frequencies, filters implemented in silicon CMOS have been reported with passband frequencies in excess of 100MHz [13] while passband frequencies of 2GHz [14] have been demonstrated in GaAs technology.

The realisation of fully integrated CT filters have been studied for many

years, but it is clear from the literature that the widespread use of this technique has not been adopted by industry. This state of affairs is understandable since the design of the filter, the on chip tuning circuit and the tunable active building blocks themselves presents very challenging problems. The work outlined in this thesis is the design of such a challenging filter, used as an Intermediate Frequency (IF) stage of an aircraft transponder for Secondary Surveillance Radar (SSR). The requirements for high frequency and high precision transfer function both in amplitude and group delay reflect that the realisation of such a filter is currently achieved using a passive RLC network. It is hoped that the work described in the following chapters which explores the issues relating to the realisation of a fully integrated CT filter will help to bring forward the day when such a filter will be part of a fully integrated transponder for SSR on aircraft.

1.2 Overview of Thesis

The design of all active integrated filters requires the use of some form of active amplifier building block. In chapter two a review is undertaken to examine the different approaches that have been taken to realise an electronic integrator to form a 2nd order filter function and how such techniques can be extended to realise filters of higher orders. In addition, the effects of non-ideal integrator characteristics are examined, their origins reviewed and their impact on filter performance evaluated. Within the context of high order continuous time filter realisation, the various approaches of filter synthesis are examined with their inherent advantages and their ability to satisfy the requirement for on chip automatic filter tuning.

In chapter three a particular class of bandpass filter used by aircraft transponders for Secondary Surveillance Radar is examined with a view to a design realisation. The effects of non-ideal amplifier gain and bandwidth used to form the integrator are examined and their relation to overall transfer function accuracy both in amplitude and group delay are explored.

The technology employed in this program was an experimental GaAs MESFET process. In chapter four the problems of using GaAs for circuit design are examined assuming use of a public domain simulator such as SPICE. This chapter is not intended to provide a comprehensive critical review of the many GaAs MESFET models published in the literature, but rather to arrive at a strategy which enables limited modelling data to be used to best advantage.

In chapter five the issues relating to the design of a fully tunable integrator realised in GaAs MESFET technology are discussed. Comparisons are made with integrators realised in other technologies such as Silicon CMOS and Bipolar and an alternative, novel tunable integrator, both single-ended and fully balanced versions are presented. In addition, a fully tunable 2nd order bandpass filter is realised using the single-ended integrators.

In chapter six the results for a set of fabricated fully tunable, single-ended integrators and fully tunable 2nd order bandpass filter are presented in order to evaluate the circuit design and tuning methods presented in chapter five.

Finally, in chapter seven conclusions of this work are presented and recommendations for future research made.

1.3 Statement of Originality

The work described in this thesis forms part of an industrial DTI LINK (contract no. IED2/445/30/006) program of research, carried out by University College London, Bradford University, Cossor Electronics Ltd and GEC-Marconi Materials Technology (Caswell) Ltd.

For the part of the author, the following are the most significant results of the research presented. The circuits ideas, simulations and measured results are, to the best of the authors knowledge, original and produced nine publications [Published Papers] in total.

A simulated design of an OTA-C integrator implemented in GaAs MESFET technology which overcomes the difficulties that GaAs presents is proposed in chapter five. This design represents the only OTA-C integrator realised to date, in GaAs MESFET technology with the use of a novel method of variable voltage gain enhancement without the reliance of early saturation techniques. In addition, independent transconductance tuning is presented without the need to alter DC bias conditions. This resulted in the realisation of a fully tunable 2nd order bandpass filter with only two OTA-C integrators. The new 2nd order bandpass filter demonstrates independent centre frequency Fo and Q tuning. This work is original and produced four publications.

The full custom design of the tunable integrator and bandpass filter presented in chapter five was carried out by the author. In addition, the design and construction of the evaluation test boards and all measurements taken to verify the simulated performance of the novel circuits presented in chapter five, were also carried out by the author. The fabrication and design rule layout verification of the integrated circuits were carried out by GEC-Marconi Materials Technology Ltd. This work is original and produced a further four publications.

The specification for the IF bandpass filter to be realised for the aircraft transponder was provided by Cossor Electronics Ltd. The detail analysis and simulation of the filter to achieve an active realisation was carried out by the author and is presented in chapter three. This work is original and produced one publication.

Modelling information for the GaAs MESFET process to be employed, were derived by measurements performed by Bradford University. This modelling information formed the basis of chapter four and was used for all subsequent circuit simulations. All modelling data is duly acknowledged.

CHAPTER 2

Integrated Continuous Time Filters : A Review

2.1 Introduction

The design of all active integrated filters requires the use of some form of active amplifier building block. In this chapter a review is undertaken to examine the different approaches that have been taken to realise an electronic integrator to form a 2nd order filter and how such techniques can be extended to realise filters of higher orders.

In addition, the effects of non-ideal integrator characteristics are examined, their origins reviewed and their impact of filter performance evaluated. Within the context of high order continuous time filter realisation, the various approaches of filter synthesis are examined with their inherent advantages and their relation on the requirement for on chip automatic filter tuning.

2.2 The State Variable Filter

The simplest 2nd order filter that can be realised is shown by Fig 2.2-1 formed by a series combination of resistance, inductance and capacitance.

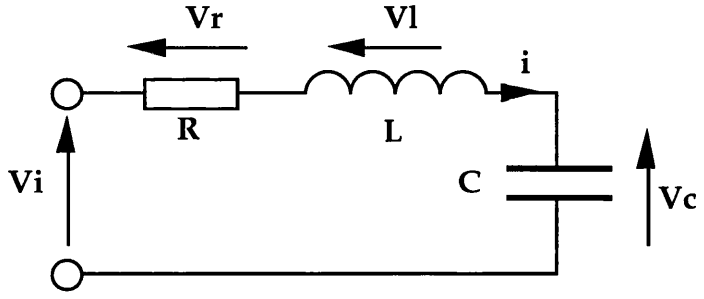


Fig 2.2-1 Simple RLC Filter

The voltage formed across the capacitor 'C' represents a 2nd order lowpass response, governed by the equation (2.2.1)

$$Vc_{lp} = \frac{1/LC\, Vi}{s^2 + s\frac{R}{L} + \frac{1}{LC}} \qquad (2.2.1)$$

If the current 'i' flowing through the inductor 'L' is considered, this represents a 2nd order bandpass response, governed by the equation (2.2.2)

$$i_{bp} = \frac{s/LC\, Vi}{s^2 + s\frac{R}{L} + \frac{1}{LC}} \qquad (2.2.2)$$

Where $\omega_0 = \frac{1}{\sqrt{LC}}$ and $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$

In both equations the cut-off and centre frequencies, ω_0 are determined by the reactive elements, 'L' and 'C' while the Q of the filter is independently determined by the resistive (loss) element, 'R'. If the filter became 'loss less', that is if $R \rightarrow 0$, then $Q \rightarrow \infty$.

To gain some insight into how a passive filter prototype may be designed and ultimately fabricated into an integrated filter, the above circuit may be represented as a state-variable equivalent circuit using the Signal Flow Graph (SFG) method [15,16]. By using the state equations as *current* flowing through the inductor and *voltage* developed across the capacitor, the equation (2.2.3) describes the RLC filter of Fig 2.2-1.

$$i_{bp} = \frac{Vi - Vr - Vc_{lp}}{sL} \equiv \frac{Vi - i_{bp}R - \frac{i_{bp}}{sC}}{sL} \qquad (2.2.3)$$

Equation (2.2.3) may be represented as an SFG shown by Fig 2.2-2

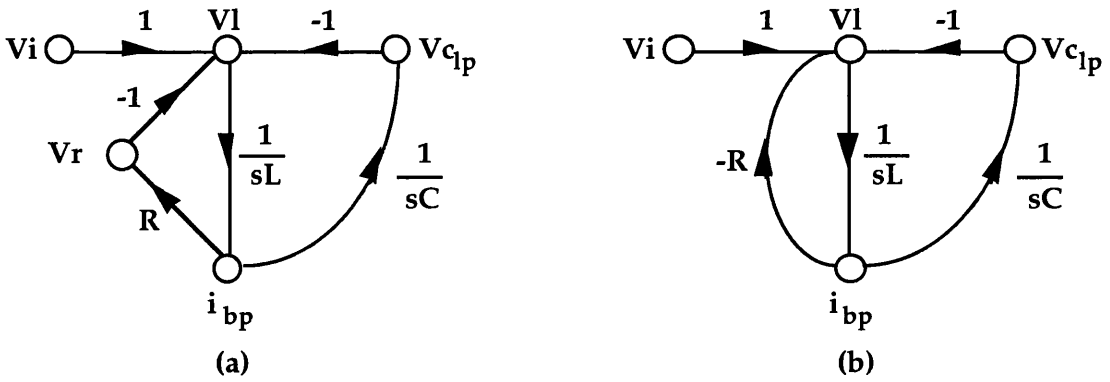


Fig 2.2-2 SFG of RLC Filter (a) Nodal Representation of Equation (2.2.3) (b) Equivalent

In the active simulation of this circuit, the currents are represented as voltage signals by multiplying the current nodal variable i_{bp} by a resistive scaling factor R, as shown by Fig 2.2-3.

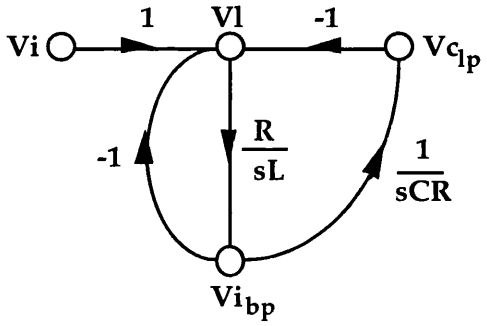


Fig 2.2-3 State-Variable *voltage* representation of an RLC Filter Prototype

By representing the RLC prototype using state-variables, a filter architecture with lowpass and bandpass *voltage* outputs is achieved. The troublesome inductor is replaced by a active integrator with a time constant τ=L/R. The cutoff and centre frequencies of the filter are determined by the integrator time constants (τ=L/R=CR) and the Q is independently determined by the feedback path -1 from the bandpass output 'vi_{bp}', representing a lossy integrator, as shown by Fig 2.2-4

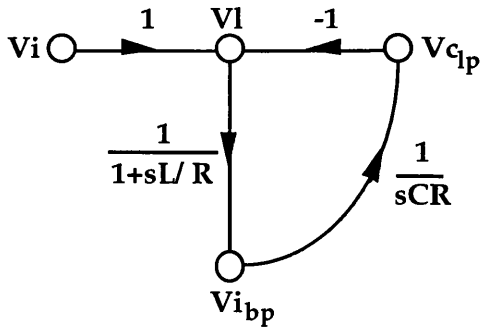


Fig 2.2-4 State-Variable representation of an RLC Filter with Lossy Inductor

In the context of a continuous time (CT) integrated filter, the cutoff and bandpass centre frequency would be subject to foundry tolerances of fabricated components and operating conditions. Thus, the design of the active integrator building blocks has an additional requirement of tunable time constants.

2.3 Active Tunable Integrators

2.3.1 Voltage Amplifier (Op Amp) Method

The simplest implementation of an active integrator is the use of an operational amplifier (op-amp) as shown by Fig 2.3.1-1, which has the classical integrating response given by equation (2.3.1.1) and its Laplace Transform by equation (2.3.1.2).

$$\text{Vout} = -\frac{1}{CR}\int \text{Vin}.dt \qquad (2.3.1.1)$$

$$\text{Vout} = -\frac{1}{sCR}\text{Vin} \qquad (2.3.1.2)$$

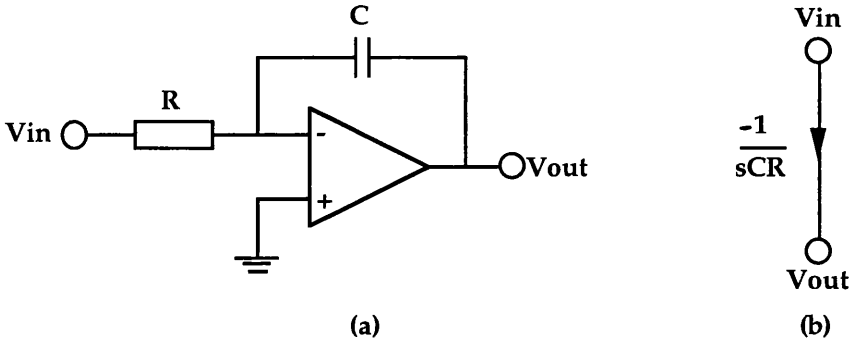


Fig 2.3.1-1 (a) Classical Active RC Integrator (b) SFG Representation

Since the fabricated component is the integrating capacitor 'C' which is subjected to foundry tolerances, the resistor is required to vary in order to maintain a constant 'τ'. This was first implemented by Banu & Tsividis [17] as a MOSFET device operating in its triode region, as shown by Fig 2.3.1-2a and 2.3.1-2b.

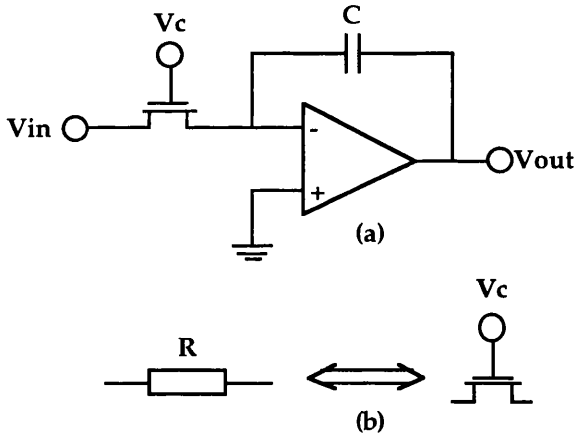


Fig 2.3.1-2 (a) Small-signal active RC integrator with variable time constant (b) Equivalent circuit element replacement

The method is commonly referred to as the MOSFET-C integrator. The triode region MOSFET resistors may also be used to implement the loss element within the state-variable filter to obtain Q control as shown by Fig 2.3.1-3.

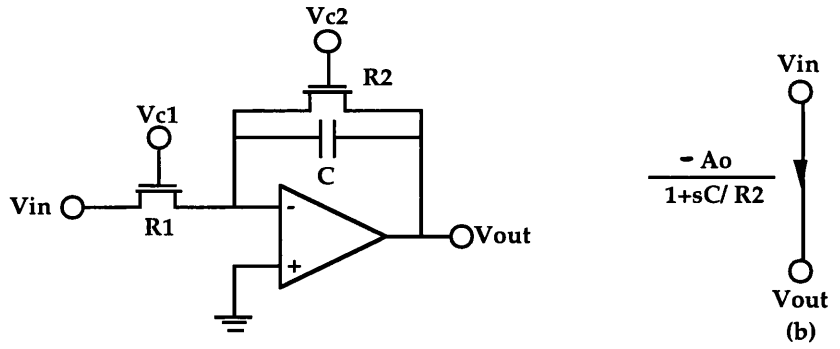


Fig 2.3.1-3 (a) Lossy Tunable Integrator (b) SFG Representation

where the voltage gain Ao= R2/R1 and the time constant τ=CR2.

The active realisation of the passive RLC filter prototype of Fig 2.2-1 using the MOSFET-C method is shown by Fig 2.3.1-4.

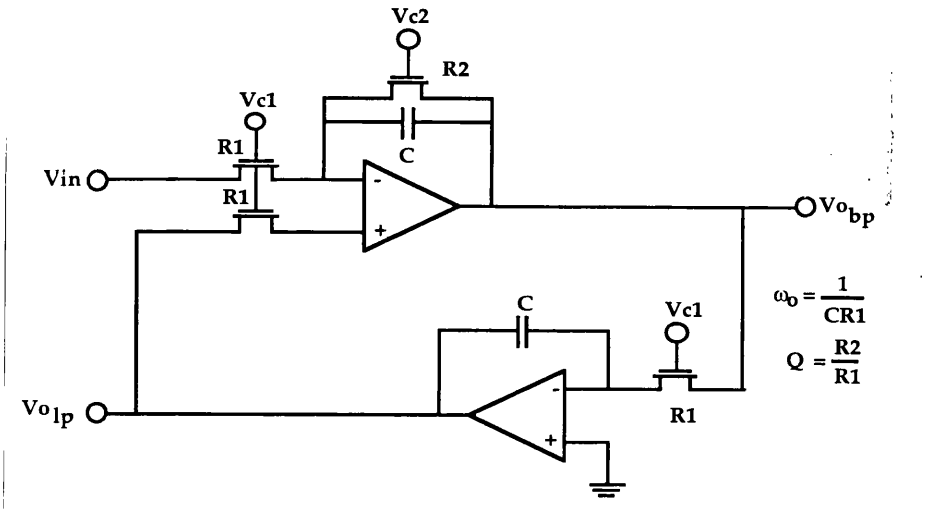


Fig 2.3.1-4 Active 2nd Order Filter using the MOSFET-C approach

Although the design objective is the realisation of a tunable integrator as the fundamental active building block, using this method the active element is the appropriate design of an op-amp. The implementation of the classical RC integrator shown above relies on the open loop gain of the amplifier to be (near) infinite, thus maintaining a virtual earth. In practice, all amplifiers have finite gain and an associated high frequency pole for closed loop compensation. Both non-idealities limit the quality of the integrating action and the signal processing frequency. In addition, the implementation

of the triode region MOSFET as a linear resistor directly in the signal path introduces considerable distortion [18].

2.3.2 Transconductance Amplifier Method

An alternative approach from the voltage amplifier method was the introduction of the transconductance amplifier as the active building block for integrators is shown by Fig 2.3.2-1.

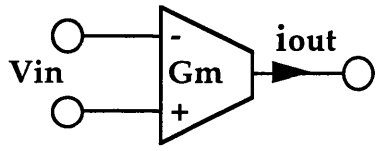


Fig 2.3.2-1 Symbol for a Transconductance Amplifier

The transconductance amplifier is in essence a voltage to current converter with a first order transfer characteristic given by equation (2.3.2.1).

$$iout = Gm(Vin) \qquad (2.3.2.1)$$

where the forward transconductance gain 'Gm' is in A/V.

An *ideal* transconductance amplifier has infinite input and output impedances, and as a consequence if the output is unloaded the effective voltage gain becomes infinite. If the output of a transconductance amplifier is loaded by a capacitor, as shown by Fig. 2.3.2-2, a Transconductance-C integrator is formed.

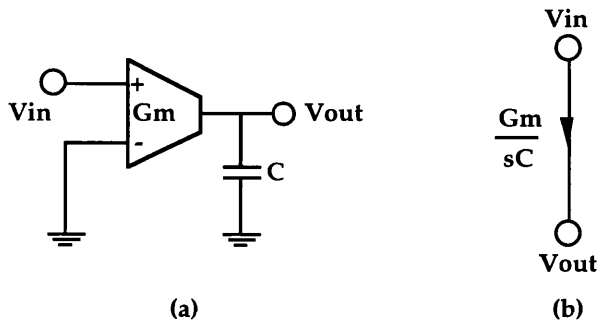


Fig 2.3.2-2 (a) Transconductance-C integrator (b) SFG Representation

The corresponding transfer characteristic is given by equation (2.3.2.2).

$$Vout = \frac{Gm}{sC} Vin \qquad (2.3.2.2)$$

where the time constant $\tau = C/Gm$.

If the load capacitor is subject to a foundry tolerances, the time constant may be maintained at its appropriate value by the adjustment of the forward transconductance 'Gm', thus a fundamental requirement of the Transconductance-C method is tunable Gm.

In addition, the use of a transconductance amplifier with the output connected to the input realises a linear grounded resistance of value $R=1/Gm$ as shown by Fig 2.3.2-3.

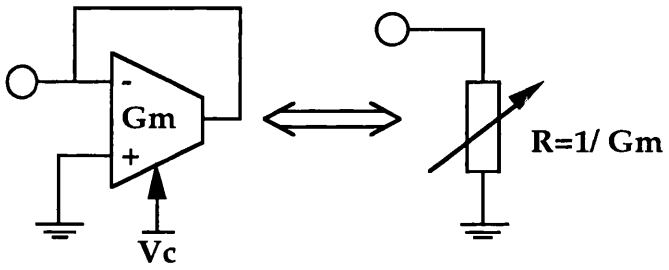


Fig 2.3.2-3 Simulating a grounded variable resistor with a Tunable Transconductor

If the transconductance amplifier exhibits a linear tunable Gm, then a linear tunable resistor determined by a control voltage 'Vc' may be implemented. As a result, the appropriate design of a linear tunable transconductance amplifier may be used to form both the active *gain* and *loss* elements in integrated tunable filter architecture as illustrated by Fig 2.3.2-4.

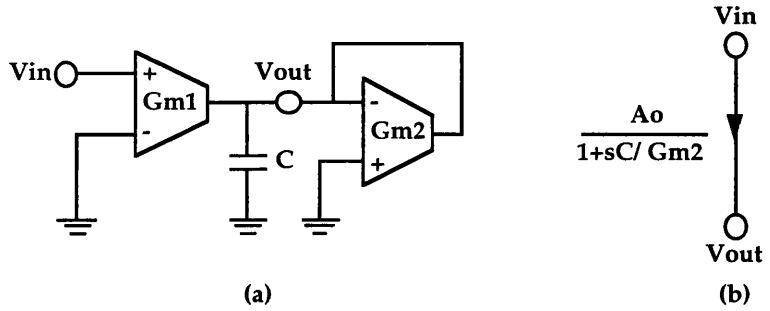


Fig 2.3.2-4 (a) Lossy Tunable Transconductance-C Integrator (b) SFG Representation

where the voltage gain Ao=Gm1/Gm2 and the time constant τ=C/Gm2

The active realisation of the passive RLC filter prototype of Fig 2.2-1 using the Transconductance-C method is shown by Fig 2.3.2-5.

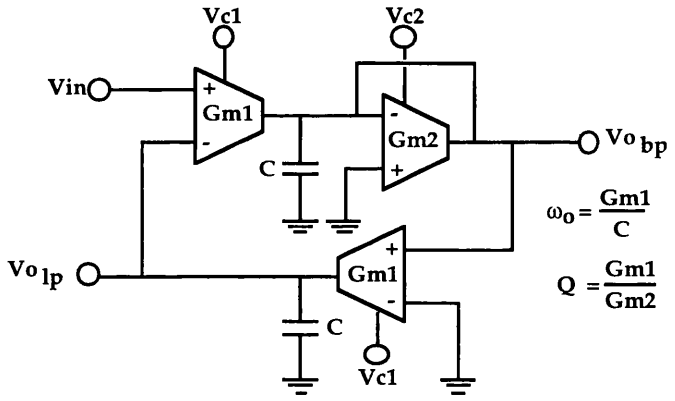


Fig 2.3.2-5 Active 2nd Order Filter using the Transconductance-C approach.

The use of the transconductance-C (or OTA-C) topologies has become the favoured method by many researcher around the world [19-22]. This choice is preferred over the MOSFET-C resistor replacement method, since the transconductor is usually a single-stage design (first stage of an op-amp) and the integrating capacitor may be considered as the compensation. This property provides superior high-frequency performance due in main to the simplicity of design and unlike the voltage gain stage of the MOSFET-C integrator, does not rely on the virtual earth principle. In addition, the transconductors do not need to drive triode region devices within the signal path, thus having the potential of lower distortion levels [23].

2.4 Higher Order Filters: Design Topologies

2.4.1 Cascade Approach

The realisation of active filters with an order greater than 2 may be achieved by connecting a number of 2nd order filter sections in cascade to provide an n^{th} order filter response. This technique is called the cascade approach.

The general transfer function for *any* type of filter response may be expressed as the product of 2nd order functions (sometimes referred to as biquads), as illustrated by Fig 2.4.1-1 and equation (2.4.1.1):

$$H(s) = \prod_{i=1}^{n} T_i(s) = \prod_{i=1}^{n} K_i \frac{\alpha_{2i}s^2 + \alpha_{1i}s + \alpha_{0i}}{s^2 + s\frac{\omega_{0i}}{Q_i} + \omega_{0i}^2} \qquad (2.4.1.1)$$

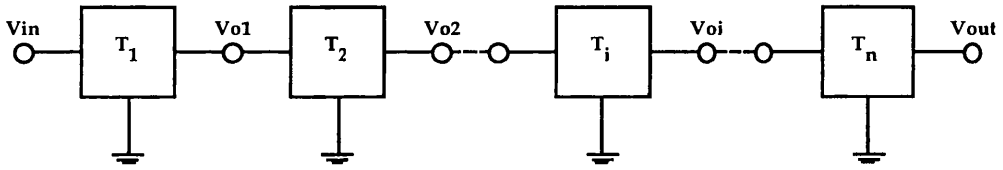


Fig 2.4.1-1 Cascade Realisation of an n^{th} Order Transfer Function

The transfer function of the individual 2nd order sections is given by $T_i(s)$. The gain of each section is defined by a constant k_i where the coefficients α_{2i}, α_{1i} and α_{0i} determine the type of 2nd order function $T_i(s)$ needed to realise an overall filter transfer function H(s), such as a low pass or bandpass response.

If the design of the 2nd order sections provide a low output impedance, or alternatively provide a high input impedance, then each section may be connected in cascade without causing mutual interaction due to loading and the product of each 2nd order section $T_i(s)$ would reliably realise the n^{th} order transfer function H(s).

The cascade method is widely used in industry [24-26] due to its well

understood, very easy implementation and efficient use of active elements, typically one active gain block per pole pair. It uses a modular approach and results in filters that show satisfactory performance in practice. This in the main may be due the fact that the cascade approach is very easy when considering on chip tuning, since each 2nd order section is responsible for the realisation of only one pole pair (or zero pair), the realisation of the individual critical frequencies of the filter are de-coupled from each other. To illustrate this point, equation (2.4.1.1) may be restricted to describe a single 2nd order bandpass filter section as equation (2.4.1.2):

$$T_i(s) = \frac{K_i \omega_{oi} s}{s^2 + s\frac{\omega_{oi}}{Q_i} + \omega_{oi}^2} \qquad (2.4.1.2)$$

At the centre frequency ω_{oi} of the bandpass filters, equation (2.4.1.2) reduces to equation (2.4.1.3):

$$T_i(\omega_{oi}) = K_i Q_i \qquad (2.4.1.3)$$

Thus, the maximum gain of the 2nd order bandpass filter occurs at the centre frequency and for a given section gain, K_i the Q for any given subsection of an nth order cascaded filter may be readily determined.

The major disadvantage with this method however, is an increased parameter passband sensitivity [27,28] of each 2nd order section, which becomes more severe as the order increases.

The cascade design, however is very flexible and this approach is *general*, in that an arbitrary transfer function can be realised with no restriction placed on the permitted location of the poles and zeros.

2.4.2 LC Ladder Prototype Approach

The ladder prototype approach to high order filter synthesis attempts to find an active realisation that inherits the recognised low passband sensitivity properties of a passive doubly terminated LC ladder filter [27].

A method which may be employed is the operational simulation of the LC ladder, where the active circuit is configured to realise the internal operation. Fundamentally, this method is based on simulating the Signal Flow Graph (SFG) of the ladder where all the voltages and currents are considered as signals which propagate through the circuit, as illustrated in section 2.2. By way of an example, the realisation of a general 4th order bandpass filter is considered.

Firstly, the 2nd order lowpass LC prototype is found from appropriate filter tables [29,30] or software [31] and transformed using the standard method to a 4th order bandpass as shown by Fig 2.4.2-1.

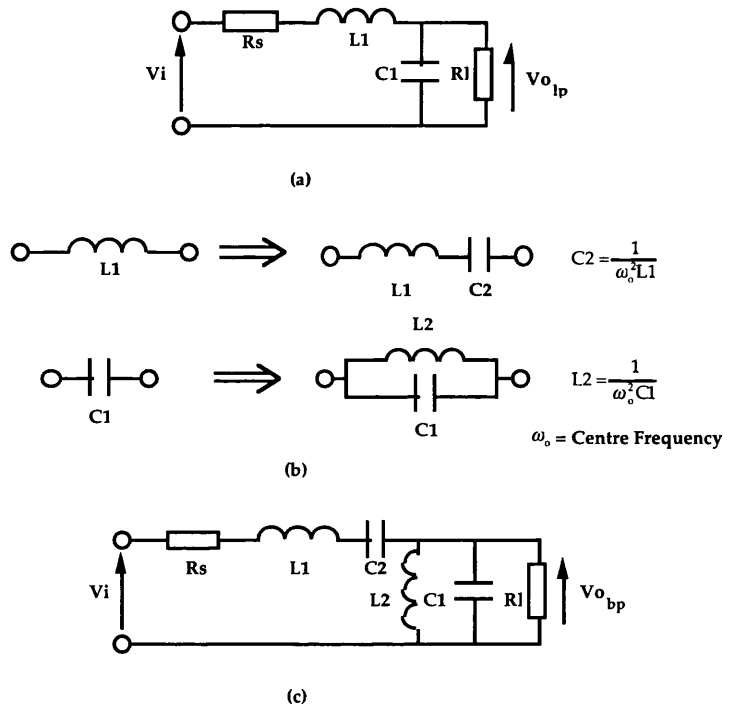


Fig 2.4.2-1 (a) Passive 2nd order Lowpass LC Prototype (b) Lowpass to Bandpass Transformation (c) Passive 4th order Bandpass LC Prototype

Once the required bandpass LC prototype has been determined, as shown by Fig 2.4.2-1 (c), the nodal voltages and currents may be represented by a SFG as shown by Fig 2.4.2-2.

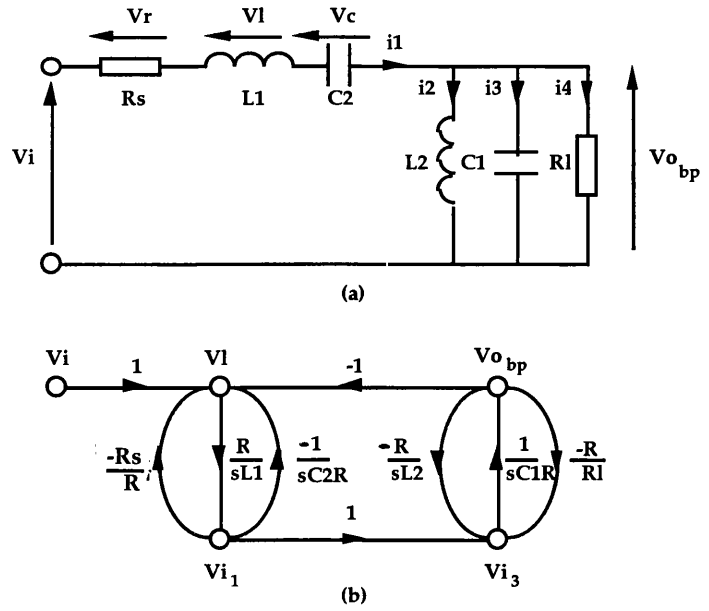


Fig 2.4.2-2 (a) Nodal Signals of 4th order Bandpass Filter (b) SFG Representation

As demonstrated in section 2.2, and shown by Fig 2.4.2-2 (b) the SFG represents the doubly terminated LC ladder filter with the nodal signals realised by integration. Thus, the inductors of the LC ladder filter may be replaced by active integrators. In addition, the SFG of Fig 2.4.2-2 (b) may be further reduced by arranging that the resistive scaling factor R is equal to the source and load resistance (ie Rs = Rl = R), thus the feedback paths formed by R/Rs and R/Rl may be incorporated into a lossy integrator, as illustrated by Figs 2.2-4 ,2.3.1-3 and 2.3.2-4 and shown by Fig 2.4.2-3.

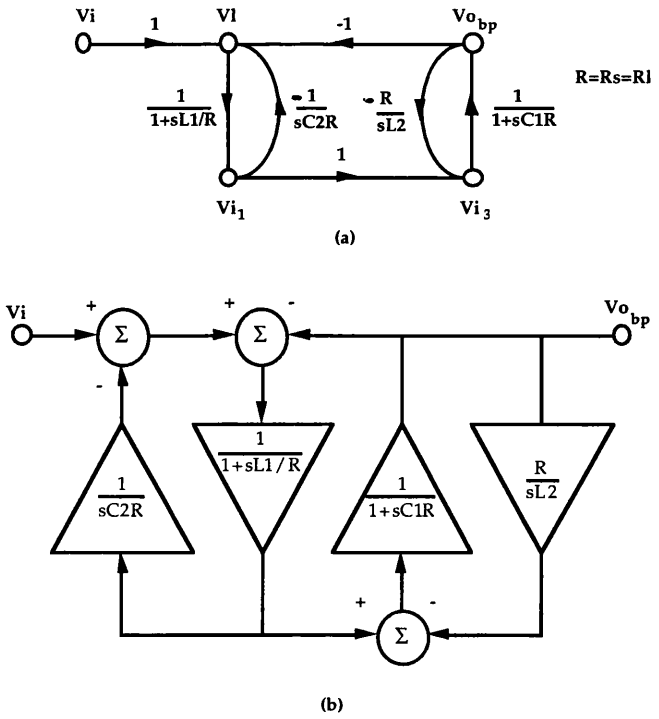


Fig 2.4.2-3 (a) Minimised SFG of 4th order LC bandpass Filter (b) Active Realisation using Integrators

Active filters simulating the behaviour of LC ladders have been found to have the lowest sensitivities to component tolerances and consequently are regarded as the most appropriate for filters with stringent requirements [32]. They have the additional advantage that they can draw on the wealth of knowledge gained in the area of analysis and synthesis of lossless filters from the many passive filters tables [29]. The disadvantage of this approach is that a passive LC prototype must, of course exist before an active simulation can be attempted.

However, despite the superior low passband sensitivity properties that the ladder synthesis poses, the main difficulty is the lack of a well understood, reliable tuning method. In contrast to the cascade approach, the problem arises in identifying which tunable component is to be varied in order to correct an observed error in the transmission characteristic. Although progress has been made in this area [33,34], the solutions are not general, but very much *ad hoc* and not as *transparent* as the cascade realisation.

2.4.3 Inductor Replacement Approach

An alternative method to realise an active doubly terminated LC ladder filter is by element substitution, where the inductors are replaced with an active simulation and inserted into the LC filter topology. The best known method for inductor simulation is that using a *gyrator* [19,35].

A gyrator is a two port network whose input impedance is represented by equation (2.4.3.1):

$$Z_{in}(s) = \frac{r^2}{Z_{load}(s)} = r^2 Y_{load}(s) \qquad (2.4.3.1)$$

where r is the gyrator resistance.

The customary circuit symbol for a gyrator is shown by Fig 2.4.3-1

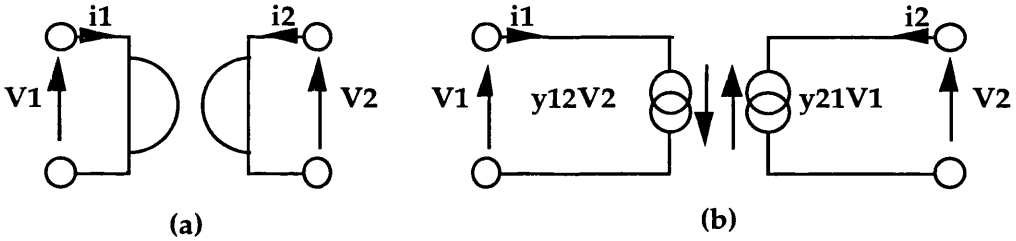


Fig 2.4.3-1 (a) Gyrator Symbol (b) Small Signal Equivalent Circuit

As shown by Fig 2.4.3-1 (b), the small signal equivalent circuit of a gyrator may be described by an admittance (y - parameter) transmission matrix given by equation (2.4.3.2):

$$\begin{pmatrix} i1 \\ i2 \end{pmatrix} = \begin{pmatrix} y11 & y12 \\ -y21 & y22 \end{pmatrix} \begin{pmatrix} V1 \\ V2 \end{pmatrix} \qquad (2.4.3.2)$$

Therefore, in order for Z_{in} to be proportional to Y_{load}, the gyrator of Fig 2.4.3-1 and described by equation (2.4.3.2), must have y11 = y22 = 0, thus equation (2.4.3.2) reduces to equation (2.4.3.3):

$$Z_{in} = \frac{V1}{i1} = \frac{-1}{y12y21}\left(\frac{i2}{V2}\right) = \frac{-Y_{load}}{y12y21} \qquad (2.4.3.3)$$

where $r^2=1/(y12y21)$, if y12 = y21 = Gm then $r^2=1/Gm^2$

Thus if $Y_{load}(s)=sC$ then $Z_{in}(s)$ would appear to be inductive as shown by Fig 2.4.3-2.

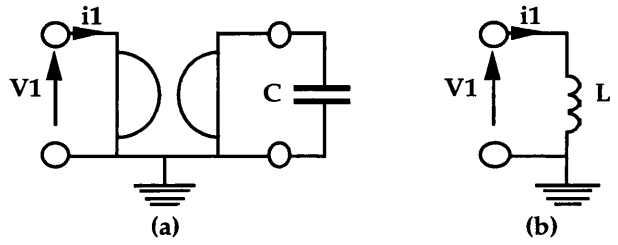


Fig 2.4.3-2 (a) Gyrator Simulation of a (b) grounded Inductor

Since most active gyrators have a common ground connection as shown by Fig 2.4.3-2, the simulated inductor would also be grounded. If a floating inductor is required in a filter prototype as shown by Fig 2.4.2-1(c) this would require the cascading of two grounded gyrators and a common capacitor as shown by Fig 2.4.3-3.

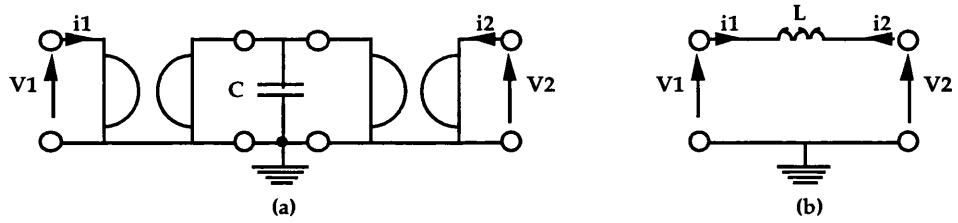


Fig 2.4.3-3 (a) Gyrator Simulation of a (b) floating Inductor

It is evident from Fig 2.4.3-1 that a gyrator consists of voltage controlled current sources and as such, the design is more easily accomplished with transconductance amplifiers. Thus, by using the small signal equivalent circuit of Fig 2.4.3-1 (b) a transconductance amplifier based gyrator realisation is shown by Fig 2.4.3-4.

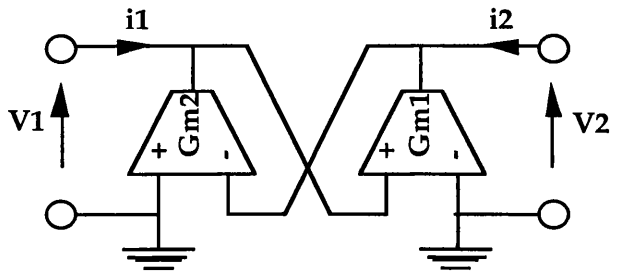


Fig 2.4.3-4 Gyrator Realisation using Transconductance Amplifiers

Using the transconductance amplifier based gyrator of Fig 2.4.3-4 both grounded and floating inductances can readly be realised as shown by Fig 2.4.3-5.

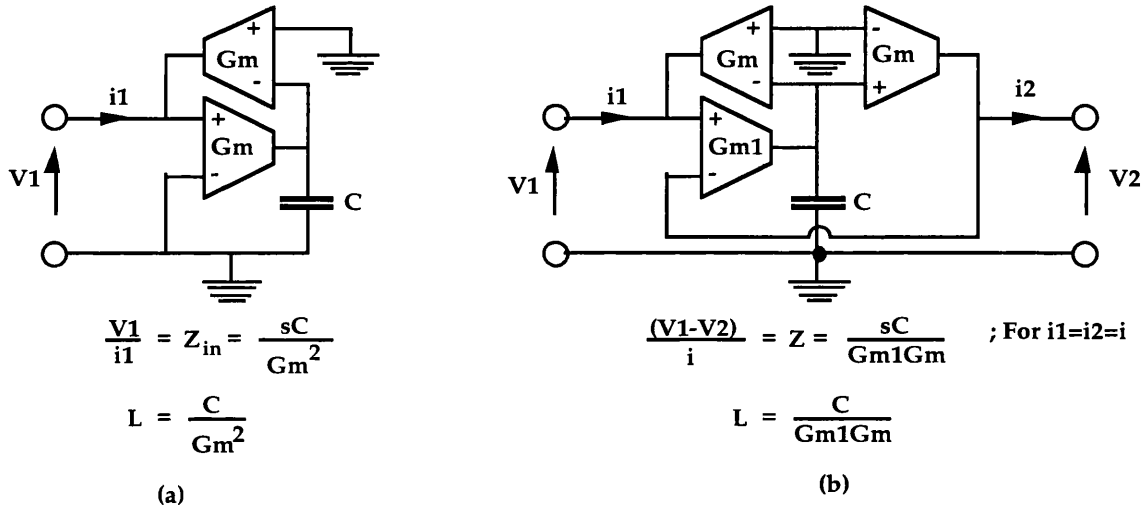


Fig 2.4.3-5 Transconductance-C Simulation of (a) grounded inductor and (b) floating inductor

By using the transconductor based active inductors shown by Fig 2.4.3-5 (a) & (b), the doubly terminated passive LC bandpass filter of Fig 2.4.2-1 (c) may be realised by the substitution of the floating inductor L1 and grounded inductor L2. All the properties of ladder filters, such as of low passband sensitivity are preserved by using this approach, but all the draw backs including complex tuning are not alleviated.

In addition, this approach to the realisation of active ladder filters, although simpler than the SFG method of synthesis may result in the use of more

active elements with a corresponding increase of power.

2.5 Integrators : Characteristics and Limitations

2.5.1 Ideal Integrator

Integrators form the basic building block to realise an active filter as illustrated in the previous sections. An ideal integrator transfer function is given by equation (2.5.1.1):

$$H(s) = \tau\frac{1}{s} \qquad (2.5.1.1)$$

where τ is a time constant

As illustrated in section 2.3, the time constant τ, of an integrator is formed by an RC time constant when an operational amplifier based integrator is used, or the time constant may be formed by C/Gm when an operational transconductance amplifier (OTA) based integrator is used. In both cases a fabricated capacitor is needed.

An ideal integrator thus has infinite DC gain, an attenuation of 20dB/decade (first order) frequency response and perfect –90° phase shift, as illustrated by Fig 2.5.1-1.

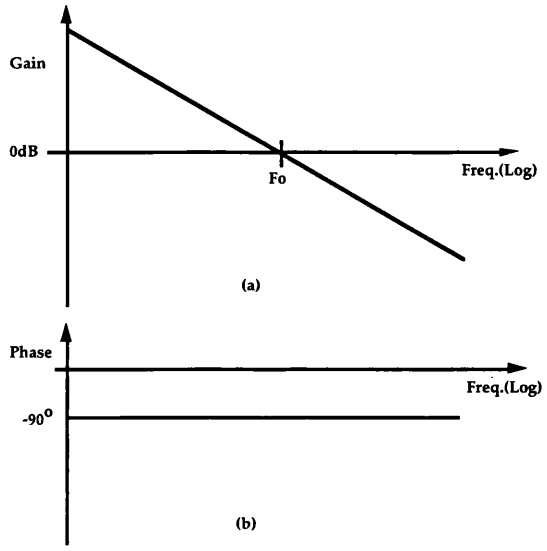


Fig 2.5.1-1 (a) Integrator Amplitude (b) Phase Response

The unity gain (0dB) frequency of the integrator corresponds to the cutoff frequency of a lowpass filter or the centre frequency of a bandpass filter.

2.5.2 Non Ideal (Practical) Integrator

In practice however, real integrators are formed using transistors which exhibit finite *ft* and finite output conductance. This has the effect of lowering the DC gain of the integrator from infinity and introducing high frequency poles. The non-ideal integrator transfer function may be described by equation (2.5.2.1):

$$H(s) = \frac{A_o}{(1+s\tau_1)(1+s\tau_2)(1+s\tau_3)....(1+s\tau_n)} \qquad (2.5.2.1)$$

As a result of a finite DC gain, A_O the first pole resulting in the 1/s term in equation (2.5.1.1) has moved from the origin of the real axis in the s-plane. The first pole now results in the term $1/(1+s\tau_1)$. The other poles result from the time constants associated with parasitics formed by internal nodes throughout the circuit. If the number of higher frequency poles can be minimised, modelling and predicting circuit behaviour is simplified. This leads to the principle of minimising the number of internal nodes in the design of aggressive high frequency circuits [13,36].

From equation (2.5.2.1), the integrating action would be formed at frequencies above the first pole location, τ_1 producing a –90° phase shift. The second pole, τ_2 would add an additional –90° phase shift and likewise for the other high frequency poles. The region of effective integrator operation (ie –90° phase shift) would lie between the first two pole locations. If the other poles are considered to be well outside this region (ie $\tau_2 >> \tau_3$) then equation (2.5.2.1) may be simplified to equation (2.5.2.2):

$$H(s) = \frac{A_o}{(1+s\tau_1)(1+s\tau_2)} \qquad (2.5.2.2)$$

Here the first pole τ_1 is referred to as the *dominant* pole and the *non-dominant* pole is formed by τ_2. The practical OTA-C integrator with non-ideal components is shown by Fig 2.5.2-1 and its corresponding frequency response is illustrated by Fig 2.5.2-2.

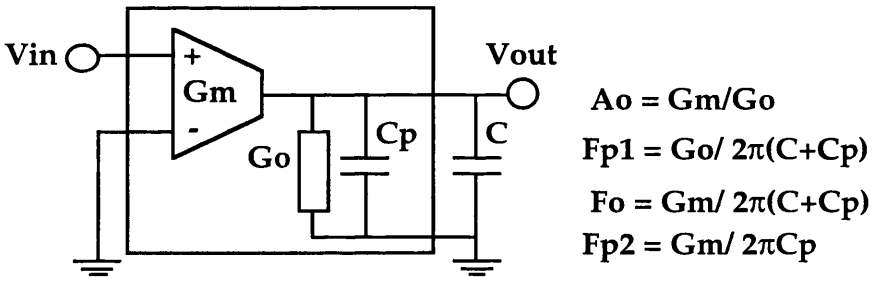


Fig 2.5.2-1 Practical (non-ideal) OTA-C integrator

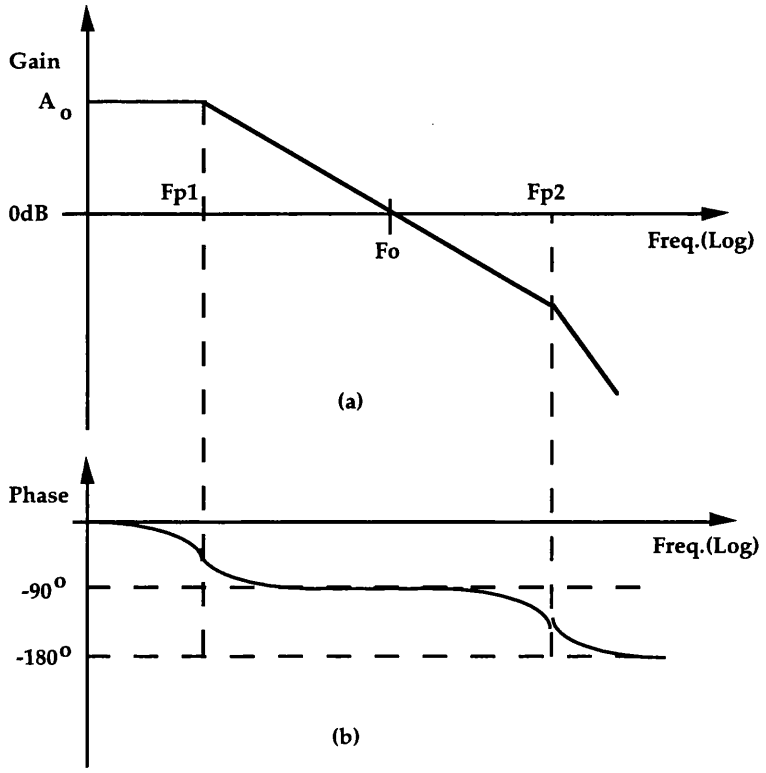


Fig 2.5.2-2 (a) Practical Integrator Amplitude (b) Phase Response

As illustrated by Fig 2.5.2-2, if the pole locations of τ_1 and τ_2 are sufficiently apart, the phase response would be close to the ideal integrator, approaching a constant –90° phase shift at Fo. However, the closer the two pole become the greater the the variation of phase shift, as illustrated by Table 2.5.2-1.

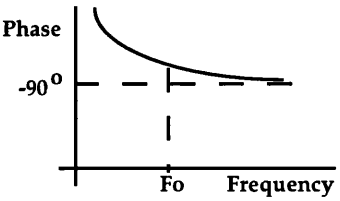
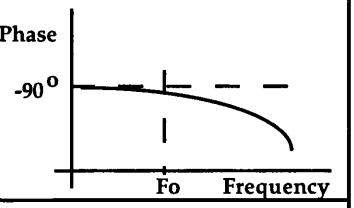
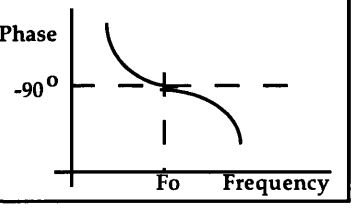
Pole Closest to Fo	Effect	Phase Response
P1	Phase Shift less than -90^{o} "Phase Lead"	
P2	Phase Shift greater than -90^{o} "Excess Phase"	
Equi-distant	Phase Shift -90^{o} at Fo, but with gradient	

Table 2.5.2-1 Effect of pole spacing on phase shift of Integrator

The major problem in designing integrators for high frequency CT filters is the existence of the non-dominant pole which exhibits excess phase as illustrated by Table 2.5.2-1. In the case of an OTA-C integrator, this non-dominant pole appears as a parasitic capacitance Cp, in parallel with the integrating capacitor. These non-ideal characteristics of a practical integrator are best illustrated by considering a gyrator of section 2.4.3 constructed using practical transconductance amplifiers of Fig 2.5.2-1, to form a 2nd order resonator, shown by Fig 2.5.2-3.

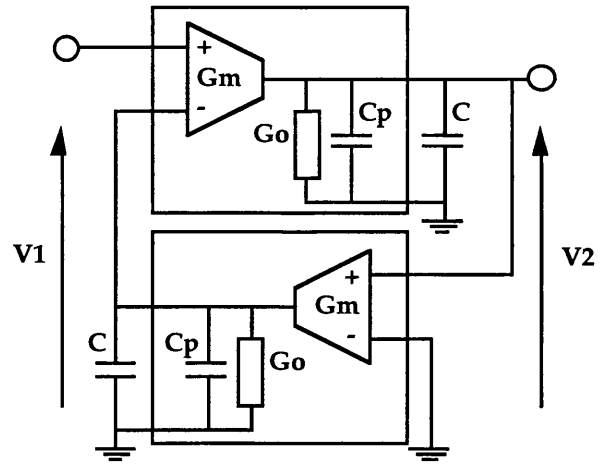


Fig 2.5.2-3 2nd order Resonator realisation using practical Transconductance Amplifiers

The ideal admittance matrix for the gyrator is derived by equation (2.4.3.2) and re-arranged to give equation (2.5.2.3):

$$Y_{ideal} = \begin{pmatrix} 0 & Gm \\ -Gm & 0 \end{pmatrix} \qquad (2.5.2.3)$$

However, considering that the resonator is constructed from non-ideal (practical) transconductance amplifiers, shown by Fig 2.5.2-3 which exhibit finite DC gain resulting in finite output conductance, Go and the presence of excess phase shirts, ∅ in the forward transconductance gain, Gm, the admittance matrix for a non-ideal gyrator is described by equation (2.5.2.4):

$$Y_{practical} = \begin{pmatrix} Go & Gme^{-j(\varnothing/2)} \\ -Gme^{-j(\varnothing/2)} & Go \end{pmatrix} \qquad (2.5.2.4)$$

This has two effects, firstly the unity gain frequency Fo of the gyrator is no longer dependent upon the Gm/C as illustrated by equation (2.5.2.5):

$$\omega_o = \frac{Gm}{C+Cp} = \frac{Gm/C}{1+Cp/C} \qquad (2.5.2.5)$$

Depending upon the ratio of the parasitic capacitance, Cp and the load

capacitance, C which for high frequency designs should be as small as possible, this effect can be corrected by some form of tuning.

In addition, the state variable filters shown by Fig. 2.3.1-4 and Fig 2.3.2-5 indicate that the Q of the respective filters should be determined purely by a ratio of fabricated component parameters, such as resistance or transconductance. However, as a result of the parasitic capacitance, Cp each transconductance amplifier exhibits excess phase ∅, resulting in Q enhancement, creating Q errors [19,37,38] and the first order relationship determining Q is no longer valid. To determine the *real* Q of the resonator circuit of Fig 2.5.2-3, the admittance matrix of equation (2.5.2.4) is evaluated. By making the following assumptions that $\varnothing << 1$ and $Gm >> Go$ for $yload = j\omega C$, then the input admittance would approximate to equation (2.5.2.6):

$$yin = 2Go - \frac{\varnothing Gm^2}{\omega C} + j\omega C - j\frac{Gm^2}{\omega C} \qquad (2.5.2.6)$$

which contains a negative real term proportional to excess phase, ∅.

If a further assumption is made, that for a first order $\omega = Gm/C$, then equation (2.5.2.6) can be re-arranged to give an expression for Q, by equation (2.5.2.7):

$$\frac{1}{Q} = \frac{2Go}{Gm} - \varnothing \qquad (2.5.2.7)$$

Furthermore, the sensitivity of Q to excess phase, ∅ can be obtained by differentiating equation (2.5.2.7) to give equation (2.5.2.8):

$$S_{\varnothing}^{Q} = \frac{\partial Q/Q}{\partial \varnothing/\varnothing} = \varnothing Q \qquad (2.5.2.8)$$

which demonstrates that the resonator of Fig 2.5.2-3 becomes more critical to design as ∅ or Q increases.

Theoretically this parasitic capacitance could be absorbed into the total integrating capacitance value, this however presents several problems.

The parasitics are not accurately known. In aggressive high frequency designs [13] in which the parasitics form a large part of the integrating capacitor, this problem means an increased uncertainty in the integrating capacitance value. Although automatic frequency and Q tuning would be used, this is complicated if integrators do not exhibit a low phase error. Phase correcting networks may be employed to cancel the phase error of the non-dominant pole but these usually work "exactly" at a given frequency (ie centre frequency) and the remaining error increases as one moves away from this given frequency, this can lead to significant Q error in the filter response.

The presence of parasitics can worsen capacitance matching accuracy and in turn leads to increased integrator mismatch. For the best matching, the proportion of parasitic capacitance to the total integrating capacitance, Cp/C should be kept the same for each integrator [39], this requires very detailed foundry modelling.

Parasitics do not track the main integrating capacitor well [40] in the presence of fabrication process variations. This once more increases integrator mismatch, unless the proportion of parasitic capacitance is kept to a minimum. In addition, the parasitics are in general non-linear. This can cause distortion as well as dependence of the frequency response on the signal amplitude and power supply voltage.

Practical transconductance-C filters have been fabricated with parasitics as high as 20% of the total integrating capacitance [13]. While they do achieve high frequency performance, they require very careful device level design with detailed knowledge of the process and are still only capable of only moderate linearity. For the application of precision high frequency design, it is desirable to maintain as low a ratio of Cp/C as possible to achieve high linearity and operating frequency while achieving accurate tuning.

2.5.3 Transconductance - Op Amp Integrator

The troublesome parasitic capacitance, Cp at the output of a transconductance amplifier can be forced to a near ground potential by using a scheme called the Transconductance-C Op Amp integrator as illustrated by Fig 2.5.3-1

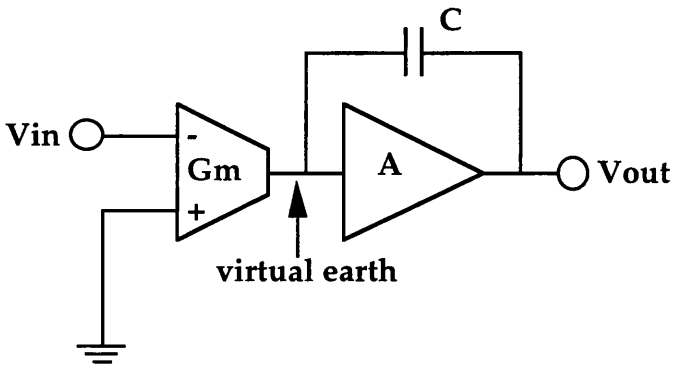


Fig 2.5.3-1 Transconductance-C Op Amp Integrator

This scheme is in essence a combination of both the Voltage Amplifier and Transconductance Amplifier integrator. By connecting a tunable transconductor at the input of the high gain voltage amplifier (Op Amp) the integrating action is still determined by Gm/C. This scheme has been successfully employed in the designs of a number of high frequency (up to 20MHz) CT filters [41].

The main advantage of employing the transconductance-C op amp integrator is that the parasitic capacitance connected at the output of the transconductance amplifier is now at a near ground potential (ie virtual earth). Since there would be very little voltage change across the parasitics their effects would be greatly reduced. In addition, since the output of the transconductor is connected to a virtual earth, its output does not require to provide large voltage swings. The demanding requirement of a low output conductance of the transconductance would also be relaxed since the output is now connected to a virtual earth.

However, the presence of two active elements in the transconductance-C op

amp integrator would inevitably lead to a greater power dissipation, despite the fact that the power dissipation of the individual elements would be reduced due to relaxed performance requirements. Moreover the bandwidth of the op-amp would be required to be much greater than that of the the integrating action formed by Gm/C while at the same time providing a high voltage gain, A to maintain the virtual earth, without which the benefits of such a scheme are questionable. Thus, for very aggressive high frequency designs, the minimisation of the number of internal nodes using the transconductance approach is favoured.

2.6 Automatic Tuning

To manufacture a practical integrated filter with its component tolerances, some form of fine tuning is unavoidable. As demonstrated by sections 2.2 and 2.3, the filter frequency parameters are determined by RC products or C/Gm ratios, which implies that to achieve accurate filter performance *absolute* values of resistors, transconductors and capacitors must be realised.

Since the fabricated tolerances of components are not sufficiently small to realise accurate filter performance, or as a result of varying operating conditions, the generally adopted solution to this dilemma is an automatic electronic tuning scheme as part of the total continuous time filter circuitry. This implies that, in tuning, a measurement of the filter performance is made, compared with a standard, determining an error (if one exists) and finally applying a correcting signal, if required, to the filter, thus reducing the error, resulting in the desired filter performance.

A review of the literature [33-35,37,38,42-44] revels that the most reliable form of filter tuning firstly requires some form of reference signal or clock. From the filter response to this *external* reference signal at a given frequency, the tuning circuitry detects and identifies any mistuning and the appropriate corrections are then applied via a suitable control circuit to the filter. A technique which has been successfully adopted in the realisation of fabricated continuous time filters is the *Master - Slave* scheme [38,44]

shown by Fig 2.6-1.

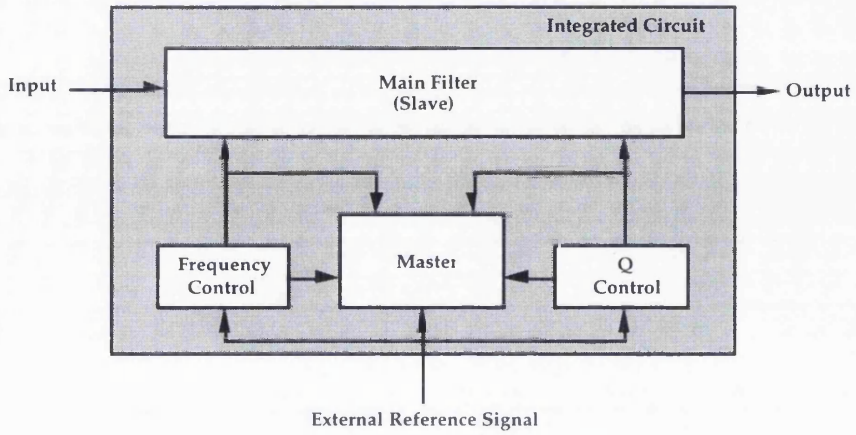


Fig 2.6-1 Master - Slave Automatic Tuning System Block Diagram

The proposed tuning scheme illustrated by Fig 2.6-1 is the application of a reference frequency signal to the 'master' filter. This filter is required to model the main filter and *track* all parameter changes. The master filter may in some cases be identical to the main filter or contain the appropriate subsections to determine the required operating conditions. Tuning is accomplished by the application of the correcting signal *simultaneously* to both the master and the main filter which is considered as *slaved*.

The tuning system contains a frequency - control subsection that compares the master response to the external reference signal. This is usually accomplished by arranging the main filter (or elements of it) within the closed loop of a phase - locked loop (PLL) [38]. Thus, the main filter resonance is compared to the external reference frequency and the phase error (and hence frequency) is reduced and the correcting signal applied to the slave.

In addition, the automatic tuning system shown by Fig 2.6-1 includes a Q control subsection. As illustrated in section 2.2 and 2.3, the Q of a filter is determined by the ratio of similar parameters, such as resistance or transconductance and as such is a dimensionless number and may, in principle be realised with great accuracy. However, the realisation of practical

integrators, as illustrated in section 2.5 demonstrates that Q is sensitive to parasitic phase shifts or excess phase resulting in non-dominant poles [19,44]. These excess phase shifts result in Q errors, particularly if high Q filters are required [38,44], thus it is usual that a Q - control subsection is included in an automatic tuning scheme.

In principle, to determine the correct value of Q for a given filter would require the measurement of the filter response at three different frequencies (ie ±3dB points and the centre frequency). This however, detracts from a relatively simple control circuitry. Fortunately, a simpler approach may be employed as illustrated in section 2.4.1, which makes use of the fact that the 2nd order section Q may be determined from the amplitude of the transfer function at the centre frequency. The 2nd order section gain would normally be determined by a ratio of like components, such as resistors for appropriate section scaling and as such be accurately known. If the master filter is correctly tuned at the centre frequency, and as such this frequency condition known, an alternative element of the master filter would be at peak gain, thus with the use of a peak detection system [38,45] the Q errors may be determined and minimised and the correcting signal applied to the slave.

It is self evident, upon reflection that the concept of self tuning is not a trivial process. A single external reference frequency is applied to the integrated filter. From magnitude and phase measured automatically at this reference frequency, the tuning circuitry decides on the basis of these errors which filter components to vary in order to maintain the filter correct response. The difficulty of this process cannot be emphasised strongly enough, that the realisation of a fully integrated continuous time filter must be considered at the outset whether the contemplated filter structure *is* tunable. That is, whether an observed error can be corrected by varying the value of a dominant tunable component. Considerations of tunability may for example dictate the realisation of a cascade design in spite of the superiority, in principle of an active realisation of a ladder filter.

2.7 Review of Fabricated Continuous Time Filters

A review of *fabricated* continuous time filters was undertaken and summarised in Table 2.7-1. The criteria for this review was to determine the highest frequency of operation achieved, employing the differing types of active integrators discussed in sections 2.3 and 2.5.3. In addition, the filter order, type (ie lowpass or bandpass) and the various technologies used is also indicated.

Integrator	Reference	Technology	Highest Frequency	Highest Complexity (FoQ)	Filter Type & Order
Voltage Amplifier Tunable Resistor Integrator	11,12,17,18	Si CMOS	8KHz	——	5th order lowpass
	43	Si Bipolar	10.7MHz	62MHz	6th order bandpass
	52	Bi-CMOS	3.3KHz	——	5th order lowpass
Tunable Transconductance Amplifier Integrator	13,21-23,25,26 37,42,46-48	Si CMOS	110MHz	——	3rd order lowpass
	19,20,24,43 49,53	Si Bipolar	100MHz	1400MHz	2nd order bandpass
	55,56	Bi-CMOS	32MHz	——	2nd order lowpass
	14,54	GaAs	2GHz	32GHz	2nd order bandpass
Tunable Transconductance Amplifier Op-Amp Integrator	57	Si CMOS	25KHz		2nd order lowpass
	41	Bi-CMOS	20MHz	——	6th order lowpass

Table 2.7-1 Review of Fabricated CT Filters for High Frequency Operation

An additional parameter, filter 'complexity', defined as the FoQ product of a bandpass filter is also included. This parameter is important when comparing the relative performance of a lowpass filter to a bandpass filter. Since the design of lowpass filter usually require low values of Q, the excess phase shifts of the integrators used are less severe (section 2.5.2). Alternatively bandpass filters may be employed with very high Q values to increase the filter selectivity and as such, the excess phase shifts in the integrator are more significant, particularly at higher frequencies.

To illustrate this point, a 2nd order bandpass filter fabricated in CMOS

technology with a centre frequency, Fo of 13.7MHz and a Q of 50 was reported by Wang, Lue and Abidi [46]. The centre frequency is an order of magnitude lower than a lowpass filter operating at 110MHz in the same technology reported by Nata [13]. To compare the difficulty in the design, the bandpass filter may be considered to be operating at an FoQ of 687MHz.

However, some care must be taken when comparing the operation of a bandpass filter to a lowpass filter. If the excess phase shifts of the integrators are significant, particularly at high frequencies, the bandpass filter may only be marginally stable and thus would present considerable problems in control. Such circuits have been employed to achieve high selectivity [14] but not to form a 2nd order section of a higher order filter with control.

An example of this situation is the fabrication of a 2nd order bandpass filter in 0.9μ CMOS with a centre frequency, Fo of 450MHz reported by Snelgrove [47]. Although the frequency of operation is high, excess phase shifts within the integrator are significant at 300MHz and the filter Q was designed to be nominally 1.1. If the Q of the filter approaches 10 the control circuit experiences difficulty in adaptation. In addition, this 2nd order filter may be regarded as pseudo continuous time, since the frequency tuning was achieved by switching various capacitance values in the integrator circuit.

The review also demonstrates clearly the wide spread adoption of the transconductance-C integrator as the favoured active element for the realisation of high frequency filters, as illustrated by Table 2.7-1. The transconductance-C has been employed for both cascade designs [43,44,48,49], active ladder simulation [21-23,42] to inductor replacements [37,46] and has proved to be very versatile as seen by the various technologies that have been employed. In addition, the use of the transconductance-C integrator has been employed by industry for commercial disk drive CT filters. This is significant since these CT filters are required to realise a low group delay response [24-26,49] to prevent pulse distortion and thus low excess phase integrators must be employed in a wide band technology. An example of this type of filter was the realisation of a 7th order 10 - 30MHz lowpass Bessel

filter fabricated in Si bipolar, reported by De Veirman and Yamasaki [49]. In addition, the filter topology employed was the cascade realisation. This filter achieved <2% group delay variation from the ideal prototype.

The cascade realisation of a high order bandpass filter has also been demonstrated. A 4MHz, transconductance-C based, 8th order Chebyshv bandpass filter realised in Si CMOS was reported by Park and Schaumann [44]. The filter topology was a cascade of 2nd order bandpass sections, the highest FoQ was 105MHz (Fo=4.42MHz., Q=23.86). The filter employed a master-slave method of automatic tuning of each 2nd order bandpass section centre frequency, Fo and Q. The cascade approach was adopted for its transparent tuning (section 2.6) which is more important if high section Qs are required. The overall passband amplitude response however suffered from Q enhancement at the higher frequencies (>4MHz) raising the passband ripple to 1db, this in the main is contributed by the low bandwidth technology employed.

The use of the cascade approach for high order filter synthesis has been adopted by other commercial IC manufactures, such as National Semiconductor [50] and Maxim [51]. The attraction of this approach is that by providing a number of 2nd order state variable filters on an IC, a customised filter may be realised. For example, a 4th order lowpass filter may be configured by one customer while the same IC may be configured as a 4th order bandpass filter by another customer. However, as mentioned above the filter complexity must be considered and as such lowpass filters that exhibit low Qs can operate at higher frequencies while high Q bandpass filters would operate at lower centre frequencies [50].

2.8 Conclusion

In this chapter, the issues relating to the realisation of an active integrator suitable for continuous time filters have been considered. A review was undertaken to examine how the integrators may be employed for the realisation of high order filtering functions and the impact of automatic tuning.

The effects of non-ideal integrator characteristics were explored. The effects of finite DC gain and the presence of non-dominant poles resulting in excess phase shifts result in integrators which may produce severe Q enhancement, particularly for high frequency, high Q bandpass filters. The reduction in these parasitic effects are discussed with a view to achieve high frequency precision filtering. As a result, the transconductance-C integrator has emerged as the strongest candidate for the application of high frequency CT filters.

In addition, the cascade approach to the realisation of high order filters is a strong candidate. Although the active simulation of an LC filter prototype produces the lowest passband sensitivities the main difficulty is the lack of a well understood, reliable tuning method, particularly for high Q filters, in contrast to the cascade approach. Although progress has been made in this area, the solutions are not general, but very much *ad hoc* and not as *transparent* as for the cascade realisation.

CHAPTER 3

High Order Continuous Time Filters : Fundamental Active Building Blocks and Their Limitations

3.1 Introduction

The issues relating to the realisation of a high order, high precision continuous-time active filter suitable for integration are complex. The use of a filter architecture, ease of tuning and effects of non-ideal active building blocks and their relation to transfer function accuracy must all be considered.

In this chapter a particular class of bandpass filter is examined with a view to a design realisation. The degree of non-ideal amplifier gain and bandwidth and their relation to overall transfer function accuracy is explored to determine design limits and the choice of technology to be used.

3.2 Realisation of a 12th order Bandpass Filter

3.2.1 Motivation for Active Filter Integration

The motivation for integrating passive filters are varied and wide. These may be due to lowering material cost, achieving greater performance or in most cases, both [58].

One particular application for achieving such a goal is the transponder on military and civil aircraft used for Secondary Surveillance Radar (SSR) [59,60]. A simplified block diagram of the RF front end of the transponder is shown by Fig 3.2.1-1.

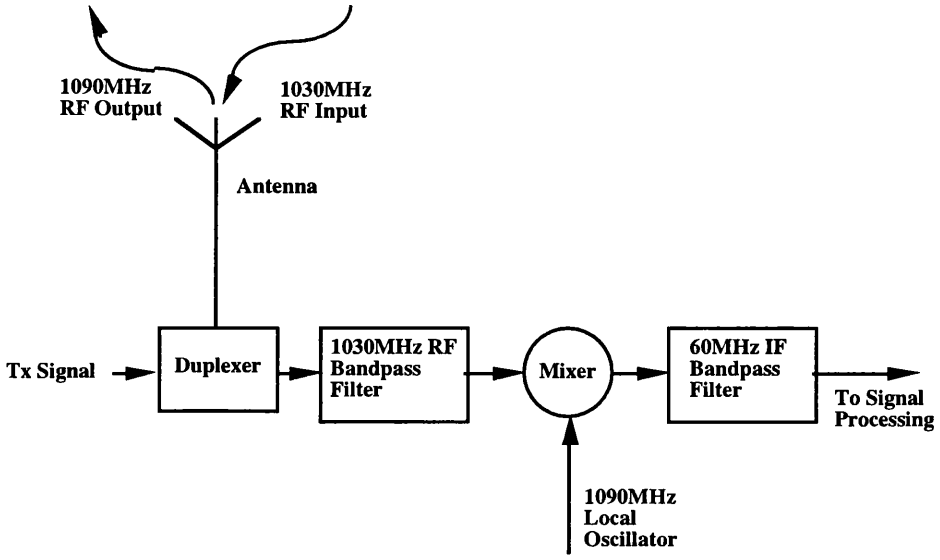


Fig 3.2.1-1 Simplified RF Front-end of SSR Transponder

On current aircraft SSR transponders, the received signal pulses are on a 1030MHz carrier. It is normal to include both RF and IF filters to block out of band signals which could possibly come from nearby primary radar and saturate the front end of the receiver.

The IF filter is designed to have a greater selectivity than the RF filter in order to reject adjacent channel interference [61]. The type of bandpass filter used has a strong influence on the pulse performance of the receiver and is required to have sufficiently wide passband response to accommodate the carrier frequency, a constant group delay across the passband so that the pulse envelope is undistorted and maximum attenuation outside the passband to reduce the effects of the out of band signals. Such a stringent filter specification has been internationally agreed according to a Standardisation Agreement, STANAG4193 [62].

No one filter is capable of providing all the properties and as such a compromise has been achieved. The requirement for constant group delay to prevent pulse distortion can be met by a Gaussian class of filter, while in the stop band a Chebyshev response would meet the requirements for signal attenuation. The type of filter used for the IF section of the SSR transponder

is a Transitional Gaussian to 6dB centred at 60MHz with an overall Q of 6.

Currently all the subsections of the SSR transponder shown by Fig 3.2.1-1, are in discrete form, both the RF and IF filters are realised using passive components. The 60MHz IF filter in particular requires high quality components and custom set-up [63] prior to installation to achieve such a demanding performance. A long term objective would be to integrate both the RF and IF filters along with the the down converter mixer on one integrated circuit. The IC is intended to maintain the filter transfer function accuracy and not require any complex pre-installation set-up. For the remainder of the chapter the problem of integrating the IF bandpass filter is investigated with a *view* to facilitate the integration of the remaining sub-sections.

3.2.2 Passive Prototype of a Transitional Gaussian to 6dB

The normalised low-pass passive prototype realisation of a 6th order Transitional Gaussian to 6dB was obtained using standard table of values [30] and shown by Fig 3.2.2-1.

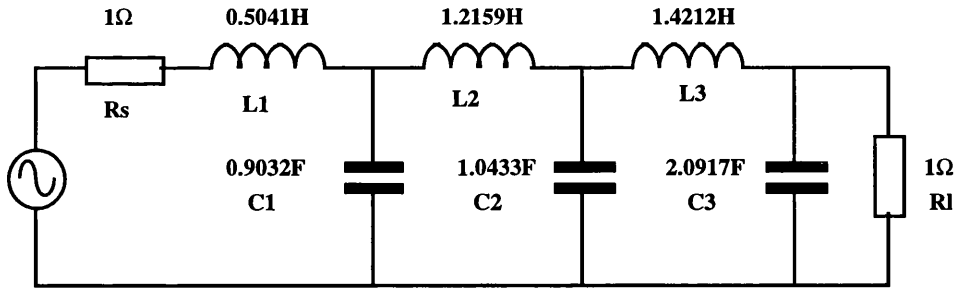


Fig 3.2.2-1 Normalised Low-Pass Transitional Gaussian to 6dB

The normalised low-pass filter shown by Fig 3.2.2-1 has a cut-off frequency at 1rad/sec. The required filter response is a bandpass with a Q of 6 centred at 60MHz. Using the appropriate transforms and frequency scaling factor, demonstrated in chapter two, the normalised 6th order low pass is transformed to a 12th order bandpass and the de-normalised passive filter prototype is shown by Fig 3.2.2-2.

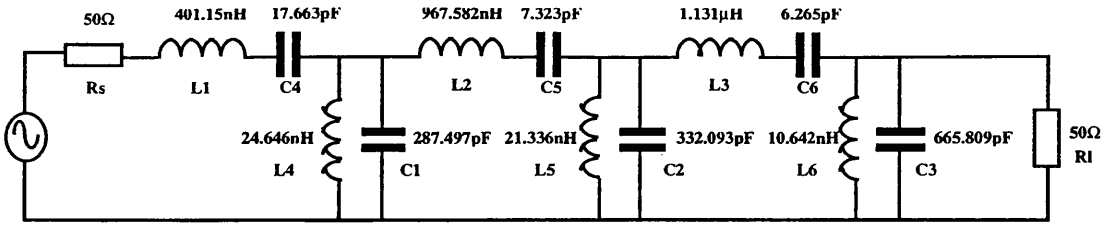


Fig 3.2.2-2 Passive Prototype of a 12th order Bandpass Transitional Gaussian to 6dB (Q of 6, Centre Frequency of 60MHz)

The amplitude and group delay response of the 12th order bandpass filter are shown by Figs 3.2.2-2 a & b

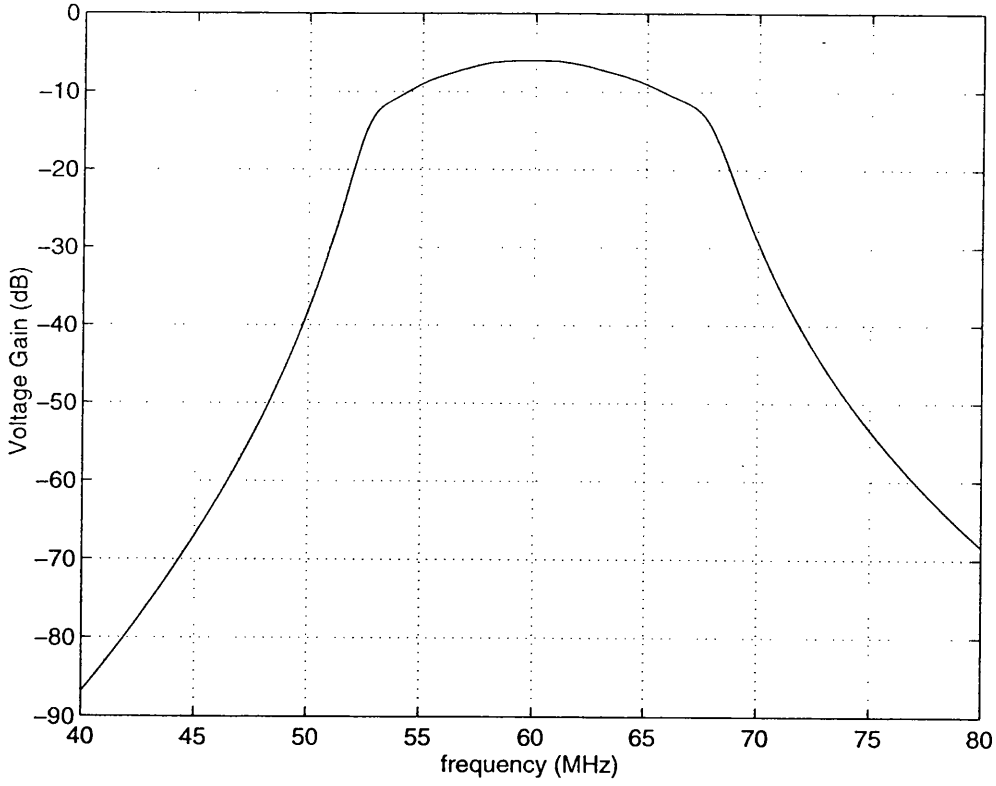


Fig 3.2.2-2a Amplitude Response of 12th order Transitional Gaussian to 6dB

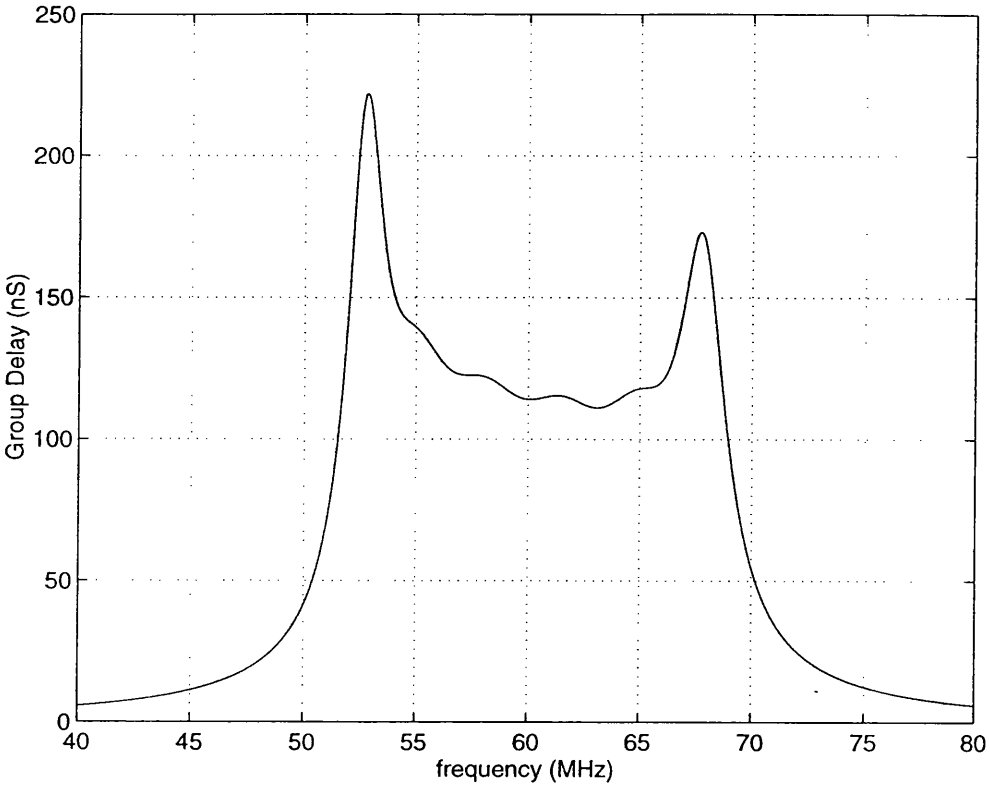


Fig 3.2.2-2b Group Delay Response of 12th Transitional Gaussian to 6dB

As shown by the amplitude response of the filter, within the pass band the amplitude response has a dome like configuration which is determined by the Gaussian response of the transfer function. Once the pass band response reaches an attenuation of 6dB from its peak value the response is Chebyshev in nature providing the rapid attenuation required.

The group delay response is also characterised by the transitional response. Within the pass band the group delay is relatively constant, only exhibiting a ripple of *10ns which is provided by the Gaussian part of the filter. Outside the pass band however the group delay rapidly rises as the Chebyshev response provides the steep attenuation as shown by the amplitude response.

* within the critical bandwidth of 57MHz to 63MHz

3.2.3 Active Transitional Gaussian using 2nd order sections

The realisation of the 12th order bandpass Transitional Gaussian to 6dB shown by Fig 3.2.2-2 in an active form may be achieved by the cascading of six 2nd order bandpass sections. Each 2nd order bandpass section exhibiting its own section centre frequency and Q, thus providing the overall bandpass response. To determine the required centre frequency and Q for each 2nd order section the pole locations of a 6th order normalised *low pass* Transitional Gaussian to 6dB was found [64]. The pole locations are :-

Real Part $(-\alpha)$	*Imaginary Part* $(\pm j\beta)$
0.5433	0.3431
0.4672	0.9991
0.2204	1.5067

By performing a low pass to bandpass transformation on the above normalised pole locations with the appropriate frequency scaling, a new set of pole locations are given that correspond to a 12th order *bandpass* Transitional Gaussian to 6dB with a Q of 6 centred at 60MHz [64]. The pole locations are:-

Real Part $(-\alpha)$	*Imaginary Part* $(\pm j\beta)$
17.615E6	387.569E6
16.631E6	365.944E6
15.951E6	409.507E6
13.498E6	346.531E6
7.814E6	427.393E6
6.078E6	332.422E6

From the above de-normalised pole locations representing a 12th order bandpass filter, the 2nd order coefficients of each section may be determined [30] from which their respective centre frequency and Q may be found. The 2nd order bandpass filter parameters are listed in Table 3.2.3-1.

Bandpass Section Number T	Centre Frequency Fo	Quality Factor Q	Complexity Fo*Q
1	61.747MHz	11.013	680.019MHz
2	58.302MHz	11.013	642.079MHz
3	65.224MHz	12.846	837.867MHz
4	55.194MHz	12.846	709.022MHz
5	68.033MHz	27.846	1.894GHz
6	52.915MHz	27.846	1.473GHz

Table 3.2.3-1 Required Q, Centre Frequency Fo, and Complexity FoQ, to realise the 60MHz IF Bandpass Filter

The 2nd order bandpass section (T), was simulated using an ideal 2nd order state variable loop shown by Fig 3.2.3-1a & b.

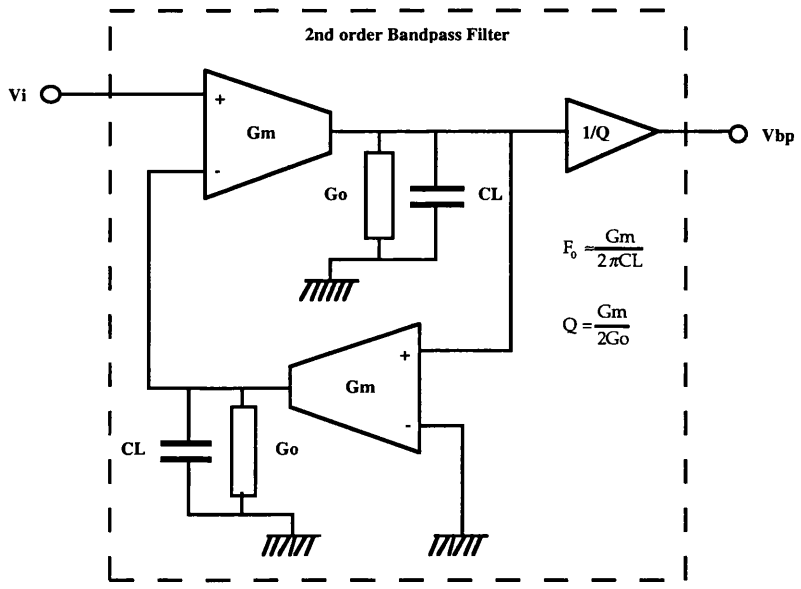


Fig 3.2.3-1a Ideal 2nd Order Bandpass Filter

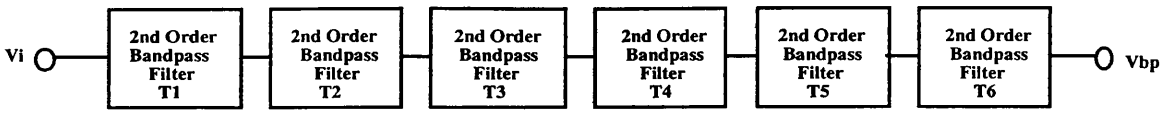


Fig 3.2.3-1b Cascaded 2nd Order bandpass Filter to Realise 60MHz Bandpass Transitional Gaussian to 6dB Response

The ideal 2nd order bandpass filter shown by Fig 3.2.3-1a is simply two integrators formed by transconductance amplifiers whose output is loaded by a capacitance C_L. The centre frequency is tuned by the variation of the transconductance gain Gm, while the Q is maintained by the variation of the output conductance Go. The output of the filter is attenuated by a factor of 1/Q, thus the peak signal for each bandpass section would be unity.

The amplitude and group delay response of each 2nd order filter and overall Transitional Gaussian response is shown by Fig 3.2.3-2a & b.

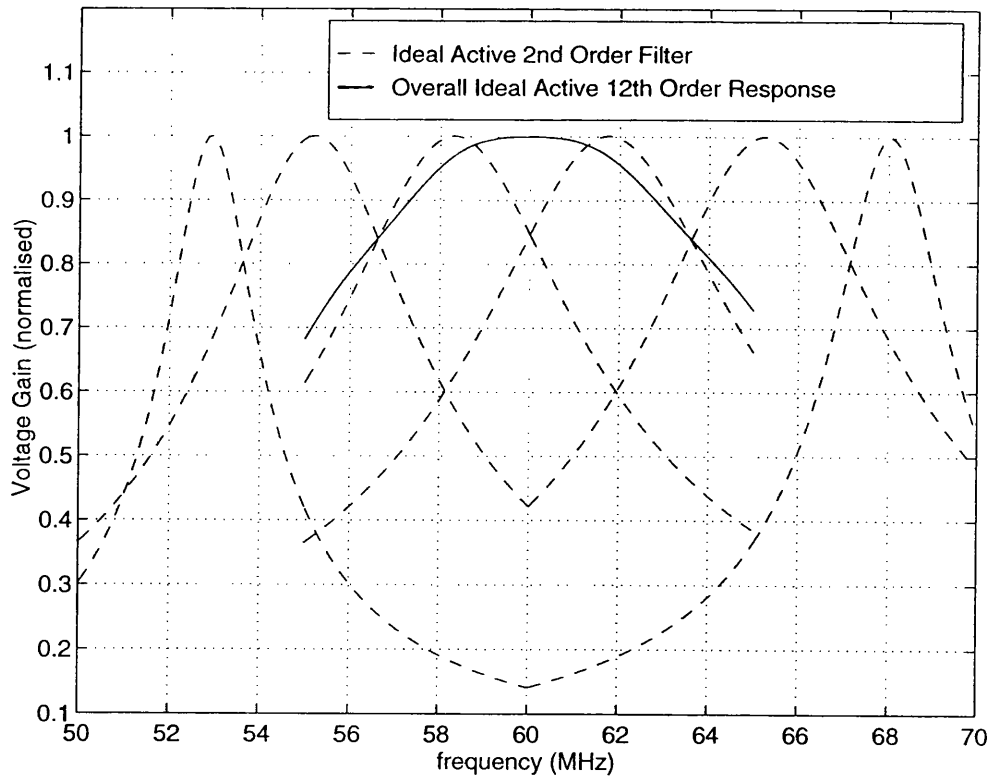


Fig 3.2.3-2a Amplitude Response of each 2nd order Filter and over all Response

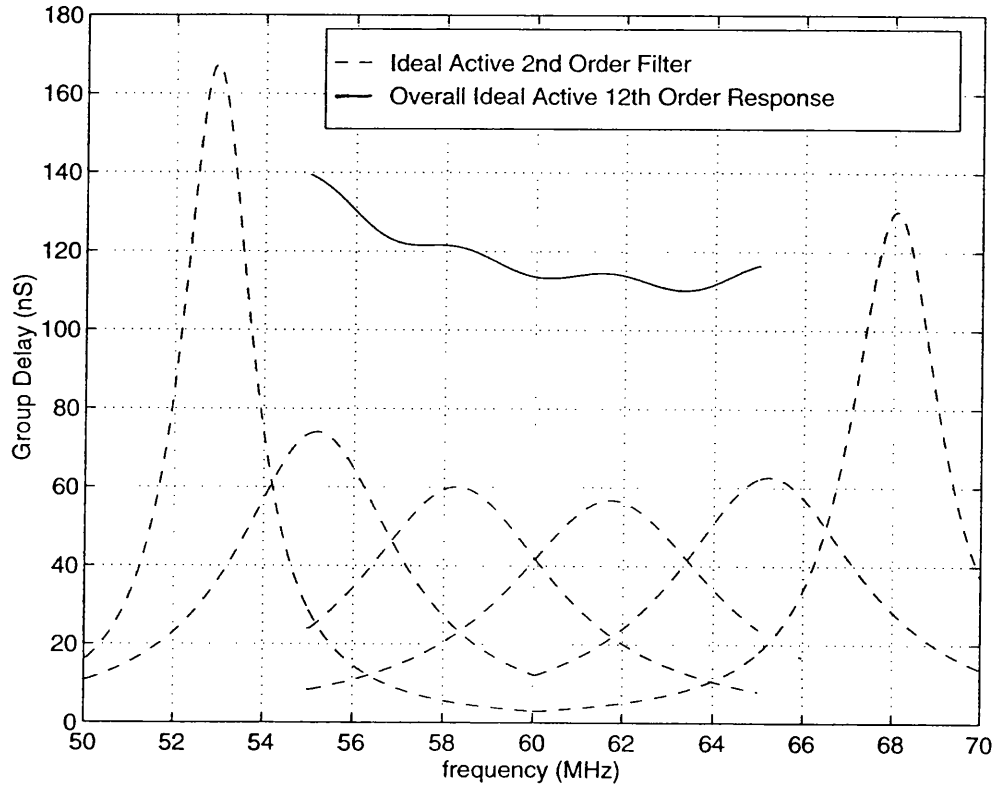


Fig 3.2.3-2b Group Delay Response of each 2nd order Filter and over all Response

As shown by Fig 3.2.3-2a, the four 2nd order filters, T1, 2, 3 & 4 form the greater part of the the Gaussian profile of the overall response. The two 2nd order filters closest to the centre frequency of 60MHz exhibit the lowest Q (11.044). As the 2nd order filter Qs increase, the further away there respective centre frequencies are in relation to the 60MHz centre frequency of the overall response, until the highest Qs (27.846) form the Chebyshev amplitude response for the out of band signals. This is as expected since a closer look at the group delay response shown by Fig 3.2.3-2b, shows that the lowest Q forms that part of the overall group delay profile that exhibits the lowest ripple, while the highest Q, as expected produces the out of band peak group delay.

3.3 Effects of non-ideal Transconductors on Transfer Function.

3.3.1 Amplitude Response

The transconductance amplifier used to form the two integrator loop shown by Fig 3.2.3-1a would be designed using transistors with finite *ft*, resulting in limited bandwidth. If this limited bandwidth were to be modelled by a single pole RC time constant for each transconductor, this would have the effect of transforming the *ideal* 2nd order bandpass filter to a *real* 4th order bandpass filter.

The effect of this limitation on the overall response of the 12th order bandpass filter, both in amplitude and group delay would be mathematically very complex, since the 12th order bandpass filter would be effectively transformed to give a 24th order response.

The effect of finite transconductor bandwidth was modelled by the circuit shown by Fig 3.3.1-1.

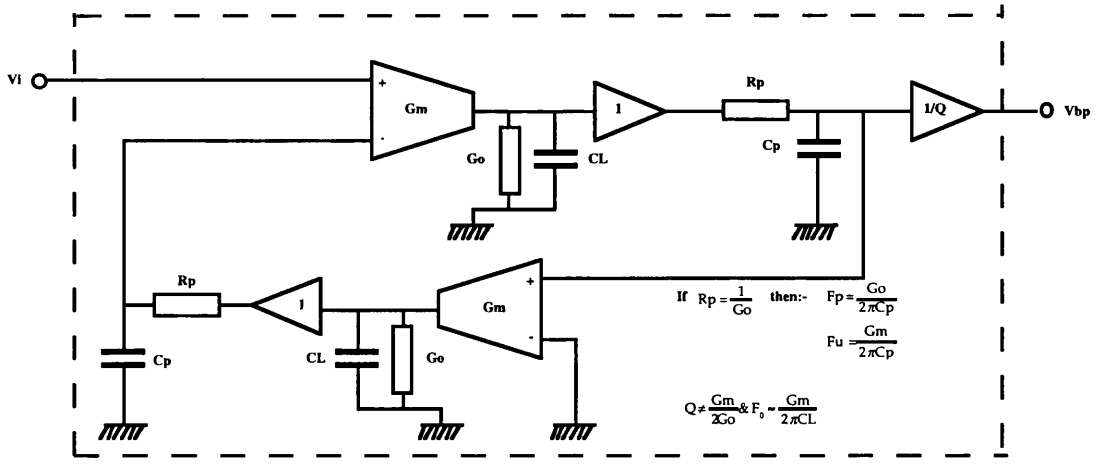


Fig 3.3.1-1 Non-ideal 2nd order bandpass filter

The non-ideal 2nd order bandpass filter shown by Fig 3.3.1-1 represents each transconductance amplifier with a parasitic pole located at $Fp=1/(2\pi CpRp)$. If the load capacitor C_L which provides the integration time constant were to be disconnected and the resistor Rp made equal to the reciprocal of the output conductance, Go, (ie $Rp=1/Go$) then the parasitic pole location would become $Fp=Go/(2\pi Cp)$. This represents the intrinsic 3dB bandwidth of the

open-circuited transconductance amplifier. In addition, the unity gain frequency, Fu of the transconductance amplifier would then be determined by $Fu=Gm/(2\pi Cp)$.

By holding the transconductance gain, Gm constant and setting a value of parasitic capacitance, Cp the unity gain may be set at a pre-determined frequency. In addition, by varying the output conductance, Go, (and also Rp accordingly) the Q of the bandpass filter may be adjusted to the appropriate value. Also, if the centre frequency requires adjustment, the load capacitance, C_L, (not Gm) may be varied accordingly.

By using this method to model the effect of finite transconductance amplifier bandwidth, *five* unity gain bandwidths, Fu of 15GHz, 10GHz, 5GHz, 1GHz and 500MHz were used. In each case of Fu, the centre frequency was adjusted for each 2nd order bandpass filter and the Q was adjusted until the gain of the bandpass response was unity, a method that would be used by an automatic tuning system [38]. For clarity the results of the simulation are shown by Fig 3.3.1-2a &b.

The amplitude responses shown by Figs 3.3.1-2a &b are normalised both in amplitude and frequency and represent the *best fit* in profile. The passive and ideal active realisation of the Transitional Gaussian are virtually identical. The effect of finite unity gain bandwidth becomes only noticeable from 5GHz and below. With lowering Fu, the IF bandpass filter has the effect of becoming more selective, since the presence of the parasitic poles are more noticeable at higher frequencies, but begins to depart from the profile of a Transitional Gaussian filter. This is particularly noticeable within the passband for Fu of 1GHz and 500MHz. The overall Transitional Gaussian profile remains within 1% accuracy with a Fu of 5GHz and above within a 10MHz bandwidth.

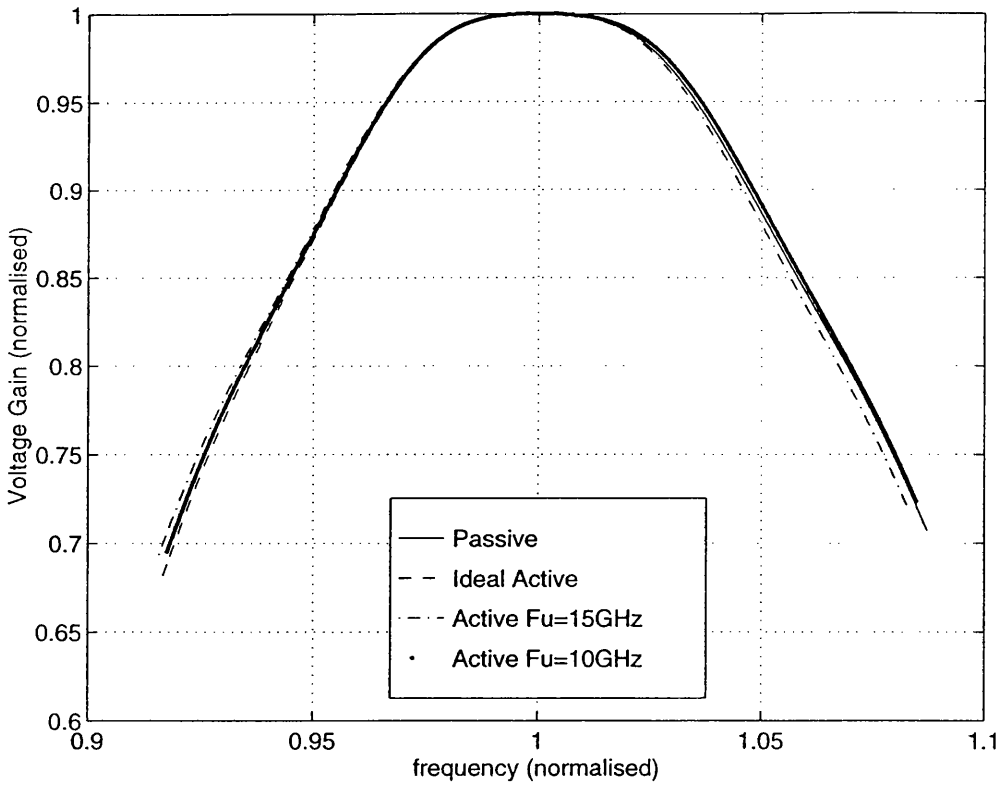


Fig 3.3.1-2a Normalised Amplitude Response of 60MHz Transitional Gaussian Filter with non-ideal Transconductance Amplifiers with Fu of infinity, 15GHz and 10GHz

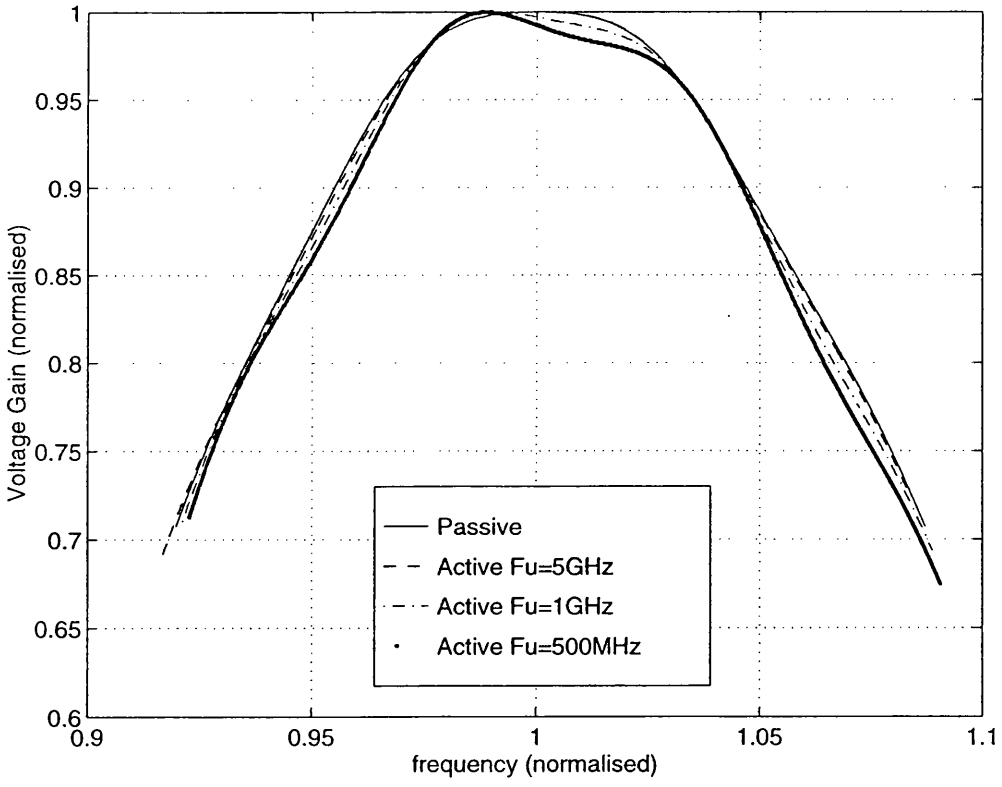


Fig 3.3.1-2b Normalised Amplitude Response of 60MHz Transitional Gaussian Filter with non-ideal Transconductance Amplifiers with Fu of 5GHz, 1GHz and 500MHz

3.3.2 Group Delay Response

The corresponding group delay responses for the *five* unity gain bandwidths, Fu of 15GHz, 10GHz, 5GHz, 1GHz and 500MHz were also simulated and compared as shown by Fig 3.3.2-1a &b.

The group delay responses shown by Fig 3.3.2-1a &b are normalised only in frequency, determined by the *best fit* in amplitude response profile. In addition, only the group delay ripple is shown by Fig 3.3.2-1a &b since any constant group delay offset as a result of finite unity gain bandwidth, Fu would be applied equally to the incoming signal frequency spectrum of the SSR pulse, with the effect of no distortion at the output. As a result, the offset of each group delay response was set to zero at 60MHz (the centre of the IF bandpass filter), allowing the effects of finite Fu to be observed more clearly.

As in the case of the amplitude responses, the effect of finite unity gain bandwidth becomes only noticeable from 5GHz and below. For the case of the 5GHz Fu, a maximum increase of ripple from the ideal (passive prototype) group delay reaches 1.34nS at 57MHz, although the error reduces to less than 1nS within a 6MHz bandwidth. For the cases of 1GHz, Fu and 500MHz, Fu the group delay responses clearly shows a more seveve deviation from the ideal within the pass band frequency range of 6MHz. A maximum increase in group delay ripple for the 1GHz, Fu is 1.83nS at 58.8MHz and 62.1MHz, while for the 500MHz, Fu the ripple increases to a maximum 3.6nS at 62.1MHz. It is clear that the effect of the finite unity gain bandwidth presents excess phase which results in a phenomenon called Q enhancement [44,65]. The effect is exaggerated if a form of peak detection is employed to determine the Q of the bandpass filter.

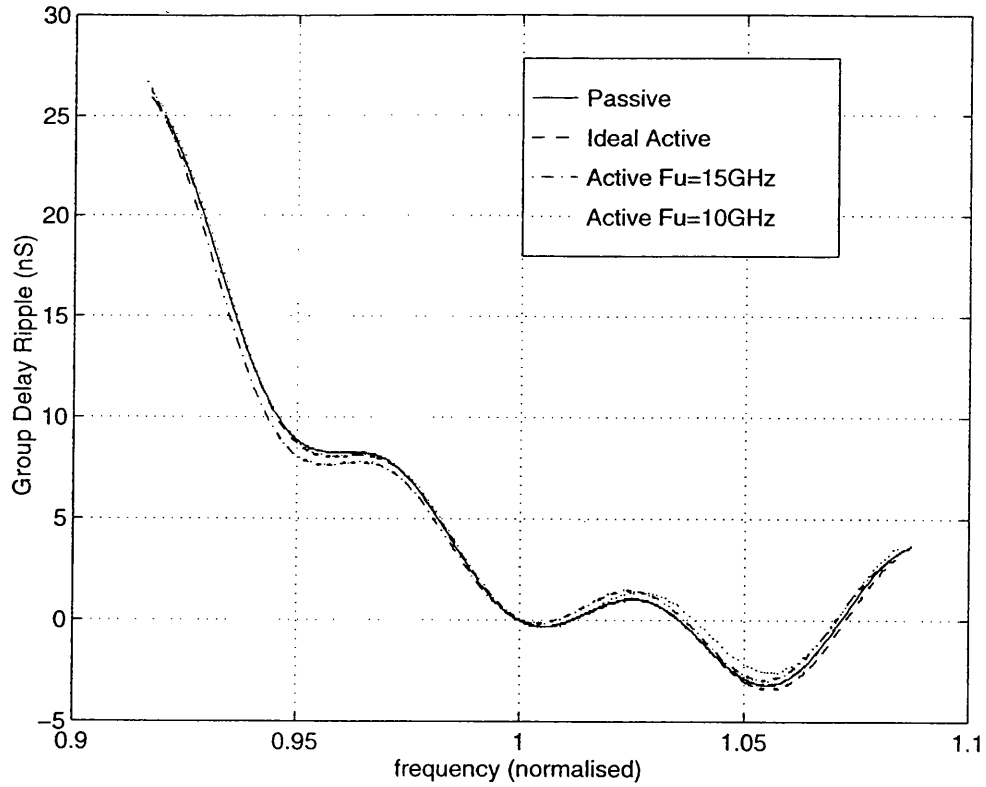


Fig 3.3.2-1a Group Delay Ripple Response of 60MHz Transitional Gaussian Filter with non-ideal Transconductance Amplifiers with Fu of infinity, 15GHz and 10GHz

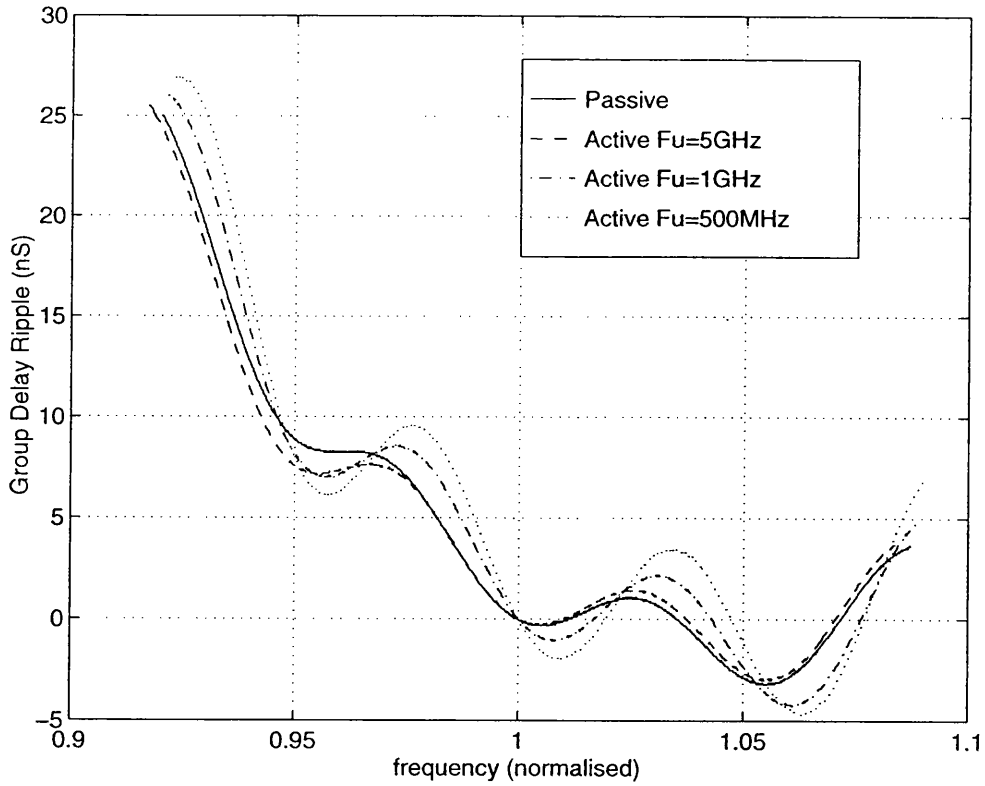


Fig 3.3.2-1b Group Delay Ripple Response of 60MHz Transitional Gaussian Filter with non-ideal Transconductance Amplifiers with Fu of 5GHz, 1GHz and 500MHz

3.3.3 Effects on Control Parameters

The use of the independent control of transconductance gain, Gm of the amplifier to vary the centre frequency, Fo and the output conductance, Go to control the Q is fundamental in the design of cascaded 2nd order sections, since this approach effectively offers transparent tuning as opposed to the tuning methods of an active ladder design [33,34,38].

However, as the finite bandwidth of the transconductance amplifier is lowered, the simple relationship between centre frequency and Q becomes more interactive, with the possible, undesirable effect of a less transparent tuning of each 2nd order bandpass section.

The effect of finite unity gain bandwidth, Fu on the transconductance amplifier DC gain (ie Gm/Go) is illustrated by Fig 3.3.3-1.

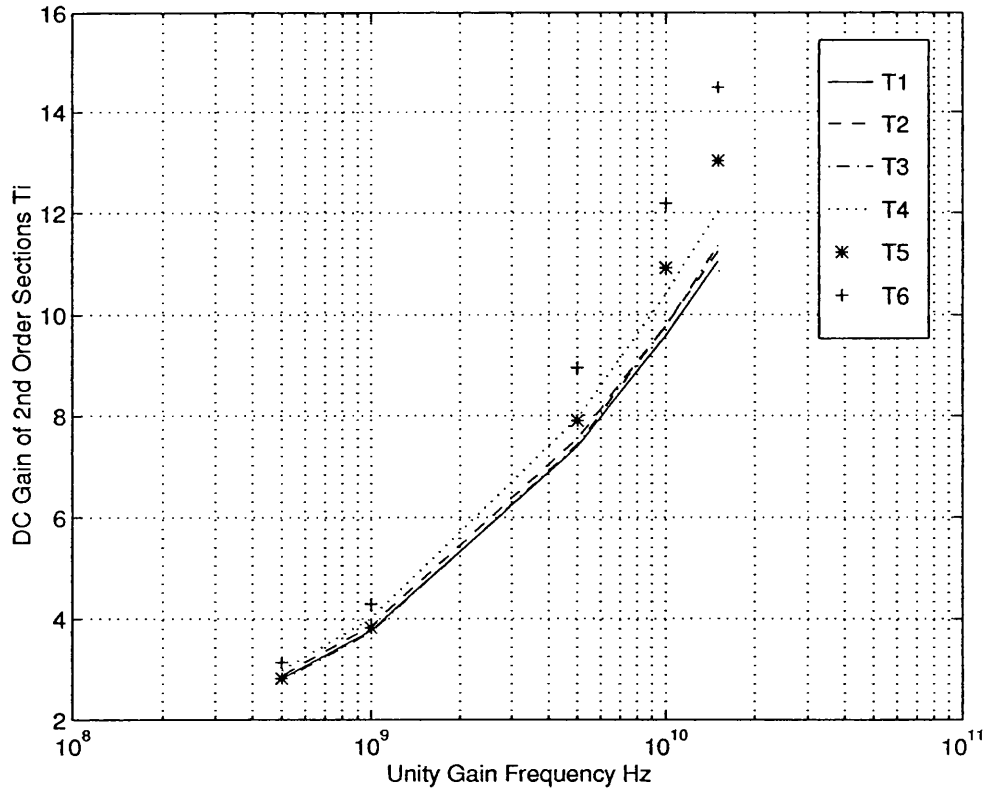


Fig 3.3.3-1 Transconductance Amplifier DC Gain (Gm/Go) with Finite Unity Gain Bandwidth, Fu

The variation of gain for each 2nd order bandpass filter with lowering unity gain bandwidth clearly shows that the DC gain of the transconductance amplifier has less effect in determining the Q value of the filter. With a unity gain frequency of 15GHz, the DC gains of each section are more varied, with the exception of the four filters with similar Qs (ie 11.013 to 12.846 for bandpass sections T1 to T4). The two bandpass filters with the highest Qs (ie for bandpass sections T5 and T6 with Qs of 27.846), exhibit differing DC gains. (13 and 15.5) which illustrates the presence of excess phase even at a unity gain frequency of 15GHz.

As the unity gain frequency is lowered, the transconductance amplifier DC gains are lower while still maintaining a given Q. Below a unity gain frequency of 1GHz the DC gains begin to converge to approximately a gain of 3 while the Q values of each 2nd order bandpass section vary between 11 and 28, illustrating that the Qs are predominantly determined by excess phase rather than the output conductance, Go. Taken to its logical conclusion, if the unity gain frequency is sufficiently lowered until the DC gains approach zero, the 2nd order bandpass filter would begin to oscillate.

Conversely, as the DC gains of the transconductance amplifiers are lower with lowering unity gain frequency, so the degree of Q enhancement increases.

Within the context of an automatic tuning systems, the value of Q would be determined by the voltage gain at the centre frequency of each bandpass section (T1 to T6). As illustrated by Fig 3.3.3-1 with lowering unity gain bandwidth of the OTA, results in excess phase, Q would no longer be determined by a simple relationship of DC gain (ie $Q \neq Gm/2Go$). As such, an error between Q measured by the centre frequency and its 3dB bandwidth and the peak value of voltage gain of the bandpass filter is the degree of Q enhancement. This Q enhancement, expressed as a percentage, is shown by Fig 3.3.3-2 with lowering unity gain bandwidth of the OTA.

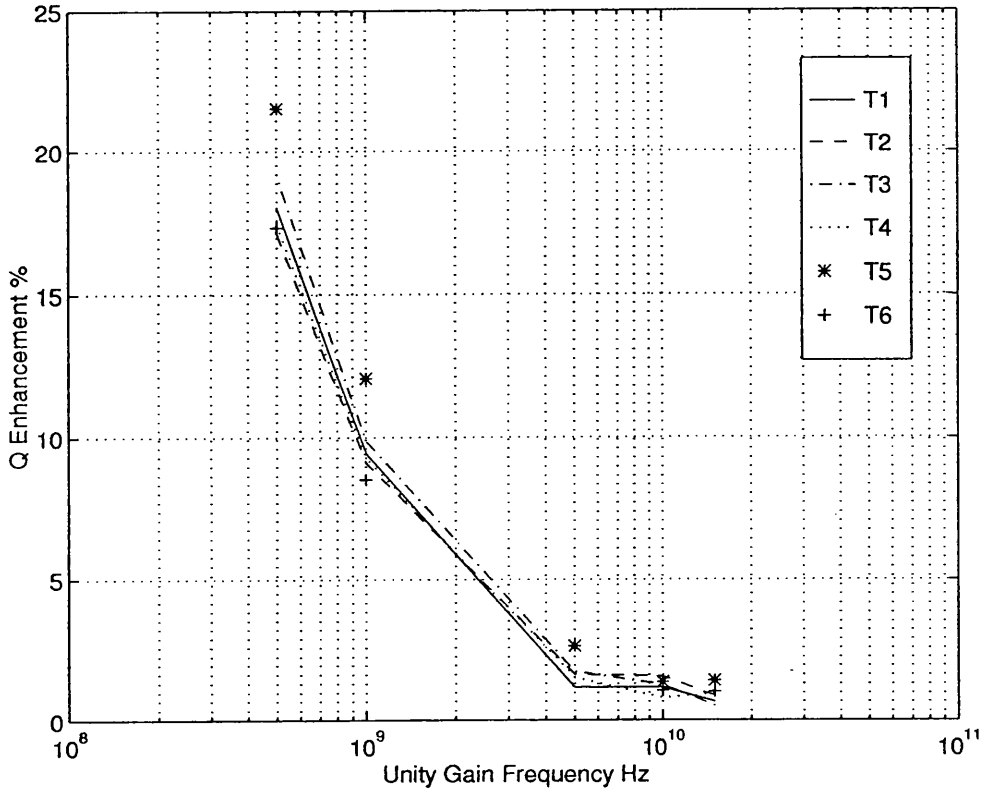


Fig 3.3.3-2 Q Enhancement with Finite Unity Gain Bandwidth, Fu

As in the case of the transconductance amplifier DC gains, the effect of finite unity gain bandwidth becomes only noticeable from 5GHz and below. At a unity gain frequency of 1GHz, the degree of Q enhancement is as high as 12% while at 5GHz, all the 2nd order bandpass filters Q are within 2.4%. If a Q enhancement of 1% and less is desirable, then a unity gain frequency of 7GHz and above would be required.

The realisation of the very demanding 12th order bandpass IF filter in the form of an integrated circuit must take into account the issues raised above. Since the profile of the filter is set to an internationally agreed standard, the accuracy both in amplitude and group delay are of paramount importance. In addition, the realisation of maintaining this high degree of filter profile in relation of the control parameters to facilitate automatic adaptive tuning seems to suggest that the unity gain bandwidth of the transconductance amplifiers must be at least 5GHz.

If a unity gain frequency of 5GHz of the transconductance amplifiers employed was taken as a design limit, the profile of the amplitude and group delay ripple of the IF bandpass filter are shown in Fig 3.3.3-3a & b.

3.4 Requirements of an Active 2nd order Tunable Filter

3.4.1 Frequency and Q tuning Range

The realisation of a high order filter using cascading 2nd order sections, requires the design of a suitable transconductance amplifier with the capability of independent control of the transconductance gain, Gm and output conductance, Go. By providing the control of these parameters a fully tunable 2nd order bandpass filter may be constructed and replicated six times to provide the overall transfer function profile as illustrated by Fig 3.2.3-1a & b. and Table 3.2.3-1.

As such, the suitable design of a transconductance amplifier with a minimum (unloaded C_L=0) unity gain frequency of 5GHz may be considered the fundamental building block. The transconductors would be configured as a bandpass filter as shown by Fig 3.2.3-1a with the capability of independent, accurate control of centre frequency and Q.

By examining Table 3.2.3-1 it is clear that the 2nd order bandpass section Q are required to vary between approximately 11 to 30. In addition, the centre frequency Fo must overcome the tolerance of a typical integrated capacitor of ±20% [35]. The 2nd order bandpass filters closest to the centre frequency of 60MHz of the 12th order IF bandpass filter must conform to the tightest transfer function accuracy, as these filters provide the lowest group delay ripple in the passband as illustrated by Fig 3.2.3-2b.
Therefore, if a 2nd order bandpass filter were to be designed with a Q variation of 11 to 30, this would demonstrate the capability of the bandpass filter to provide the required variation of Q for all six of the bandpass sections. In addition, if the centre frequency were capable of varying between 45MHz to 75MHz (centred at 60MHz) this represents a tuning range of

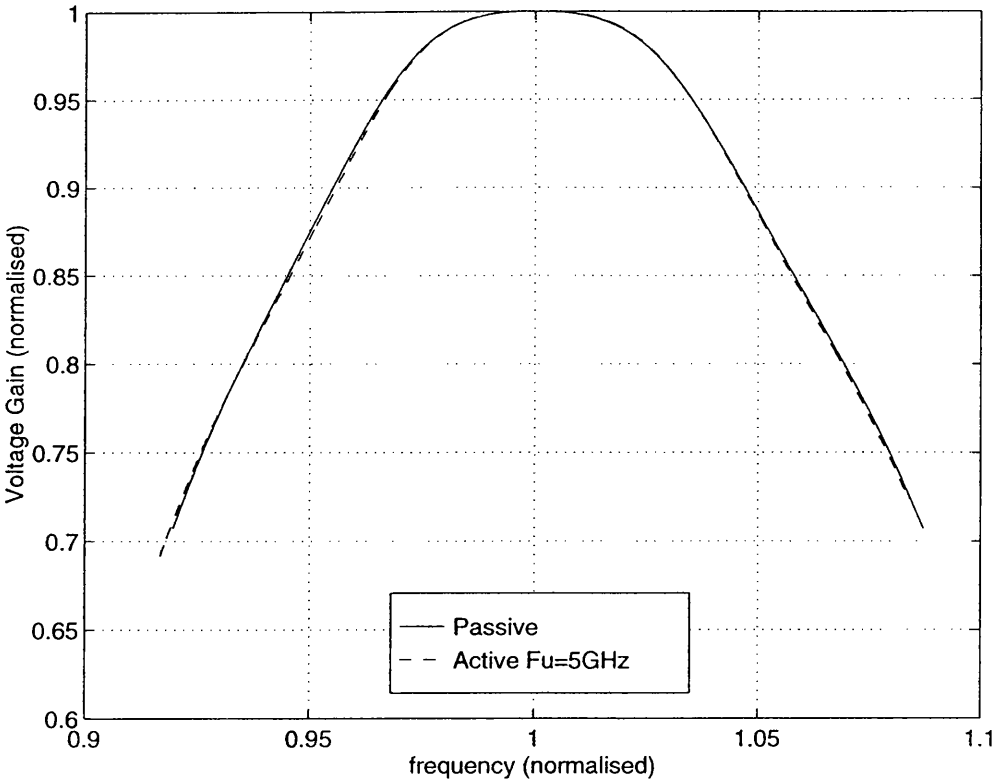


Fig 3.3.3-3a Normalised Amplitude Response of the 12th Order Bandpass Filter with Passive and Active Realisation with a Fu of 5GHz

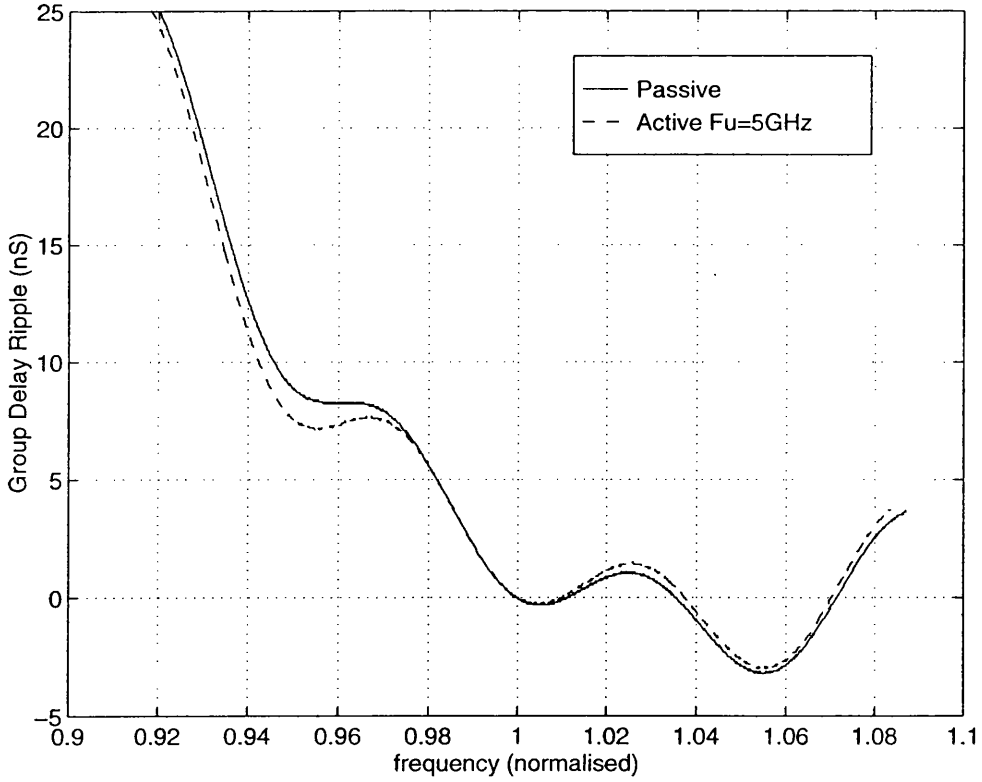


Fig 3.3.3-3b Group Delay Ripple Response of the 12th Order Bandpass Filter with Passive and Active Realisation with a Fu of 5GHz

±25%, capable of overcoming the tolerance of integrated capacitors and covering the range of centre frequencies required to realise the 12th order IF bandpass filter.

3.4.2 Transfer Function Accuracy

The accuracy of the transfer function of the overall 12th order bandpass IF filter is of central importance, as illustrated by the preceding sections. As a result the accuracy of each 2nd order bandpass filter both in transfer function and measured parameters such as section Q have a direct relation to the overall IF bandpass filter response.

It is thus very important to establish the degree of accuracy required by the 2nd order bandpass filters used for the 12th order bandpass IF filter. As illustrated by Fig 3.3.3-3a & b by using transconductor amplifiers with no less than a unity gain frequency, Fu of 5GHz, would provide a very accurate 12th order Transitional Gaussian to 6dB. As such, the amplitude and group delay responses of a 2nd order bandpass filter with a Fu of 5GHz is shown by Fig 3.4.2-1a & b.

As shown by Fig 3.4.2-1a, the amplitude response of the 2nd order bandpass filter which exhibits a unity gain frequency, Fu of 5GHz is very closly matched to that of an ideal response of a 2nd order amplitude transfer function. To compare the difference more closly, the error between the two amplitude responses are shown by Fig 3.4.2-1a. As shown by Fig 3.4.2-2a the largest error of 2.2% occurs at the extremes of frequency.

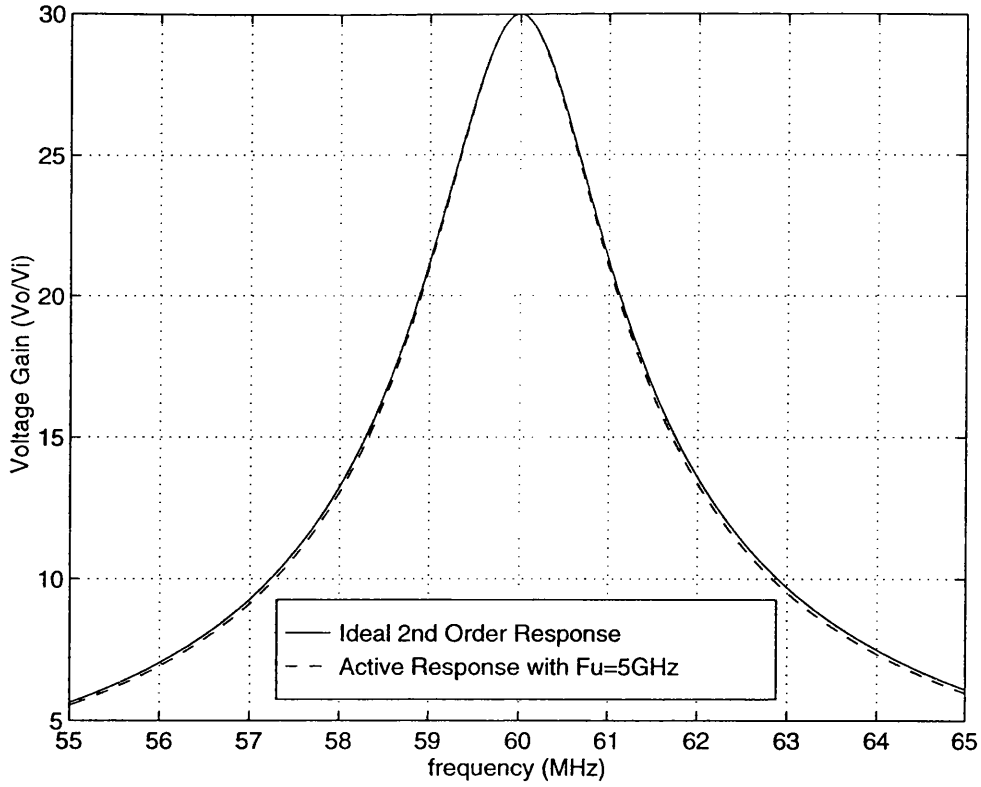


Fig 3.4.2-1a Amplitude Response of 2nd order Bandpass Filter with a Q of 30

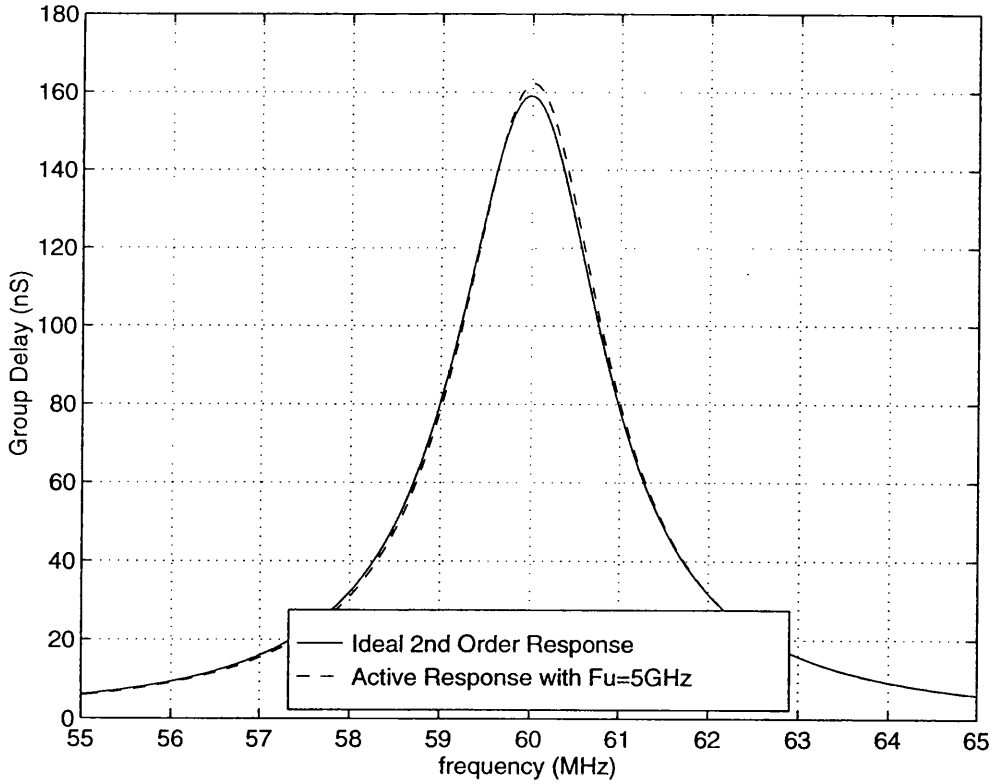


Fig 3.4.2-1b Group Delay Response of 2nd order Bandpass Filter with a Q of 30

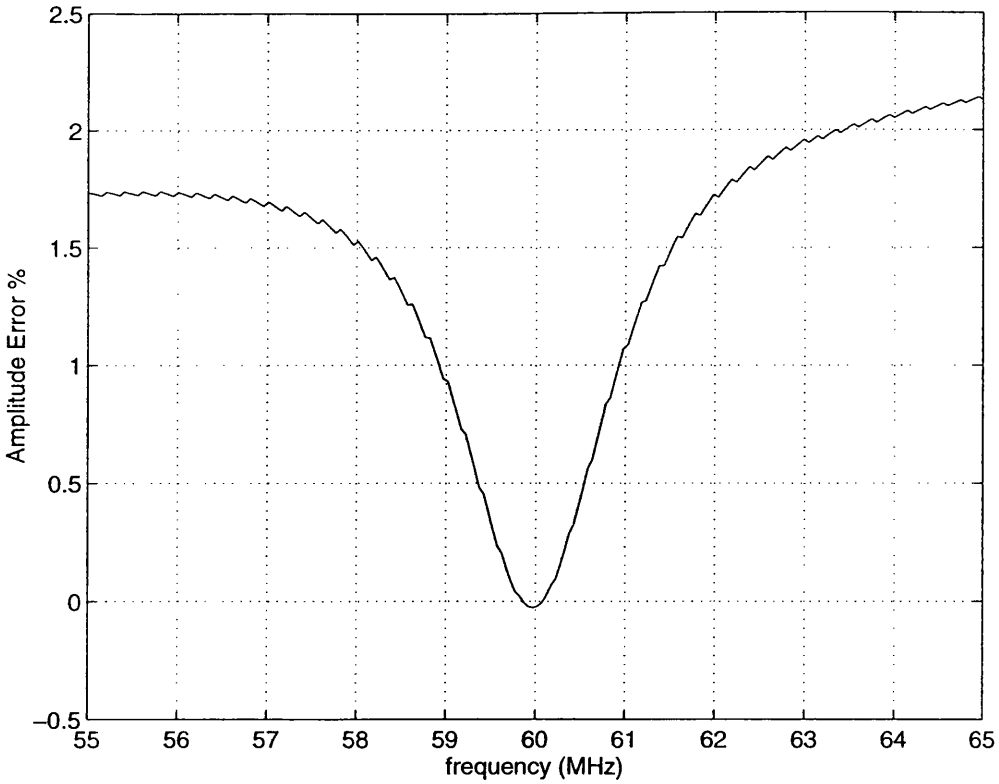


Fig 3.4.2-2a Error in Amplitude Response Compared to the Ideal

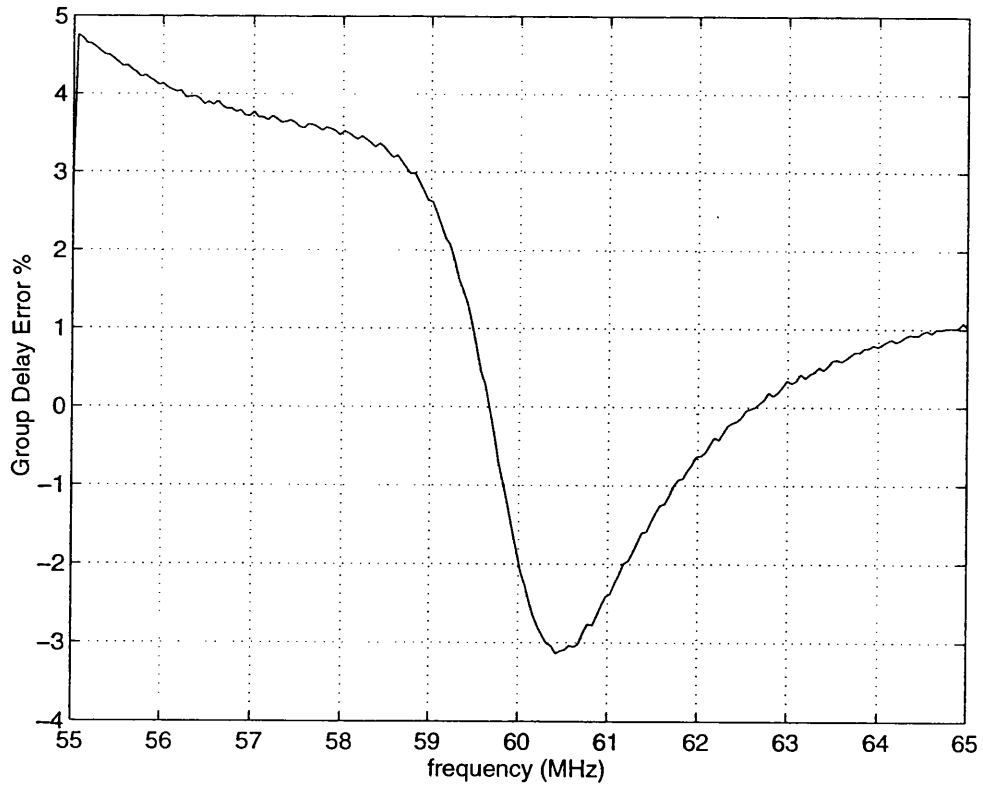


Fig 3.4.2-2b Error in Group Delay Response Compared to the Ideal

Conversely the group delay responses are shown by Fig 3.4.2-1b and a greater deviation from the ideal is apparent, exhibiting a maximum in group delay error of 4.7% compared to the ideal response and an error of -2% at 60MHz. This is not only due to excess phase shifts but also to the finite DC gain (ie Gm/Go) of the transconductance amplifier resulting in phase lead from the ideal.

To maintain the overall accuracy of the 12th order bandpass IF filter, the automatic adaptive tuning system would rely on measurements of the centre frequency by the application of a suitable input reference signal [38], while 2nd order bandpass Q would be determined by measurement of peak gain [38]. If excess phase is kept to a minimum (ie Fu ≥ 5GHz) independent control would be achieved and accurate transfer function, both in amplitude and group delay, maintained.

3.5 Conclusion

In this chapter the issues relating to the realisation of a 12th order bandpass Transitional Gaussian to 6dB filter have been investigated.

By using the method of cascading six sections of 2nd order bandpass filters to provide the overall bandpass IF response, each filter Q and centre frequency, Fo was determined. In addition the bandpass filter section complexity (FoQ) was also determined, the maximum being at 1.9GHz.

The effects of finite transconductance amplifier bandwidth was also investigated, with particular regard to the 12th order IF bandpass transfer function accuracy, in amplitude and group delay. To maintain an overall accuracy to within 1% in the amplitude response and not to increase the group delay ripple by 2nS within a passband of 6MHz, a unity gain frequency of 1 to 5GHz for the transconductance amplifier is required.

In addition, the effect of Q enhancement was also investigated in relation to

the finite transconductance amplifier bandwidth. To limit the degree of Q enhancement to within 1%, the transconductance amplifier unity gain bandwidth is required to be at 7GHz or above, increasing to a Q enhancement 2.6% at a unity gain bandwidth of 5GHz. An Fu of 5GHz is taken as the design requirement.
A fully tunable 2nd order bandpass filter capable of independent control of Q and centre frequency is required. The centre frequency tuning range is required to vary between 45MHz to 75MHz (centred at 60MHz) and Q should vary between 11 to 30, while maintaining an amplitude accuracy to within 2% at 60MHz.

The severe requirements of the 12th order bandpass IF filter, and the long term objective of the total integration of the transponder RF front end indicates that a high bandwidth technology would be best served to investigate the realisation of such a filter. The technology available for this program was an experimental low threshold GaAs MESFET process.

CHAPTER 4

GaAs MESFET Technology

4.1 Introduction

The technology employed in this programme was an experimental 0.5μm gate length, -1V threshold, 20GHz *ft* GaAs MESFET process provided by GEC-Marconi Materials Technology (Caswell) Ltd [66]. This process is characterised for device widths from 20μm to 300μm and the characterisation studies were carried out at Bradford University [67].

The use of a device model to predict the performance of the complete circuit is of great importance in IC design. In general, the greater the accuracy of the model, the closer the simulated performance of the circuit approaches measured results. In this chapter, the difficulties of modelling the measured characteristics of GaAs MESFETs are reviewed. It is emphasised that the choice of device model must take into account the observed variations of the MESFET parameters across foundry runs and the restrictions imposed by the use of a circuit simulator with fixed model equations (eg. SPICE).

This chapter is not intended to provide a comprehensive critical review of the many GaAs MESFET models published in the literature, rather to arrive at a strategy which enables limited modelling data to be used to best advantage.

4.2 The Physics of Gallium Arsenide : a summary

Throughout the semiconductor and electronics industry the dominant semiconductor material is silicon (Si) due to its abundant supply and low cost of manufacture. The success of Si is often attributed to two main characteristics, firstly, its high bandgap of 1.12eV which permits Si to operate over a wide temperature range giving good thermal stability, and secondly Si forms a natural oxide which is one of the best insulators known. This oxide grows from the bulk of the material which provides improved stability. This planar technology quickly led to integrated circuits (IC) and the electronics revolution.

As a semiconductor, gallium arsenide (GaAs) has one of the characteristics that proved so important to the rapid development of Si technology, which is a wider bandgap of 1.42eV. This larger bandgap allowed GaAs to operate over a wider temperature compared to Si, a feature especially important to the military and as such displays a much lower intrinsic carrier concentration at room temperature (the number of carriers which will have sufficient thermal energy to occupy the conduction band) - 1.79×10^6 cm^{-3} for GaAs compared to 1.45×10^{10} cm^{-3} for Si. As a result, GaAs exhibits a much lower intrinsic conductivity compared to Si, forming a *semi-insulating*, rather than *semi-conducting*, substrate. The low intrinsic carrier concentration also means that the parasitic capacitance such as gate-drain, gate-source and source-substrate is much less than for Si. Parasitic capacitance being the major factor limiting the speed of the devices and hence circuits.

The main attraction of GaAs however is the very high, low-field electron mobility (8500 cm^2/V-s in *n*-type GaAs compared to 1500 cm^2/V-s in *n*-type Si) which sets an upper limit on the speed of devices. From these figures it appears that GaAs is about five times 'faster' than silicon, but is actually an over simplification which will be considered shortly. In a semiconductor there are two principle carrier types, electrons, which are the majority carriers in *n*-type semiconductors, and holes, which are the majority carriers in *p*-type semiconductors. In a given semiconductor, the holes have a greater effective mass than the electrons, which implies that the *p*-type devices will operate more slowly than *n*-type devices. The peak carrier mobilities of Si and GaAs are shown in Table 4.2-1. For this reason comparable *p*-type devices are not generally available with high-speed IC processes such as Si bipolar and GaAs. This can cause serious problems for circuit designers who are restricted to *n*-type devices only.

Material	Electron mobility $cm^2/V\text{-}s$	Hole mobility $cm^2/V\text{-}s$
Si	1500	450
GaAs	8500	400

Table 4.2-1 Carrier Mobilities in Si and GaAs

The physical properties and bandgap structure of GaAs is comprehensively documented in the literature [68-70] of which the variation of the electron drift velocity with electric field is shown by Fig 4.2-1.

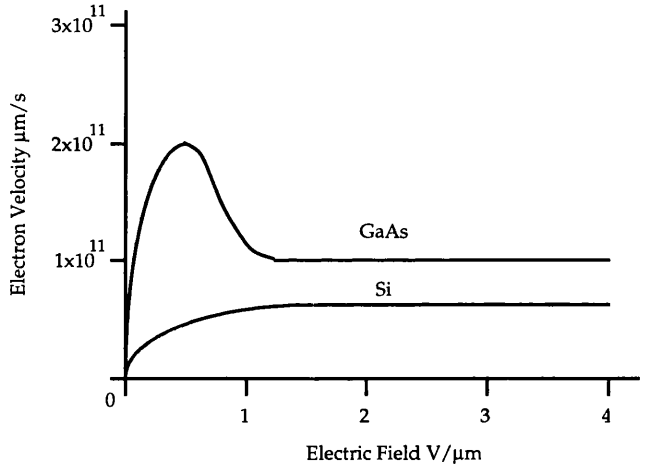


Fig 4.2-1 Drift Velocity in Si and GaAs

From Fig 4.2-1 clearly illustrates both the origin of the five times 'faster' claim and the reason why it is unlikely to be realised in actual circuits. In a sample of GaAs most of the electrons will be of low effective mass (and therefore high mobility) below a critical field of approximatly 0.3V/µm. Above this field electrons are excited into an upper bandgap valley [69] and therefore become high effective mass, low mobility. The importance of this is clear when one considers that a typical GaAs gate length is 1µm. If the voltage across the device is 1V, then the field will be approximately 1V/µm, thus higher than the critical field for maximum mobility. At high fields the electron drift velocity in GaAs tends to a value of about 1.4 times faster than

silicon. This is the main reason why GaAs is not 'five times faster' than Si. Although the electron mobility is a limiting factor, the speed of the device is also affected by the parasitic capacitance. The semi-insulating substrate exhibited by GaAs has a very low parasitic capacitance which results in devices with very high *f*ts.

4.3 Modelling : Problems & Restrictions

4.3.1 The GaAs MESFET

A wide range of GaAs devices have emerged, including the junction field effect transistor (JFET), metal insulator semiconductor field effect transistor (MISFET), high electron mobility transistor (HEMT), heterojuction bipolar transistor (HBT) and the metal semiconductor field effect transistor (MESFET) [68,69]. Of these technologies the only devices in widespread commercial use at present is the depletion mode MESFET (D-MESFET) and the high electron mobility transistor (HEMT). Some foundries also produce an enhancement mode MESFET (E-MESFET), but these devices are more difficult to fabricate and tend to find more widespread use in digital, rather than analogue circuits [71]. A schematic of a typical D-MESFET is shown by Fig 4.3.1-1.

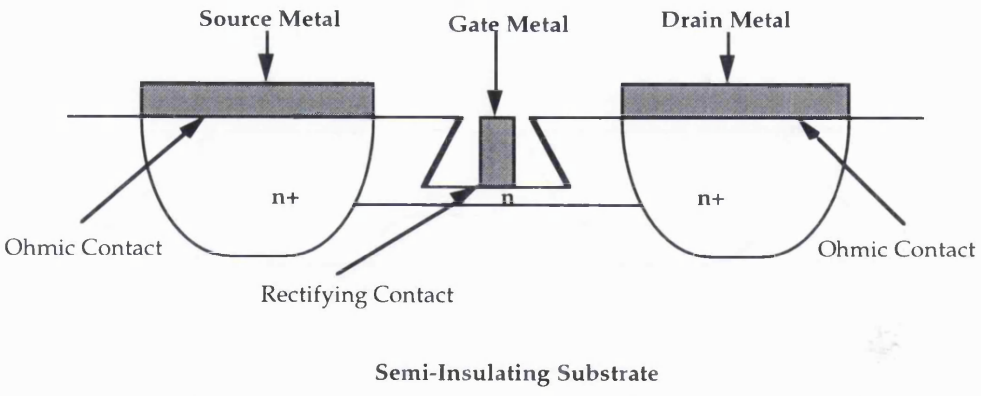


Fig 4.3.1-1 Schematic of a Typical D-MESFET

As shown by Fig 4.3.1-1 a cross section of a typical D-MESFET consists of an n-type implanted region in a semi-insulating substrate. The channel region depth is generally defined by an etching step for maximum control of this dimension. The gate metal and source/drain metal are different since the

latter provides an ohmic contact to the device, as opposed to the gate which forms a rectifying junction. The whole structure is covered with a silicon nitride or polyimide dielectric insulator, on top of which runs the second level interconnect metal. GaAs processes typically differ in the material growth/deposition techniques such as epitaxial growth, ion implantation [69] and in the methods used to define device geometry such as self-aligned gate or electron beam lithography [69].

When attempting to describe the device operation it is helpful to categorise them according to channel length. A long-channel device is far easier to describe than a short-channel device since it is possible to make a number of simplifying assumptions about their operation.

An idealised MESFET structure as shown by Fig 4.3.1-1 is fairly simple and in terms of operation it is very similar to the JFET. With the gate shorted to the source, the voltage drop down the channel caused by current flow from the drain to source causes an increase in the reverse bias of the gate-channel junction as one proceeds from source to drain. This causes the depletion layer to extend further into the channel at the drain end. The neck through which the current flows will be narrowest at the drain and will narrow further as the current is increased. This mechanism imposes a limit on the current that can flow in the channel, since too high a current would *pinch-off* the channel, stopping further current flow. An equilibrium is reached which is termed saturation. The device is normally operated in the saturation region. A straightforward analysis of the device for modelling purposes is based on the following assumptions:-

(1) Uniform doping distribution in channel
(2) Validity of the gradual channel approximation
(3) Constant carrier mobility
(4) Abrupt depletion layer

It will be shown in the following sections that the assumptions made above to describe the MESFET operation have to be discarded once the device

channel length is scaled down and the chosen device model is modified accordingly.

4.3.2 The DC Models

Modelling of MESFETs is a complex issue and detailed accounts can be found in the literature [72-77]. In a practical situation these sophisticated models often have little relevance, as the circuit designer is often restricted to the models which can be used with a circuit simulator with pre-set models. For the simulation carried out for this project, the SPICE circuit simulator was used which provides two models suitable for MESFET simulation.

The simplest model is the Shichman-Hodges model [78], which was developed in 1968 for the simulation of insulated gate field effect transistor (FETs). This model separates the FET operation into three regions - *cut off* defined by equation (4.3.2.1), the *triode* region (sometimes referred to as the linear region) defined by equation (4.3.2.2) and the *saturated* region which assumes quadratic FET behaviour defined by equation (4.3.2.3).

$$Id = 0 \qquad \text{cut-off } (V_{gs} \le Vto) \qquad (4.3.2.1)$$

$$Id = \beta\left[2(V_{gs} - Vto)V_{ds} - V_{ds}^2\right](1 + \lambda V_{ds}) \qquad \text{triode region} \qquad (4.3.2.2)$$

$$Id = \beta(V_{gs} - Vto)^2(1 + \lambda V_{ds}) \qquad \text{saturated region } (V_{gs} \ge V_{gs} - Vto) \qquad (4.3.2.3)$$

Where Id = drain current, V_{gs} = gate-source voltage, V_{ds} = drain-source voltage, Vto = threshold voltage, β = device gain A/V^2 and λ = 1/(early voltage) 1/V. The Id vs V_{ds} FET characteristics governed by the Shichman-Hodges model is shown by Fig 4.3.2-1

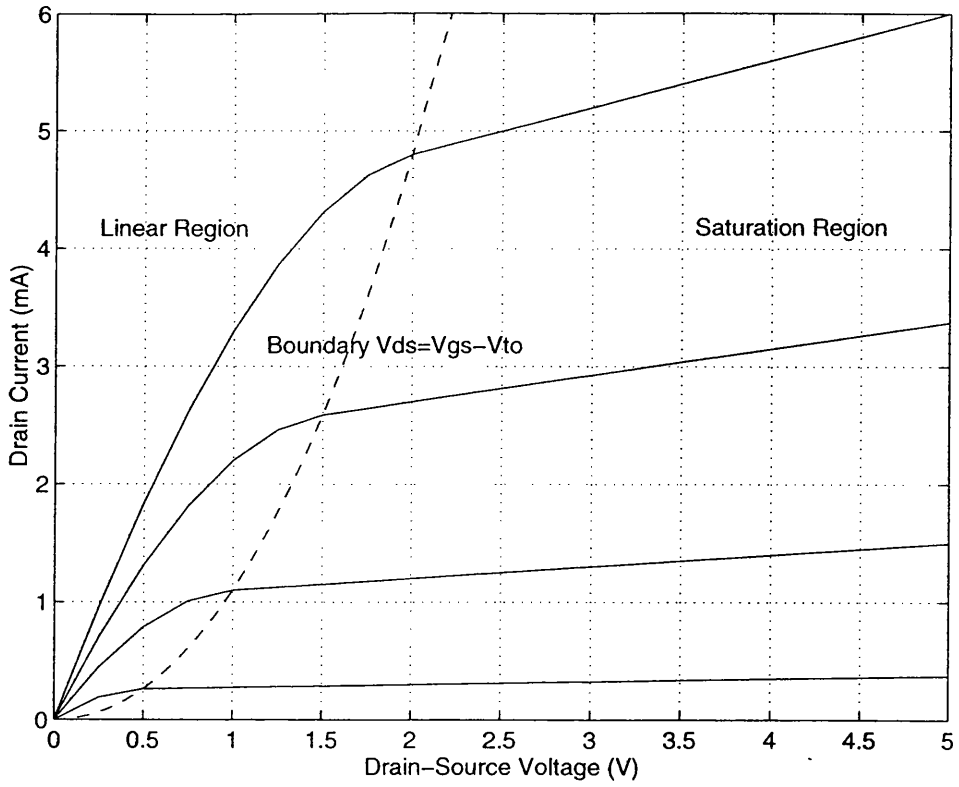


Fig 4.3.2-1 Shichman-Hodges Model of FET Characteristics
($\beta = 1mA/V^2$, $\lambda = 0.1V^{-1}$, Vto = -2V)

This model is useful due to its simplicity, but when compared to the measured MESFET data it is often found to be inaccurate, the most pronounced departure occurring between the transition of the triode region to the saturated region. An effect commonly observed in GaAs MESFET is that the 'knee' of the Id-V_{ds} curve appears at a lower V_{ds} than predicted by the Shichman-Hodges (S-H) model and the onset of saturation occurs at a constant V_{ds} rather than along a quadratic curve indicated by the boundary line in Fig 4.3.2-1. This effect is caused by electron velocity saturation and is known as the *early saturation* effect [79]. In Fig 4.2-1, electron velocity is shown to reach a high-field maximum value when an electric field of approximately 1V/μm is applied, thus increasing the field further will not increase the current flow.

A more sophisticated model which can also be used with SPICE is the Curtice model [80]. This replaces the Shichman-Hodges equations with a single expression adding a hyperbolic tangent to adjust the saturation point

shown by equation (4.3.2.4)

$$Id = \beta(V_{gs} - Vto)^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \qquad (4.3.2.4)$$

Where α is a device constant.

An unusual characteristic of the GEC-Marconi, low threshold MESFETs is the absence of any significant early saturation. Since circuit designers have chosen to exploit the early saturation effect in GaAs [81] which has been successful in some circumstances, the data provided by Bradford University and supported by the literature indicates that it can not be used as a general circuit design method [82]. In particular devices with a low Vto such as these, generally saturate at $V_{ds} = V_{gs}$ - Vto [82]. This can be best illustrated by Fig 4.3.2-2, which shows the Id vs V_{ds} of the measured data for a 20μm GaAs MESFET along with a best fit Shichman-Hodges and Curtice models.

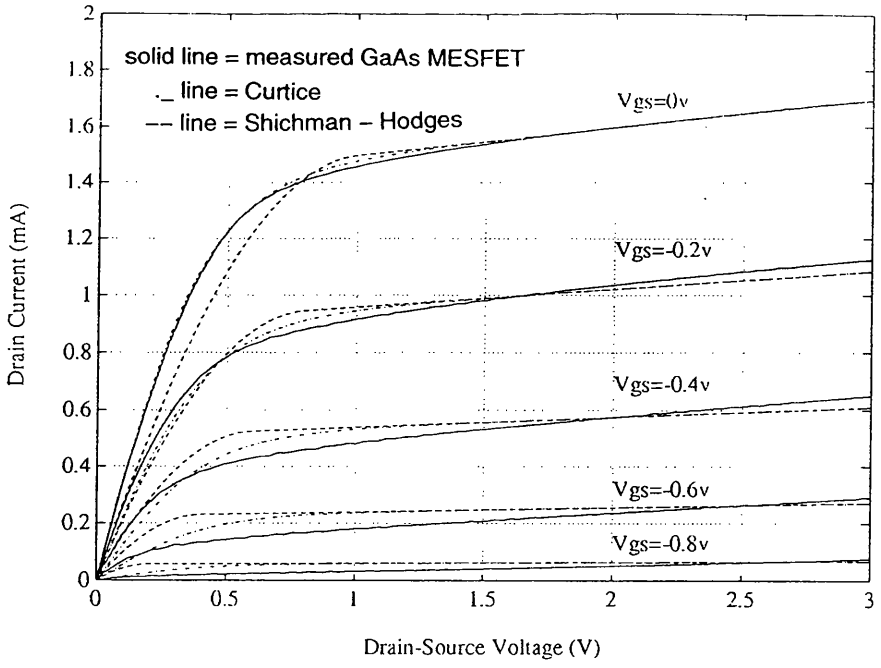


Fig 4.3.2-2 Measured Characteristic of the GEC-Marconi 20μm GaAs MESFET with Shichman-Hodges and Curtice models

The similarity between the measured data and the Curtice model is clearly shown to be the closest at low values of V_{gs} (ie close to Id = Idss), while accuracy is reduced as the GaAs MESFET approaches the threshold voltage. In addition, if the MESFETs are operating in saturation only, this enables the use of the Shichman-Hodges model, since in the saturated region of operation the Shichman-Hodges and the Curtice model converge.

For this reason the circuit design is restricted to operate well into the saturated region, with V_{ds} = 2.5V where the MESFET behaviour is more predictable and allows the use of a public domain simulator such as SPICE.

4.3.3 MESFET Geometry

For the realisation of an integrated continuous time filter, small size and low power dissipation are important considerations. As such, the smaller the MESFET devices available for the circuit design, the lower the power consumption of the filter. Although modelling data was provided for MESFET geometry up to 300μm, the minimum size device is considered the more promising candidate for use.

The MESFET modelling parameters for the 20μm and 40μm gate widths were supplied for a single wafer and between separate foundry runs. The results are shown on Tables 4.3.3-1a & b.

Device Size	β	Vto	λ	α
20μm	26%	11%	19%	16%
40μm	13%	11%	63%	28%

Table 4.3.3-1a Maximum Variation of MESFET Parameters Across a Single Wafer

Device Size	β	Vto	λ	α
20μm	26%	15%	54%	24%
40μm	16%	17%	67%	32%

Table 4.3.3-1b Maximum Variation of MESFET Parameters Across Four Foundry Runs

It is clear from this data that the MESFET characteristics can show significant variation across a single wafer and an even larger variation between separate foundry runs. Data was also provided for devices with gate widths of up to 300μm and these all show a similar range of variation.

As a result of these large parameter variations it is clear that to ensure device characteristic scaling in proportion to the device size is impractical. If a variety of device geometry were used in the circuit design, which is often the case [83], particularly so in CMOS, the parameter variation may cause non-optimum DC operating conditions. Thus, in addition to the use of the Shichman-Hodges model, a further restriction is to use a single geometry device throughout the design. As such, the minimum size MESFET was chosen.

From the data provided, a Shichman-Hodges model [78] for a 20μm MESFET device was determined with high - low parameter values, based on meaured tolerances, shown by Fig 4.3.3-1.

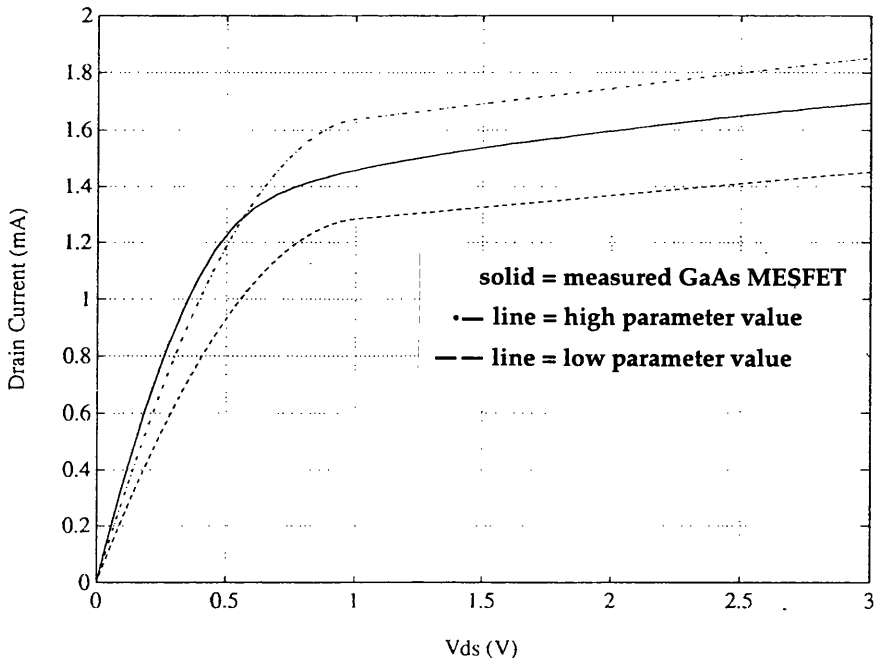


Fig 4.3.3-1 Simulated Id - V_{ds} Characteristics for a 20μm MESFET (Model Parameters derived from Measured Data)

In must be stressed however, that the parameter variation observed may be attributed to the development of this experimental low threshold process and as such, commercially available GaAs MESFET devices may not exhibit such a wide variation.

4.3.4 The AC Small Signal Model

Once the DC operating conditions and device geometry are fixed, the small signal model for the 20μm MESFET is simplified. As is the case of the DC model restriction imposed as a result of using the SPICE simulator, only the predominant AC parameters are chosen to represent the small signal operation of the device.

When analysing MESFET (or any FET) circuit it is useful to define the *transconductance, gm* and the *output conductance, go.* These parameters are derived from the saturated region equation (4.3.2.3) of the Shichman-

Hodges model and can be defined as:

$$g_m = \left(\frac{\partial Id}{\partial V_{gs}}\right)_{V_{ds}} = 2\beta(V_{gs} - Vto)(1 + \lambda V_{ds}) \qquad (4.3.4.1)$$

$$g_o = \left(\frac{\partial Id}{\partial V_{ds}}\right)_{V_{gs}} = \lambda\beta(V_{gs} - Vto)^2 \qquad (4.3.4.2)$$

As shown by equations (4.3.4-2) and (4.3.4-2), both the value of g_m and g_o are determined by the DC operating conditions, V_{ds} and V_{gs}, therefore at a given operating point a small signal description of the MESFET is given by equation (4.3.4.3).

$$id = g_m v_{gs} + g_o v_{ds} \qquad (4.3.4.3)$$

Due to the DC modelling restriction discussed in section 4.3.2, the MESFET was chosen to operate well into saturation with V_{ds} = 2V5, thus to accommodate g_m tuning, V_{gs} must be varied. However, the use of active loads in GaAs MESFET technology is widespread and is often achieved by the use of a single MESFET current load [84,85], with V_{gs} set to zero. If g_m tuning was implemented by varying V_{gs}, resulting in varying DC bias currents, large DC voltage offsets would occur within the circuit. This in turn would alter the DC condition imposed to maintain the devices in saturation. Therefore a further restriction is imposed upon the circuit design, that all MESFET devices operate at V_{gs} = 0 that is, Id = Idss. In addition, an advantage of this restriction is shown by Fig 4.3.2-3 that the Shichman-Hodges model is the closest match to the measured MESFET data at V_{gs} = 0. Due to the severe design restrictions, g_m tuning can only be achieved by breaking the design requirements, by biasing the MESFETs in the triode region to act as variable resistors.

As a result of the maximum variation of MESFET parameters shown by Fig 4.3.3-1, the corresponding variation in g_m would also be large. For the intended application, the bandpass filter centre frequency would be

dependant upon the OTA-C integrator Gm/C_L. Although Gm is required to vary as a result of the tolerance of the fabricated load capacitance C_L, the maximum upper centre frequency would depend upon the MESFET device g_m, since this value would be reduced for tuning. As such, to ensure that a minimum centre frequency of 60MHz (Chapter 3, section 3.4) is obtained, the lower limits of the simulated GaAs MESFET parameters were chosen for the circuit design.

An unusual property of the GEC-Marconi, low threshold MESFET is that the output conductance, g_o of the devices is significant. The intrinsic gain, g_m/g_o shown by equation (4.3.4-4), derived from equations (4.3.4.1 &2) is dependant upon the reciprocal of the early voltage, λ and the bias conditions of the MESFET.

$$\frac{g_m}{g_o} = \frac{2(1+\lambda V_{ds})}{\lambda(V_{gs} - Vto)} \qquad (4.3.4.4)$$

As, illustrated by Fig 4.3.3.1, the Id vs V_{ds} curves are almost level in the saturated region, indicating a early voltage of 12.5V (ie λ of $0.08V^{-1}$). If the lower limits of the simulated GaAs MESFET parameters of Fig 4.3.3-1 are used, a gain g_m/g_o of only 30 is determined under the operating conditions of V_{ds} = 2.5V and V_{gs} = 0.

However, the Id vs V_{ds} characteristics of Fig 4.3.3-1 were obtained from DC measurements of the GaAs MESFET which masks a property which has a serious consequence for circuit design, the frequency dependance of the output conductance, g_o. This frequency dependance of drain conductance is caused by the trapping and subsequent thermal re-emission of electrons in the substrate [86]. This thermal process is slow, having a time constant of the order of 1mS to 100mS. As a result of this effect, λ must be changed for DC and AC analysis of the circuit. For the experimental low threshold devices to be used, detailed AC (ie Scattering-parameter) information was not available, thus the foundry guide [66] indicated that the AC MESFET gain, g_m/g_o is typically in the range of 8 to 15. If a mid value of 11.5 is chosen to

represent the MESFET AC gain, this would correspond to an AC λ of $0.3V^{-1}$. The consequence of this is that the DC output conductance, g_o would be 96μS, while for frequencies above 1KHz the output conductance would increase to 360μS.

A major factor in determining the speed of a semiconductor device is the parasitic capacitance. The charge depletion region of a semiconductor device forms this parasitic capacitance. The depletion region beneath the gate produces parasitic capacitance between the gate and source, C_{gs} and the gate and drain, C_{gd}. As the width of the depletion region is determined by the applied voltage, each capacitance may be considered as a Schottky-barrier device with a voltage dependent capacitance. In normal operation the MESFET is biased with $V_{dg} > V_{gs}$, imposed by the design operating conditions that $V_{dg} = 2.5V$ with $V_{gs} = 0V$. Under these conditions, $C_{gs} >> C_{gd}$ and will dominate the input capacitance of the MESFET. The variation of C_{gd} with respect to applied voltage can be approximated by the expression derived for the ideal metal-semiconductor junction [87] and given by equation (4.3.4.5).

$$C_{gd} = \frac{C_{gdo}}{\sqrt{1 - \frac{V_{sd}}{V_{bi}}}} \qquad (4.3.4.5)$$

Where C_{gdo} = zero volt capacitance, V_{sd} = source-drain voltage and V_{bi} = built-in voltage for GaAs at 0.8V.

This equation is useful in many circumstances, but does not correctly describe the value of capacitance beyond the threshold voltage Vto, giving infinite or complex values for voltages equal to, or larger than V_{bi}. For junction voltages equal to or beyond the threshold voltage, the depletion layer extends to the substrate and the associated capacitance would fall to zero, with only fringing capacitance remaining. However, with the self imposed design restrictions of operating the MESFET under a common bias condition well into the saturated region, the value of parasitic governed by

equation (4.3.4.5) is only used as a first order approximation to determine the ft.

Since no AC information for the 20μm MESFET was available, an estimated value for the parasitic capacitance can be found by knowing that the process is intended to have a minimum ft of 20GHz. In addition, since the device is symmetrical the assumption that $C_{gso} = C_{gdo}$ can be made. Thus the operating capacitance C_{gs} and C_{gd} can be found using the expression for ft:

$$f\text{t} = \frac{g_m}{2\pi\left(C_{gso} + 0.49C_{gdo}\right)} \qquad (4.3.4.6)$$

By using the Shichman-Hodges equations, (4.3.4.1) and (4.3.4.2), an AC λ of $0.3V^{-1}$ and the metal-semiconductor junction equation (4.3.4.5) in conjunction with the ft equation (4.3.4.6) a small signal model for the 20μm GaAs MESFET device is derived and shown by Fig 4.3.4.-1 with SPICE parameters for a JFET Level 1 Model given in Table 4.3.4-1.

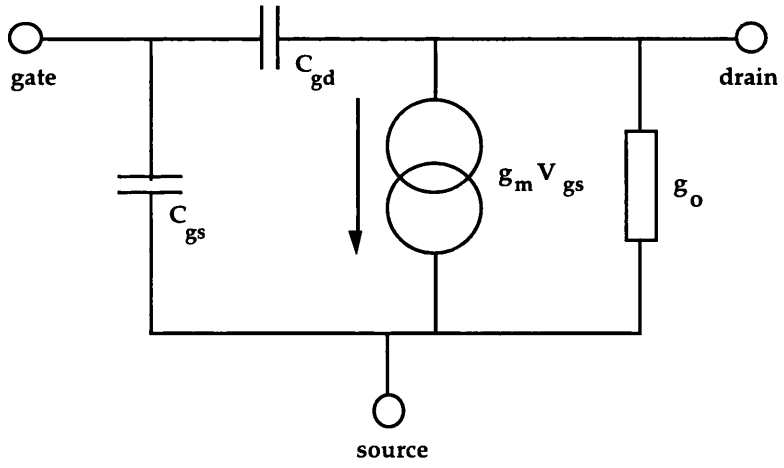


Fig 4.3.4-1 Small Signal Model for the 20μm GaAs MESFET

Parameter	Value
Vto	-1.0V
β	$1.2mA/V^2$
λ	$0.3V^{-1}$ *
PB	0.8V
Cgso	22fF
Cgdo	22fF

* DC value $0.08V^{-1}$

Table 4.3.4-1 SPICE Parameters for the 20μm GaAs MESFET

A small signal frequency response is shown by Figs 4.3.4-2a & b indicating MESFET gain g_m/g_o and *ft* using the JFET Level 1 Model above operating at the DC conditions of V_{ds} = 2.5V and Idss.

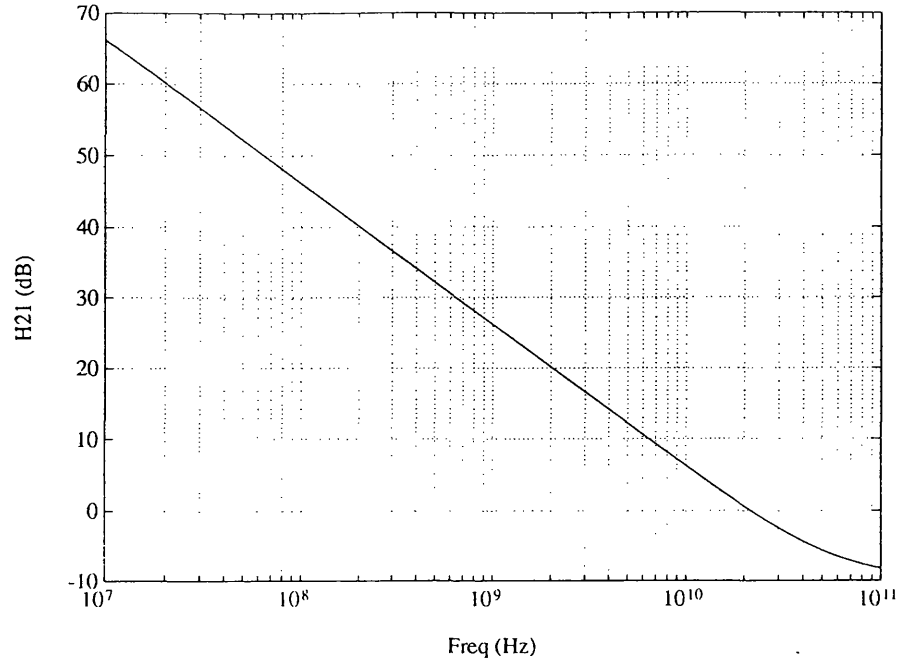


Fig 4.3.4-2a Simulated Small Signal Frequency Response of 20μm MESFET Current Gain H21

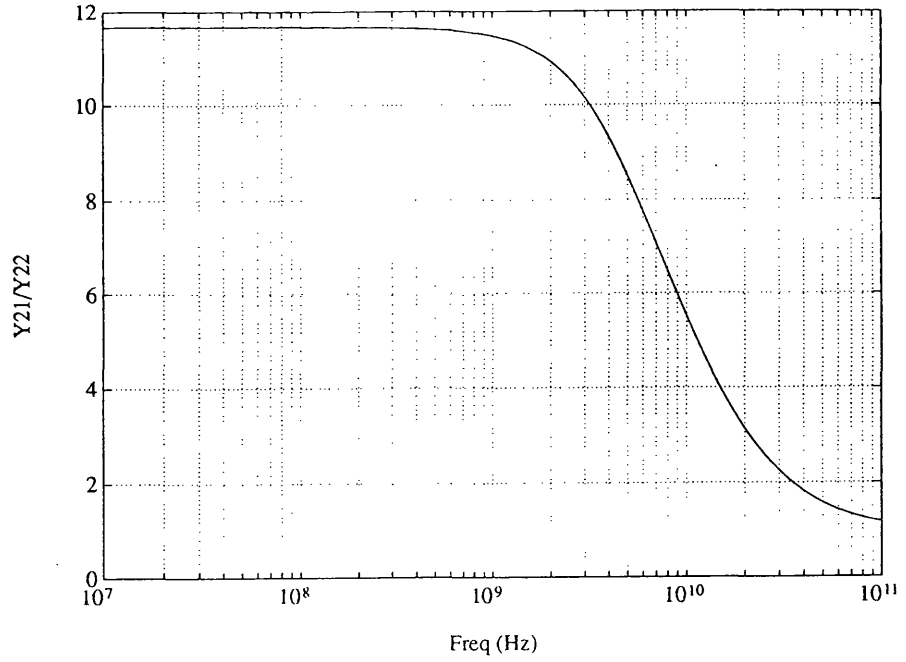


Fig 4.3.4-2b Simulated Small Signal Frequency Response of 20μm MESFET Voltage Gain (g_m/g_o)

4.4 Conclusions

In this chapter the GaAs MESFET characteristics of measured devices have been compared to device models used for circuit simulation. In general the more complex the model the greater the accuracy to which the measured data is characterised. In addition the more complex the device model the more sophisticated the simulator required to support the model.

An approach is to use the simplest GaAs MESFET model available (Shichman-Hodges) and to bias the device at the point where the model provides the greatest accuracy. This would allow the use of a public domain simulator such as SPICE which supported the use of the Shichman-Hodges model.

Therefore, as a result of the restrictions of the simulation tool used, the observed variation of the device characteristics from the Shichman-Hodges model to the measured data and the variation of data with various geometries measured, the circuit design was restricted to the use of a GaAs MESFET biased in *deep* saturation, operating at id=idss and the use of a single geometry device throughout.

This will present a very demanding challenge to the design of a fully tunable 2nd order bandpass filter realised in GaAs MESFET technology.

CHAPTER 5

An Novel OTA-C Integrator Approach Realised in GaAs MESFET Technology

5.1 Introduction

The design of a high quality fully tunable integrator for high frequency operation in GaAs MESFET technology is a key requirement to the successfully implementation of a bandpass filtering function. As a result of the limited modelling information and self imposed restriction discussed in chapter four, the design of such a tunable integrator poses a very demanding challenge.

In this chapter, the issues relating to the design of a fully tunable integrator realised in GaAs MESFET technology are discussed. Comparisons are made with integrators realised in other technologies such as Silicon CMOS and Bipolar and an alternative tunable integrator, both single-ended and fully balanced versions, is presented. In addition, a fully tunable 2nd order bandpass filter is realised using single-ended integrators.

5.2 Basic GaAs MESFET OTA

The availability of a complementary device, in such technologies as silicon CMOS, greatly facilitates the design of OTA-C integrators by using current mirrors. Using this approach a particularly simple method of external G_m tuning (ie tail current tuning) [38,88] can be implemented since the DC currents in the OTA device and thus the Gm, can be varied without altering DC voltage levels in the circuit [38,88]. In addition cascoding techniques [84] may be implemented to obtain very low levels of output conductance and voltage gains (G_m/G_o) in excess of 40dB have been reported [13] which are adequate for most practical analogue signal processing applications. Second-order OTA-C bandpass filters realised in CMOS with approximately independent control of Q and centre frequency have been demonstrated [44]. The filter consisted of a network of seven identical, very simple OTAs configured as integrators, buffers and variable shunt resistors.

However, situations exist where due to the absence of an adequate complementary device, circuit techniques involving current mirrors, tail

current tuning cannot be applied. Such instances are common when using a high frequency technology such as GaAs. This problem is exacerbated in the case of GaAs MESFET technology since in addition to the absence of a suitable *p*-channel device, the *n*-channel device displays a much larger drain conductance in saturation than their equivalents in other technologies [84].

An example of a GaAs OTA based on the MESFET inverter is shown in Fig 5.2-1. This consists of a common source *n*-channel FET M1 terminated in a floating *n*-channel load FET M2. It is assumed that the devices are identical and operate at Id=Idss·

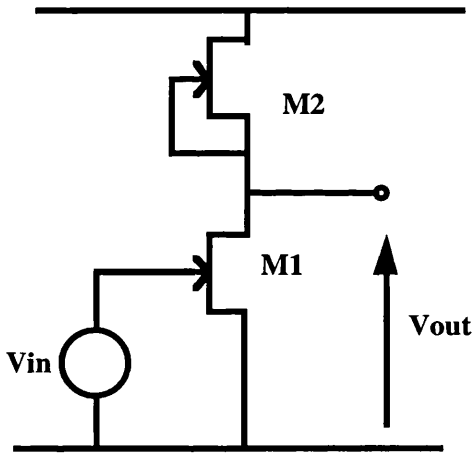


Fig 5.2-1 Basic MESFET Transconductor Cell

The low frequency voltage gain of this amplifier, v_{out}/v_{in} is $g_m/2g_o$, where g_m and g_o are the transconductance and drain conductance of the devices, respectively. Since the ratio g_m/g_o is typically in the range 8 to 15 for a GaAs MESFET foundry process the available voltage gain is correspondingly restricted. The voltage gain of the amplifier may be increased by reducing the drain conductances of both the amplifier and load devices. The drain conductance of the amplifier M1 can be reduced by adding a common gate (cascode) device M2, as shown in Fig 5.2-2.

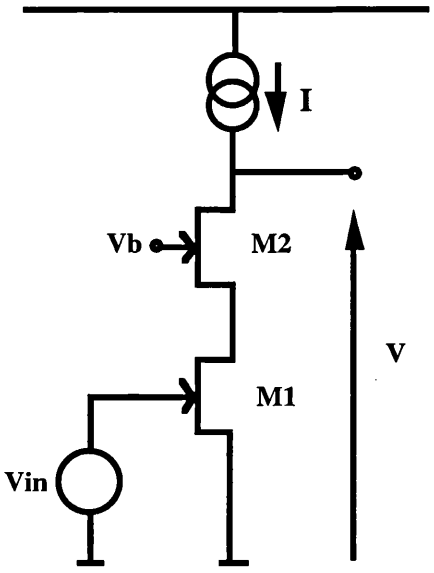


Fig 5.2-2 Single Cascode Amplifier Cell

Assuming identical devices, the output conductance of the composite amplifier, G_o, can be shown to be approximately g_o^2/g_m. Thus, if the amplifier of Fig 5.2-2 was terminated by a single *n*-channel depletion MESFET floating load as in Fig 5.2-1, the voltage gain would approach g_m/g_o, an increase of approximately 2. However, since for most practical analogue signal processing applications, a voltage gain of at least 40dB is required, this is clearly still inadequate. This problem can be alleviated by reducing the conductance of the load device M2 in Fig 5.2-1, but since this is a floating load, cascoding cannot be applied directly.

5.3 Bootstrap Gain Enhancement

5.3.1 Fixed Voltage Gain-Enhancement Techniques

The conductance of a floating load can be reduced by the application of broadband positive feedback, a technique known as *bootstrapping* [84], as shown schematically in Fig 5.3.1-1.

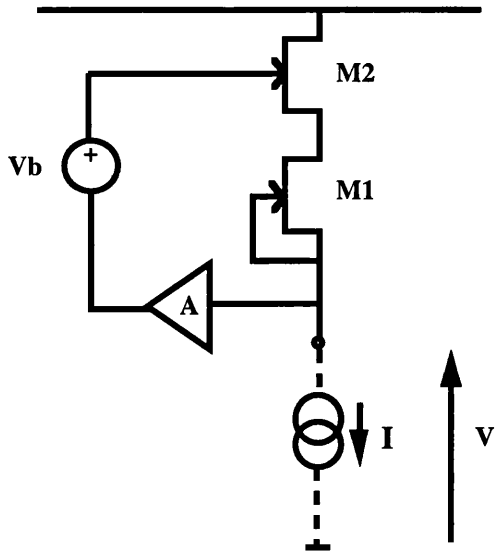


Fig 5.3.1-1 Generalised Bootstrap Load

The load device is M1, the voltage amplifier A with a voltage level shift and the source follower M2 have transfer functions A(s) and B(s) respectively. It can be shown that the output conductance of the load device M1 is given by equation (5.3.1.1):

$$Go = go[1 - A(s).B(s)] \qquad (5.3.1.1)$$

A practical implementation of a bootstrap load is shown in Fig 5.3.1-2a where M1 is the load device.

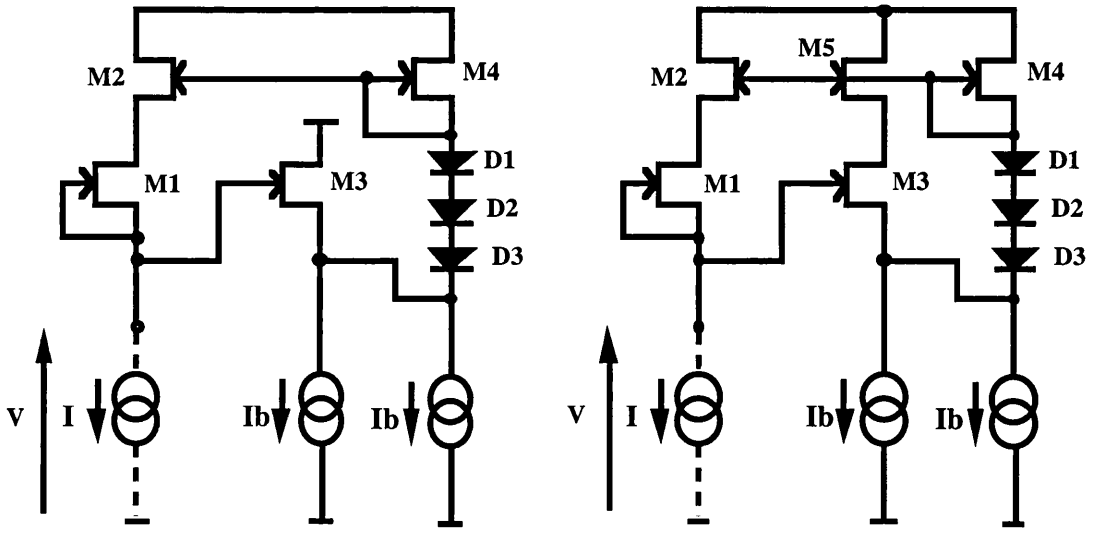


Fig 5.3.1-2 (a) Bootstrap Load (b) Improved Bootstrap Load

The bootstrap feedback is implemented by the source followers M2 and M3 and the voltage level shifting diode string D1-3. In addition, in Fig 5.3.2-1b, M3 is bootstrapped by the follower M5 to reduce its drain conductance and hence increase its efficiency as a source follower [84]. The output load conductance of the arrangement of Fig 5.3.1-2a, G_{oL}, is given approximately by equation (5.3.1.2):

$$G_{0L} \cong g_0\left[1-\left(\frac{g_m}{g_m+g_0}\right)^n\right] \qquad (5.3.1.2)$$

where n approaches 2. In Fig 5.3.1-1b, where the drain conductance of M3 is bootstrapped by the follower M5, n≅1. For a typical foundry MESFET process with g_m/g_o= 12, G_{oL} for the load circuit of Fig 3b is approximately $0.08g_o$, ie., a more than twelve-fold reduction. If such a load were used to terminate a single cascode transconductance amplifier with transconductance G_m, whose output conductance, G_{oA} was $g_o/(g_m/g_o)=0.08g_o$, the voltage gain is given by equation (5.3.1.3) as $6.25.g_m/g_o$ or approximately 37.5dB.

$$A_v = \frac{G_m}{G_{0L}+G_{0A}} \qquad (5.3.1.3)$$

OTAs with this level of voltage gain have been simulated [10,84]. Further gain enhancements can be obtained by means of additional stages of bootstrapping and cascoding [84], but this is achieved at the cost of high levels of circuit complexity.

Another type of fixed conductance load, intended specifically for use with GaAs MESFET technology is shown, in its original form, in Fig 5.3.1-3 [81].

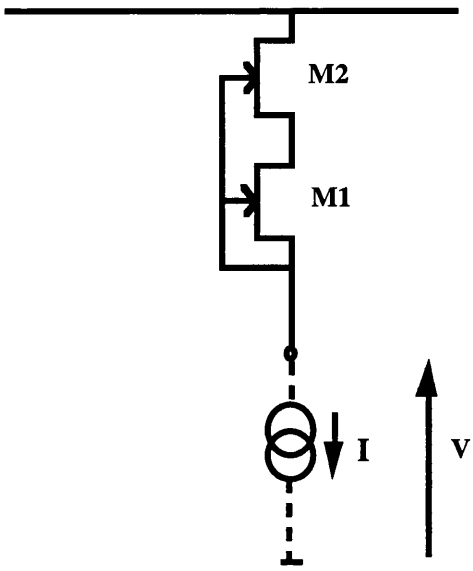


Fig 5.3.1-3 Self-Bootstrapped Load

In this approach, both the feedback and the DC level shifting are implemented by the device M2 and so the method has been called *self-bootstrapping*. It can be shown [81] that the resulting output conductance is given by equation (5.3.1.4):

$$G_{0L} = g_{o1}\left[1 - \frac{g_{m2}}{g_{m2} + g_{02}}\right] = \frac{g_{01}g_{02}}{g_{m2} + g_{02}} \qquad (5.3.1.4)$$

and OTA voltage gains of about 42dB have been reported [81]. In order that both M1 and M2 remain in saturation, it is necessary to make use of a particular property of short-channel GaAs MESFETs called *early saturation* [79]. Devices which display this property enter saturation at values of V_{ds} less than is the case for silicon FETs or long-channel GaAs MESFETs. In early saturation, the value of V_{ds} at the knee of the output characteristic tends to be independent of V_{gs} rather than related to it by a square law as in classical FET behaviour. However, early saturation is a strongly process dependent effect and in addition, its use in the circuit of Fig 5.3.1-2 requires the width of M2 to be much larger than that of M1 (typically 5-10:1) for both devices to remain in saturation. Consequently a well characterised MESFET foundry process featuring a wide range of device geometries is required for the successful use of the self-bootstrapped load technique. In addition, although

the circuit of Fig 5.3.1-3 is apparently much simpler than that of Fig 5.3.1-2, this advantage is offset by the large device width ratios required in self-bootstrapping, whereas the arrangement of Fig 5.3.1-2 can be implemented using identical, minimum geometry devices under common bias conditions. The circuit of Fig 5.3.1-3 has been subsequently developed and improved in various ways, eg., to achieve wider bandwidth [89,90] and smaller output conductance [91-93] while at the same time reducing (but not eliminating) the undesirable dependence on *early saturation.*

5.3.2 The Variable Gain Bootstrap Method

An alternative approach to the design of the OTA load is to realise A in Fig 5.3.1-1 as a voltage amplifier capable of realising a gain *greater than unity.* A gain of ≈ 1.1 is required to compensate the losses in the follower M2 represented by B(s) in equation (5.3.1.1) in order to drive Go to zero. In addition, if the gain of the amplifier A is made *variable,* this provides a convenient method by which Go can be varied without any additional *external* circuitry.

We begin by considering the generalised bootstrap load circuit as shown in schematic form in Fig 5.3.1-1. The bootstrap feedback is implemented by means of the voltage amplifier A, the DC level shift Vb and the source follower M2. M1 is the load device and M1 and M2 are assumed to be identical. The low frequency conductance of this arrangement, $G_{0L}=i/v$ is given by equation (5.3.2.1):

$$G_{0L} = g_0\left[1 - \frac{Ag_m}{g_m + g_0}\right] \qquad (5.3.2.1)$$

G_{0L} can be reduced to zero, or made negative by means of a suitable choice of the amplifier gain, A. If such a load circuit terminates an amplifier with transconductance G_m and output conductance G_{0A}, the resulting voltage gain A_V is given by equation (5.3.1.3) above. Hence A_V can in principle be made infinitely large, given a suitable choice of A in equation (5.3.2.1).

Consider the circuit of Fig 5.3.2-1 where the bootstrap feedback elements A and Vb are implemented by an OTA consisting of M3, 4 and 5.

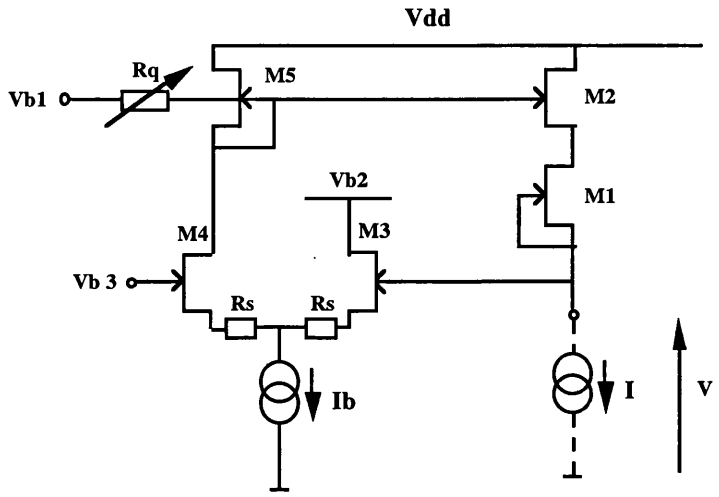


Fig 5.3.2-1 Variable Bootstrapped Load Circuit

Unlike the arrangements of Figs 5.3.1-1 & 5.3.1-2 the loop gain of this feedback arrangement can be greater than unity, with a maximum value (no source degeneration: Rs=0) of approximately $g_m/3g_0$, or about 3.8 for a typical foundry process. From equation (5.3.2.1), in order to drive G_{0L} to zero we require only that A≈1.1 and so there is scope for making G_{0L} small *and* tunable by arranging for the gain of the bootstrap OTA to be variable. In the circuit of Fig 5.3.2-1 this is achieved by source-degenerating the long tail pair M3, M4 and by connecting the variable resistor Rq between the gate of M5 and a DC bias point (AC ground). Note that since one terminal of Rq is connected to a DC bias point, Rq has the secondary effect of stabilising the DC operating point of the high impedance node at the gates of M2 and M5.

In practice, the variable resistor Rq is realised by a control network consisting of a series/parallel combination of two resistors and a MESFET operating in its linear region. The complete circuit of the variable bootstrap load is shown in Fig 5.3.2-2.

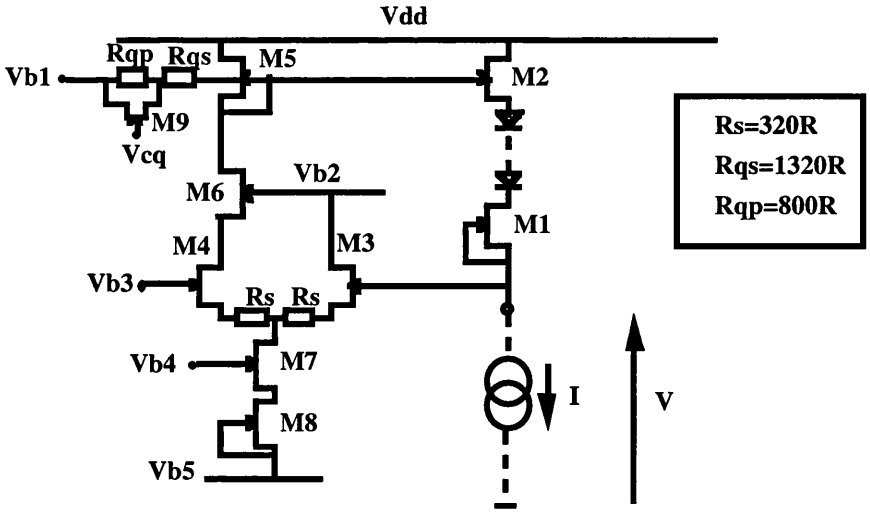


Fig 5.3.2-2 Complete Variable Bootstrap Load

Additionally, a stage of cascoding is added to the bootstrap amplifier which has the effect of increasing the open loop gain which increases the tuning range and reduces the sensitivity of the amplifier small signal AC gain to variations in the DC operating point. The tail current source Ib of Fig 5.3.2-2 is realised by the cascode combination M7,8 and the DC level shift between M1 and M2, necessitated by the addition of M6, is implemented by the diode string as indicated.

5.3.3 Sensitivity and Tuning

The gain of the amplifier, where the resistance of the control network is Rq and excluding the effect of the source follower M2 is given by equation (5.3.3.1) and derived in the Appendix.

$$A = \left(\frac{g_m}{g_o}\right).\frac{g_o R_q}{2(1+g_o R_q)(1+g_m R_s)} \qquad (5.3.3.1)$$

For 20μ MESFETs operated at Id=Idss with V_{ds}=2.5v and with the resistor values indicated on the diagram, the mid-range (nominal) value of Rq is about 2,000Ω, corresponding to a simulated output conductance, GoL, of 25.20μS. When V_{cq}-V_{b1} is varied in the range: -0.93V<V_{cq}-V_{b1}<0, GoL varies from 0.79μS to 44.41μS (or ±96.50%). This GoL tuning range is adequate for most OTA-C applications, and larger variations can be obtained by using

different values of Rqs and Rqp or by increasing the dimensions of M9.

Although we have demonstrated that external variation of Rq provides adequate control of A (and hence GOL), it is important to ensure that resistor variations due to process and /or thermal variations can be corrected by the tuning process. From (5.3.3.1), the first order differential sensitivity of A to a change in the value of Rq is given by equation (5.3.3.2) and derived in the Appendix.

$$S_{R_q}^{A} = \frac{R_q}{A}\frac{\partial A}{\partial R_q} = \frac{1}{1+g_0 R_q} \qquad (5.3.3.2)$$

and has a value of about 0.6 at the nominal tuning point of the system described above. If, however, the values of Rq and Rs are assumed to *track*, so that Rs=KRq, where K is a constant, then the gain sensitivity is given by equation (5.3.3.3) and derived in the Appendix.

$$S_{R_q}^{A} = \frac{1 - Kg_m g_0 R_q^2}{\left(1+g_o R_q\right)\left(1+Kg_m R_q\right)} \qquad (5.3.3.3)$$

This has a corresponding value of about 0.01 and shows that A (and hence GOL) is relatively insensitive to changes in the values of the resistors when the values track, which is a reasonable assumption for an IC realisation. On the other hand, the relatively high sensitivity to a unilateral variation of Rq allows an adequate tuning range to be obtained, as demonstrated above. The relative differences between the two levels of sensitivity indicates that OTA parameter variations brought about by thermal and process variations can be absorbed easily by the external tuning mechanism.

Another advantage of the load circuit just described is that, with the single exception of the control device M9, it is constructed from identical devices under identical DC bias conditions. As a result, it makes less demands on the foundry process than the self-bootstraped system mentioned above.

5.4 A Novel Transconductance (Gm) Tuning Method

5.4.1 The AC Current Shunt Method

Frequency tuning is a crucial issue in all integrated continuous time filtering systems. Using the OTA-C integrator approach requires the tuning of the forward transconductance, G_m, to vary the centre frequency of a bandpass filter or the cut-off frequency of a low pass filter (where $F_o=G_m/2\pi C_L$). In realisations where complementary devices are available (ie., silicon CMOS and bipolar technologies) and hence high quality current mirrors can be constructed, tail current tuning is generally used [37,38,53, 88,94]. This makes use of the fact that the device gm (and hence the OTA Gm) depends on the DC operating point of the device and can be implemented by varying the tail current source of the OTA. However, the method depends crucially on the availability of a high quality current mirror and this is not available in GaAs MESFET technology due to the absence of a complementary device. Another approach which has been suggested is to use additional transistors to bypass a proportion of the total drain currents of the OTA devices [90]. This approach allows G_m to be varied without altering the tail current and hence the DC load currents, but suffers from a limited tuning range necessitating extra circuitry and associated parasitic capacitance.

A novel approach to Gm tuning is proposed [95] which offers the widest tuning range available in GaAs MESFET technology. The OTA circuit is shown in Fig 5.4.1-1 and consists of a differential input, single cascode long-tail pair formed by devices M10, M11, and M12, the transconductance output is connected to an *ideal* current source load.

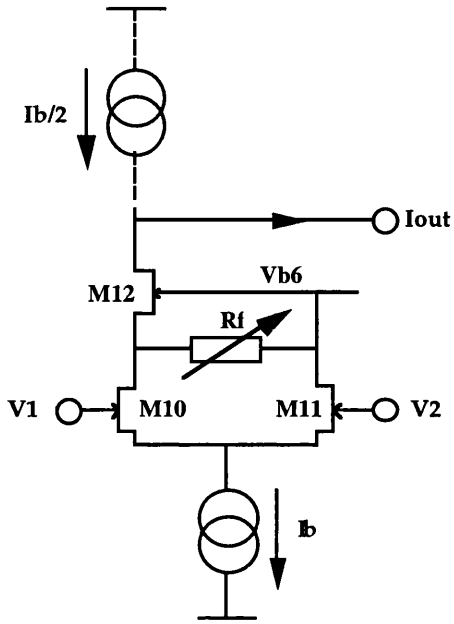


Fig 5.4.1-1 Variable Gain OTA

The novel Gm tuning proposed consists of connecting a variable resistor R_f between the drain of the OTA long tail pair transistor M10 and AC ground. If all device geometries are the same and operating at Idss the DC voltage applied across R_f is zero, thus the DC bias conditions of the OTA are unaltered. The small signal output current transfer function of the OTA is given by equation (5.4.1.1):

$$\text{iout} = \frac{R_f gm(gm+go)(v1-v2)}{R_f(2gm+3go)+1} \qquad (5.4.1.1)$$

From equation (5.4.1.1) it can be shown that if $R_f \to 0$ ie a short circuit, then $\text{iout} \to 0$, alternatively if $R_f \to \infty$ ie an open circuit, then the output current is given by equation (5.4.1.2):

$$\text{iout} \to \frac{gm(v1-v2)}{2}\left(\frac{1+gm/go}{3/2+gm/go}\right) \cong \frac{gm(v1-v2)}{2} \qquad (5.4.1.2)$$

which is the transconductance gain, Gm of a single ended long tailed pair.

However, the output conductance G_{oA} of the OTA is given by equation (5.4.1.3):

$$GoA = \frac{go(R_f go + 2)}{2\left\{R_f\left(gm + \frac{3}{2}go\right) + 1\right\}} \qquad (5.4.1.3)$$

when R_f is used to vary Gm of the OTA, the output conductance G_{oA} also varies. From equation (5.4.1.3) it can be shown that if $R_f \rightarrow 0$ ie a short circuit, then $G_{oA} \rightarrow$ go, alternatively if $R_f \rightarrow \infty$ ie an open circuit, then $G_{oA} \rightarrow 0.036go$. At the extreme of tuning, when $R_f = 0$, G_{oA} of the OTA increases to the intrinsic value of the MESFET go, thus greatly increasing the output conductance of the OTA.

The output conductance, G_{oA} of the OTA can be further reduced by adding an additional stage of cascoding as shown by Fig 5.4.1-2.

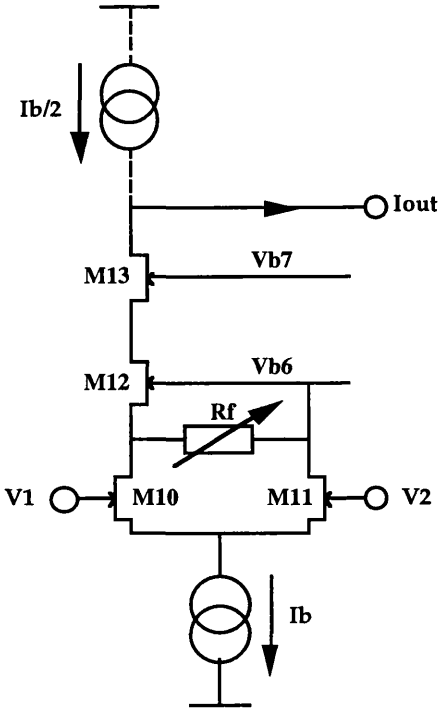


Fig 5.4.1-2 Double Cascode Variable Gain OTA

With the addition of the device M13, the small signal current transfer function of the OTA is given by equation (5.4.1.4):

$$\text{iout} = \frac{R_f gm(gm+go)^2(v1-v2)}{R_f\left(\sqrt{2}gm+\sqrt{3}go\right)^2+2(gm+2go)} \qquad (5.4.1.4)$$

From equation (5.4.1.4) it can be shown that if $R_f \to 0$ ie a short circuit, then $\text{iout} \to 0$, alternatively if $R_f \to \infty$ ie an open circuit, then the output current is given by equation (5.4.1.5):

$$\text{iout} \to \frac{gm(v1-v2)}{2}\left\{\frac{(gm/go)^2+2(gm/go)+1}{(gm/go)^2+\frac{5}{2}(gm/go)+2}\right\} \cong \frac{gm(v1-v2)}{2} \qquad (5.4.1.5)$$

Thus, with the addition of one extra cascoding device does not significantly change the low frequency transconductance gain of the OTA. However, the output conductance G_{oA} of double cascoded OTA is given by equation (5.4.1.6):

$$GoA = \frac{go^2(R_f go+2)}{2\left\{R_f\left(gm^2+2go^2+\frac{5}{2}gmgo\right)+(gm+2go)\right\}} \qquad (5.4.1.6)$$

and when the double cascoded OTA is subjected to Gm tuning the output conductance G_{oA} is significantly reduced. From equation (5.4.1.6) it can be shown that if $R_f \to 0$ ie a short circuit, then $G_{oA} \to 0.071go$, alternatively if $R_f \to \infty$ ie an open circuit, then $G_{oA} \to 0.0028go$. At the extreme of tuning, when $R_f = 0$, G_{oA} of the OTA is maintained at a low value compared to the single cacoded case, with no degradation in forward transconductance Gm.

5.4.2 Tuning Range and Extension

In practice, the variable resistor R_f shown in Fig 5.4.1-2 is realised by a MESFET operating in its linear region. The complete circuit of the variable gain OTA with an *ideal* current source load is shown in Fig 5.4.2-1.

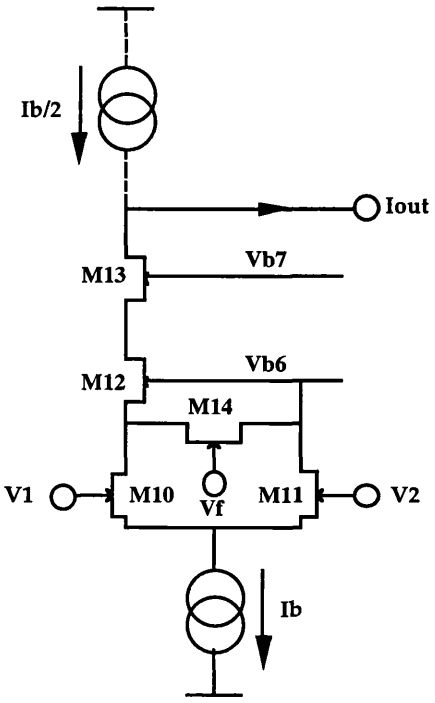


Fig 5.4.2-1 Complete Variable Gain OTA

The source of the control device, M14 is connected to a DC bias level Vb6 while its drain is connected to the source of M12. Since all the devices (apart from M14) operate at Idss, then the DC voltage at the source of M12 is at Vb6 and so the control device M14 operates in its linear region at Vds (DC)=0, acting purely as an AC current shunt.

The control device, M14 channel resistance is varied by a DC voltage V_f, applied between the gate and source. If the Schichman-Hogers MESFET model is used to determine the channel resistance of the device, then if V_f-V_{b6} is less than the threshold voltage Vto of -1V, the device is open circuit. Alternatively, if V_f-V_{b6} is increased to 0v DC the channel resistance reduces to approximately gm. The resistance can be further reduced by increasing V_f-V_{b6} to ~0.6V just before forward diode conduction. Therefore the range of control voltages Vf are restricted to $0.6v \leq V_f - V_{b6} \leq -1v$.

Using the proposed approach with common geometry devices and for a typical foundry MESFET process with $g_m/g_o = 11.5$, the *minimum* value of forward transconductance Gm_s is given by equation (5.4.2.1):

$$Gm_s \cong \frac{gm}{2}\left\{\frac{gm/go+2}{2(gm/go+9)}\right\} \cong \frac{gm}{2}0.49 \qquad (5.4.2.1)$$

From equation (5.4.1.5) the *maximum* value of forward transconductance Gm_O, obtainable, corresponding to the control device M14 in pinch off, is gm/2. Therefore, the maximum tuning range using the proposed approach is given by equation (5.4.2.2):

$$\frac{Gm_s}{Gm_o} \cong 0.49 \qquad (5.4.2.2)$$

which corresponds to a Gm tuning range in excess of ±25% without altering the DC conditions of the circuit. Since the purpose of varying Gm is to compensate for the tolerance of a fabricated capacitor which is subjected to a typical variation of ±20% [66], the tuning range achieved is more than adequate.

A larger tuning range is possible by connecting one or more control devices, M14 in parallel such that the overall channel resistance connected at the drain of M10 of Fig 5.4.2-1 is reduced. If the assumption is made that the minimum channel resistance of the multiple control device M14 is 1/ngm, where n is the number of equal geometry devices connected in parallel, the minimum forward transconductance Gm_s is given by equation (5.4.2.3):

$$Gm_s \cong \frac{gm}{2}\left\{\frac{(gm/go+2)}{(gm/go+5/2)+n(gm/go+2)}\right\} \cong \frac{gm}{2}\left\{\frac{1}{1.04+n}\right\} \qquad (5.4.2.3)$$

Therefore, the maximum tuning range may be increased as shown by equation (5.4.2.4):

$$\frac{Gm_s}{Gm_o} \cong \frac{1}{1.04+n} \qquad (5.4.2.4)$$

Using this approach the tuning range has been extended to ±33% for n=2

and ±37% for n=3. It is important to note that the extended tuning range is obtainable within the control voltage restriction of $0.6v \leq V_f - V_{b6} \leq -1v$.

The simulated forward transconductance, Gm frequency response with different number of tuning MESFET connected in parallel is shown in Fig 5.4.2-2.

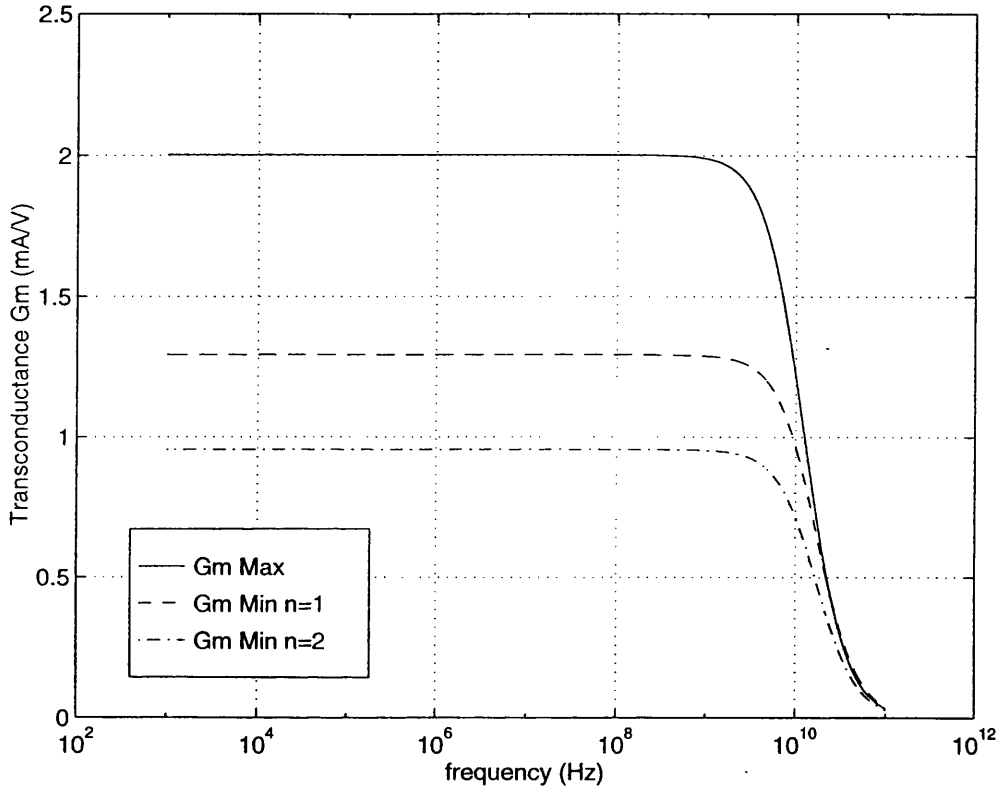


Fig 5.4.2-2 Gm Frequency Response with Tuning

5.5 Fully Balanced OTA and Load Conductance

5.5.1 Tunable OTA

The extension of the single-ended design to a fully balanced form in relation to the OTA part of the integrator is simply achieved by doubling the existing circuitry. The OTA, modified for balanced operation is shown in Fig 5.5.1-1 In order to realise, for example, an OTA-C state variable filter, dual balanced inputs are required and this is conveniently implemented by means of two long tail pairs (M10a,b - M11a,b) with outputs connected in parallel, as shown in Fig 5.5.1-1.

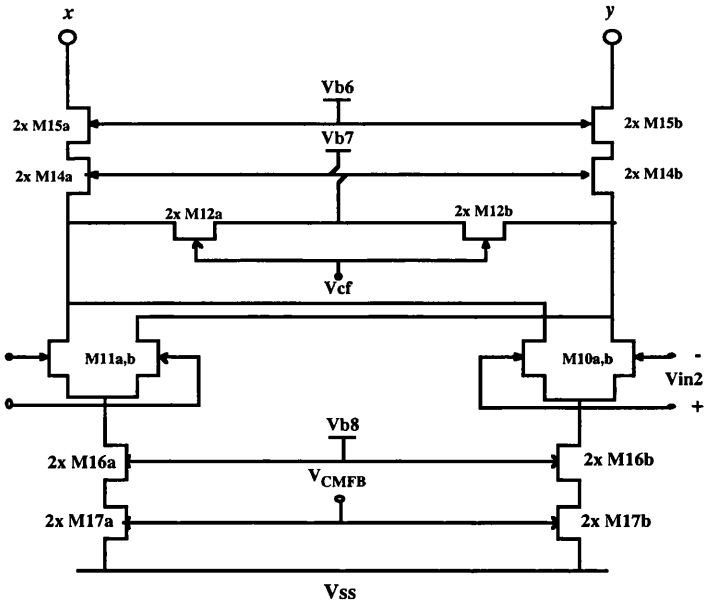


Fig 5.5.1-1 Fully Balanced, Differential OTA With Controllable Transconductance, Gm

To ensure that the MESFET devices M11ab and M10ab are operating at Idss, the current sources formed by M16ab and M17ab must be doubled (ie two devices connected in parallel) as in the case for the single-ended design. In addition, the cascoding devices M14ab and M15ab are also required to be formed by two MESFETs connected in parallel to ensure their operation at Idss and thus maintain the Gm tuning triode region devices M12ab with $V_{ds}=0$.

The complementary output current nodes are *x* and *y*, with the overall Gm of the OTA being controlled by the devices M12a,b operating in their linear region with DC $V_{ds}=0$, as in the single-ended version. Since the Gm tuning method used is an AC current shunt, M12ab device on resistance must be low in comparison to the conductance seen at the source of M14ab, thus to achieve the desired tuning range obtained in the single-ended case, two MESFET devices are connected in parallel to reduce the overall on resistance for high values of Vcf.

5.5.2 Tunable Load Conductance

The single-ended load arrangement of Fig 5.3.2-2 can be adapted to fully balanced operation simply by duplicating the existing circuitry as in the case of the OTA. However, in this case, the duplication of the cascoded differential pair M3,4,6 and its associated current source M7,8 can be avoided [96] by using both outputs of the existing differential pair in the cross-coupled arrangement shown in Fig 5.5.2-1.

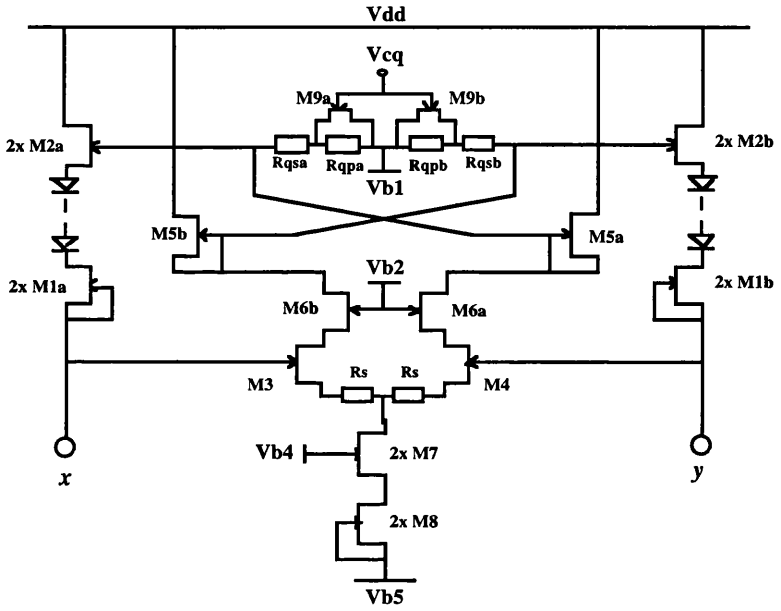


Fig 5.5.2-1 Fully Balanced, Variable Load Conductance, Go

As a result, the number of extra components (and hence extra power consumption) required to extend the single-ended load circuit to fully balanced differential form is modest. The fully balanced, variable load conductance, Go is seen at nodes x and y. As in the case of the single-ended design, all the MEFSET devices are operating under common DC conditions at Idss and as such the current source of the variable gain bootstrap load devices M1ab with their associated voltage followers M2ab are formed by the connection of two devices in parallel.

The high sensitivity of the bootstrap amplifier gain to resistor ratio variation, and unilateral resistor changes demonstrated in the single-ended design is preserved in its fully balanced form.

5.5.3 Common Mode Stability

A particular feature of fully balanced systems is the need for external stabilization of the common mode (CM) DC operating point [97]. This can be a serious problem in tuned OTAs of the type where Gm is varied by means of tail current tuning [37,38,53, 88,94]. For the design presented, Gm is varied *without* altering the DC bias conditions in any way, allowing a simpler common mode feedback (CMFB) circuit to be employed [96] and this circuit is shown in Fig 5.5.3-1.

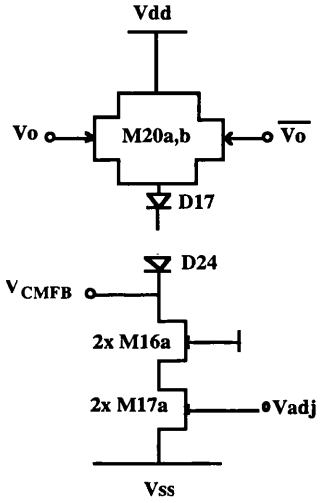


Fig 5.5.3-1 Common Mode Stabilization Circuit

The buffered outputs from the OTA are applied to the long tail pair consisting of M20a,b whose source voltage is a measure of the CM output voltage. This DC voltage is level shifted and applied to the gates of the OTA tail current source transistors in Fig 5.5.1-1, thus stabilising the overall CM operating point of the system. Note that the CM operating point of the system can be adjusted by means of the current source of the CM stabilization circuit (Vadj) as shown in Fig 5.5.3-1.

The fully balanced, differential OTA-C integrator is completed by the connection of an integrating capacitor C_L between nodes x and y of Figs. 5.5.1-1 and 5.5.2-1 and as shown by Fig 5.5.3-2. The current sources are conventional single cascode arrangements [95].

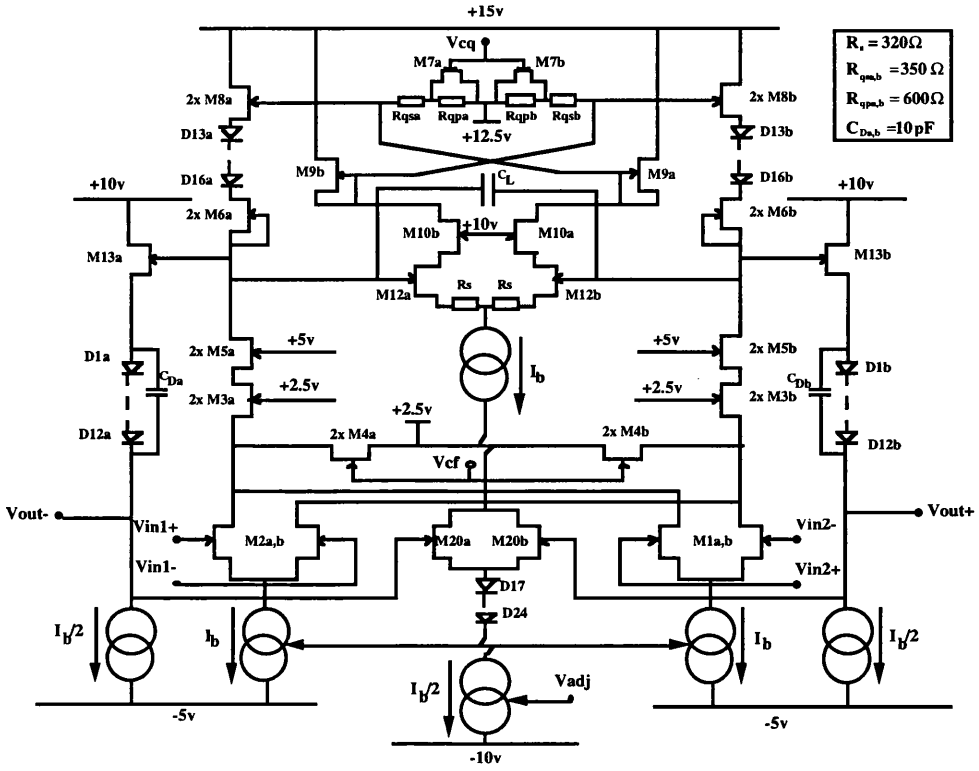


Fig 5.5.3-2 Complete Dual Input Fully Balanced OTA-C Integrator

5.6 Simulated Performance of OTA-C Integrator

5.6 1 Single-Ended OTA-C Integrator

The circuit of the complete OTA-C integrator is given in Fig 5.6.1-1. The effect of the double cascoding is to decrease the contribution of the OTA output conductance G_{OA} to the total output conductance Go as illustrated by section 5.4.1. This serves two main functions: firstly, since the output conductance of the OTA is now very small (0.071go at the extremes of Gm tuning), Go is dominated by the conductance of the bootstrap load G_{OL} and hence increases the available Go tuning range for a given Rq. Secondly, varying the conductance of M12 (to implement Gm tuning) has very little effect on the OTA output conductance Go and hence the functions of Gm and Go tuning are effectively de-coupled, facilitating the design of simple control circuitry. Although the presence of two levels of cascoding restricts the bandwidth of the OTA somewhat, this is immaterial since the overall bandwidth of the system is dominated by the load.

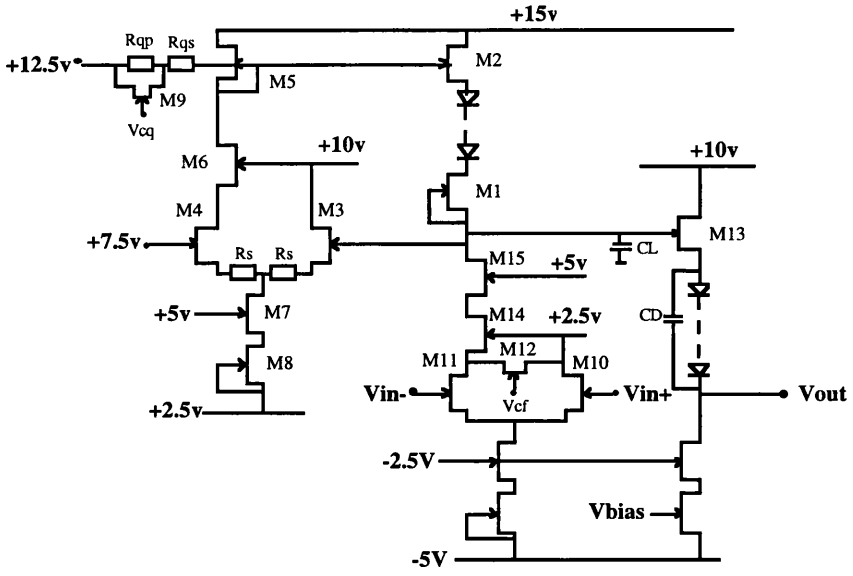


Fig 5.6.1-1 Complete Fully Tunable OTA-C Integrator with Independent Control of Gm and Go

The output current from the OTA/bootstrap load combination is passed through the integrating capacitor C_L and the resulting voltage buffered and level shifted to facilitate connection to the next stage. The output buffer consists of the source follower M13, a diode string and an externally adjustable cascode current source, allowing DC offsets to be nulled. The excess phase contribution of the diode string is compensated by the bypass capacitor C_D. The unity gain voltage buffers serve a dual purpose, enabling a DC level shift from the transconductance point, loaded by C_L to the input of the next OTA-C, and also providing a low impedance output allowing a number of 2nd order sections to be cascaded.

The load capacitor C_L was chosen for a nominal unity gain frequency of 60MHz (C_L=4pF). Although in theory the device widths can be scaled to any required value, this should be kept as small as possible in order to minimise power consumption. A device width of 20μm was used in the design, which is the minimum width for which the foundry process is characterised.

5.6.2 Integrator Frequency Response with Tuning

The frequency response of the OTA-C integrator was simulated using the SPICE level 1 (jFET) model with parameters chosen for best fit to measured foundry data for a 20μ × 0.5μ device. Figs 5.6.2-1a & b show plots of the amplitude and phase of the AC frequency response with tuning of the circuit of Fig 5.6.1-1.

Figure 5.6.2-1a shows the variation in gain (ie., 40.2 to 88.4) achieved by controlling Go, while maintaining Gm constant. This was obtained by varying Vcq-12.5V (nominal value: -0.6V) in the range: -0.28V > Vcq-12.5V > -0.74V. Note that the unity gain frequency remains unaltered at 60MHz under this variation of Go. Figure 5.6.2-1b shows the variation of the unity gain frequency (ie., 45MHz to 70MHz) achieved by controlling Gm, while maintaining Go constant. This was obtained by varying Vcf-2.5V (nominal value: -0.6V) in the range: 0.6V > Vcf-2.5V > -1V. Note that in this case the gain also varies since this is a function of both Gm and Go. Both figures show the excess phase due to the finite bandwidth of the OTA.

In addition, by way of a comparison the fully balanced version was also simulated to show that none of the tuning behaviour of the single-ended version was lost. The AC frequency response with tuning of the circuit of Fig 5.5.3-2 is shown by Figs 5.6.2-2a & b.

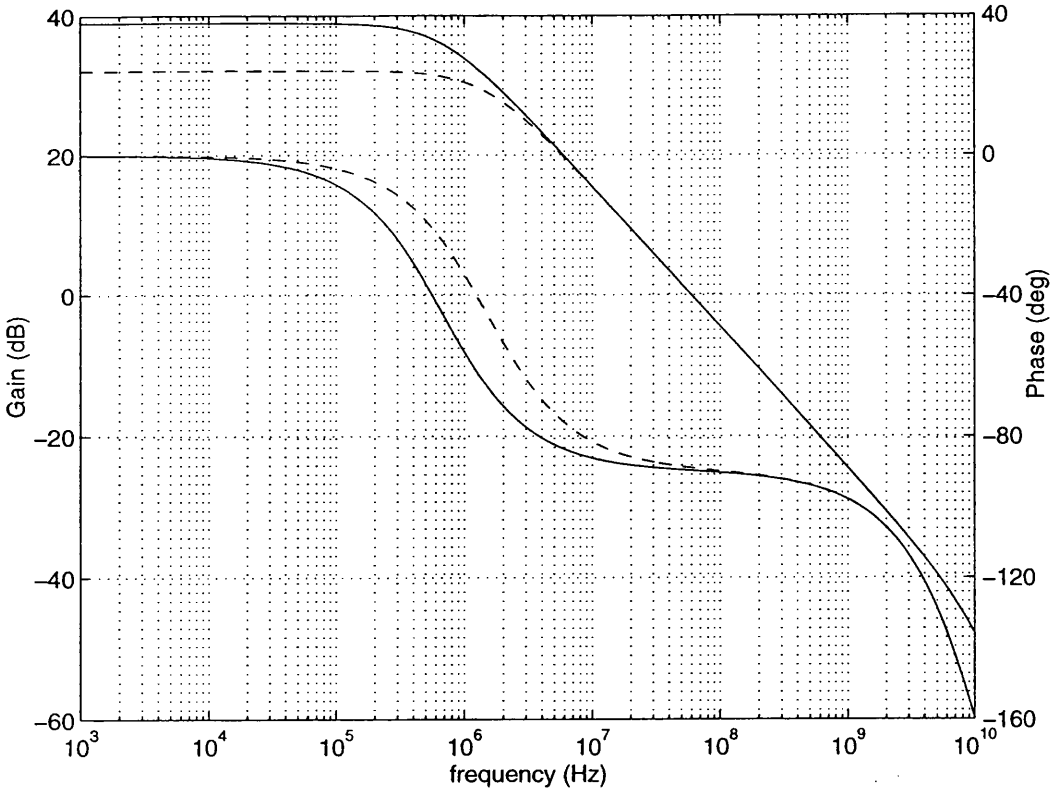


Fig. 5.6.2-1a Single-Ended Amplitude & Phase Response of the OTA-C Integrator (Gm constant, Go varied)

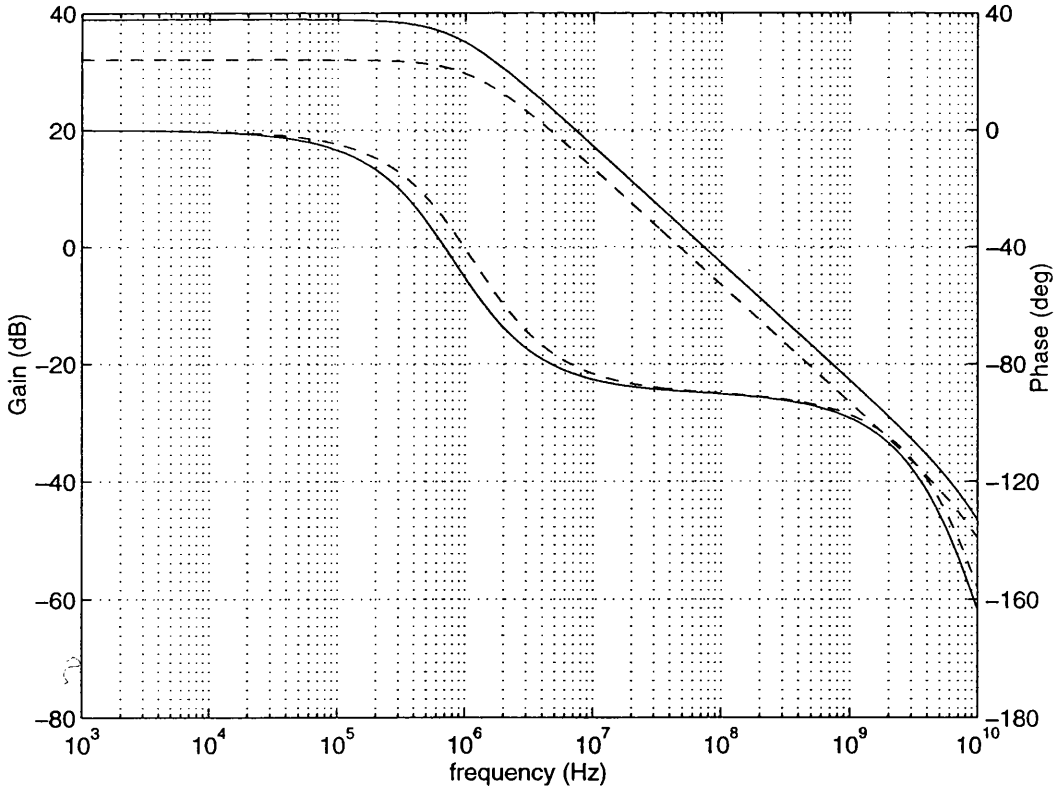


Fig. 5.6.2-1b Single-Ended Amplitude & Phase Response of the OTA-C Integrator (Gm varied, Go constant)

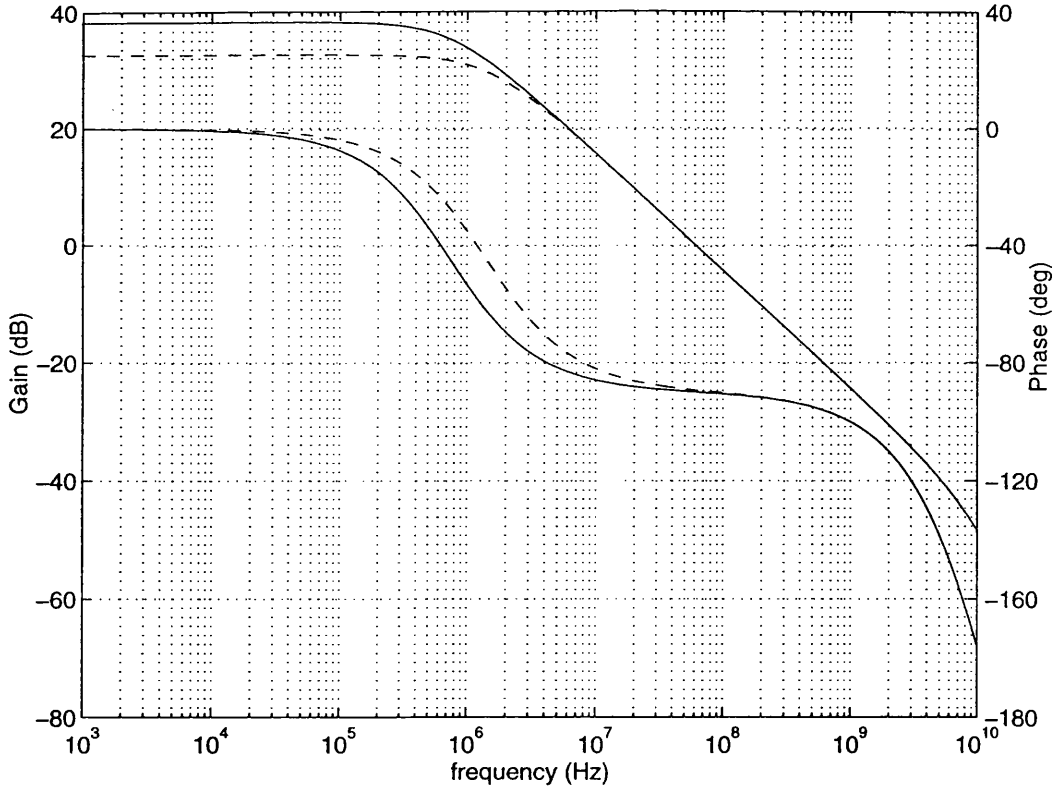


Fig. 5.6.2-2a Fully Balanced Amplitude & Phase Response of the OTA-C Integrator (Gm constant, Go varied)

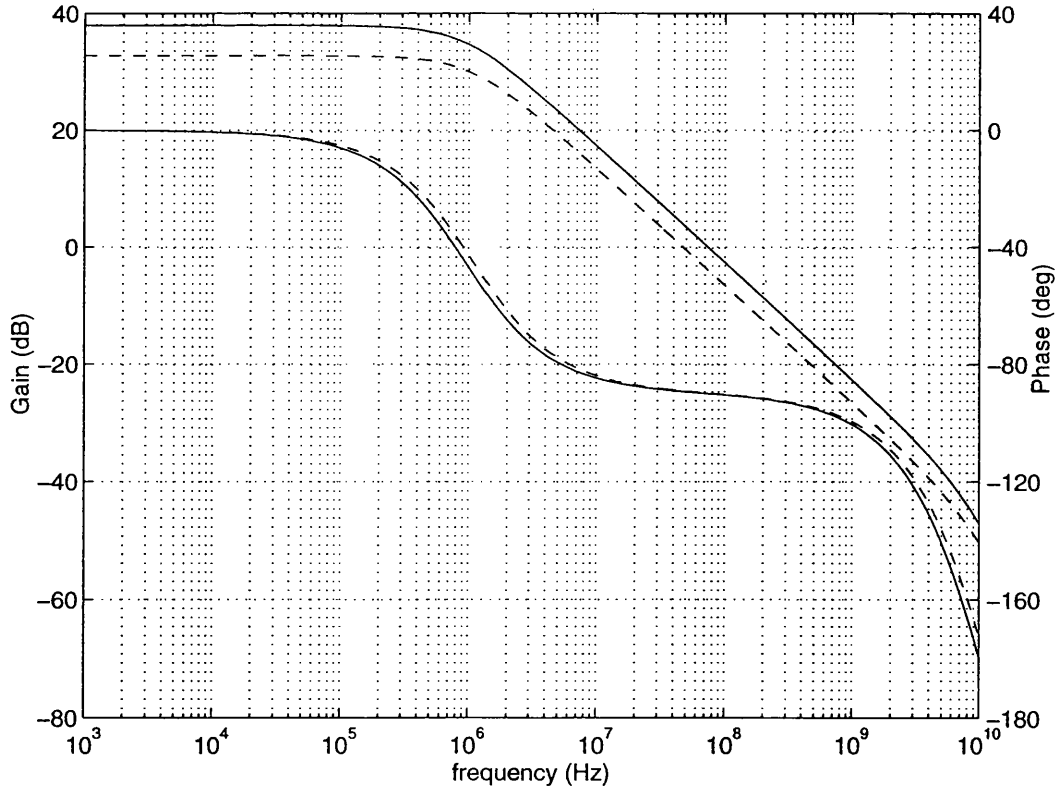


Fig. 5.6.2-2b Fully Balanced Amplitude & Phase Response of the OTA-C Integrator (Gm varied, Go constant)

5.6.3 Integrator Distortion with Tuning

In assessing the total harmonic distortion (THD) of an OTA, a frequently adopted method is to measure the harmonic purity of the short circuit output current in response to a sinusoidal input voltage [89,94]. However, when the OTA is terminated by a capacitor as an OTA-C integrator for use in a state variable filter, the non-zero load impedance allows an AC voltage to appear at the output node which introduces additional harmonic distortion. In [98,99] a more comprehensive distortion test was proposed which consists of the following set of *three* measurements of the output in response to a sinusoidal input:

(1) Short circuit output current ('S/C');
(2) Output voltage with a resistive load of 1/Gm ('1/Gm');
(3) Output voltage with load open circuit ('O/C')

Measure (1) is the traditional method of evaluating the linearity of an OTA, effectively ignoring the load conductance Go. In measure (2) the OTA is shunted with a resistive load (replacing the load capacitor) equal to the modulus of the load impedance of an OTA-C integrator at its unity gain frequency (ie., the centre frequency of a 2nd order state variable filter) and the output voltage is measured for non-linearity. Measure (3) is an extreme test in which the OTA is effectively employed as a voltage amplifier with the controllable Go serving as load providing a voltage gain of 30dB and as in the case of measure (2) the amplified output voltage is measured for non-linearity.

The AC amplitude frequency response of the OTA-C Integrator shown in Fig 5.6.1-1 are presented by Fig 5.4.2-2, and Fig 5.6.3-1 when connected as required for tests 1,2 and 3 above. In all cases the integrating capacitor C_L is disconnected. In the case of test (1), the frequency response of the OTA transconductance, Gm is shown in Fig 5.4.2-2 when subjected to tuning. For tests (2) the OTA is loaded in place of the integraing capacitance C_L with a resistance equal to 1/Gm, giving a unity voltage gain, while for test (3) the

load conductance Go is varied with Gm tuning to maintain a voltage gain (Gm/Go) of 30dB, as shown in Fig 5.6.3-1.

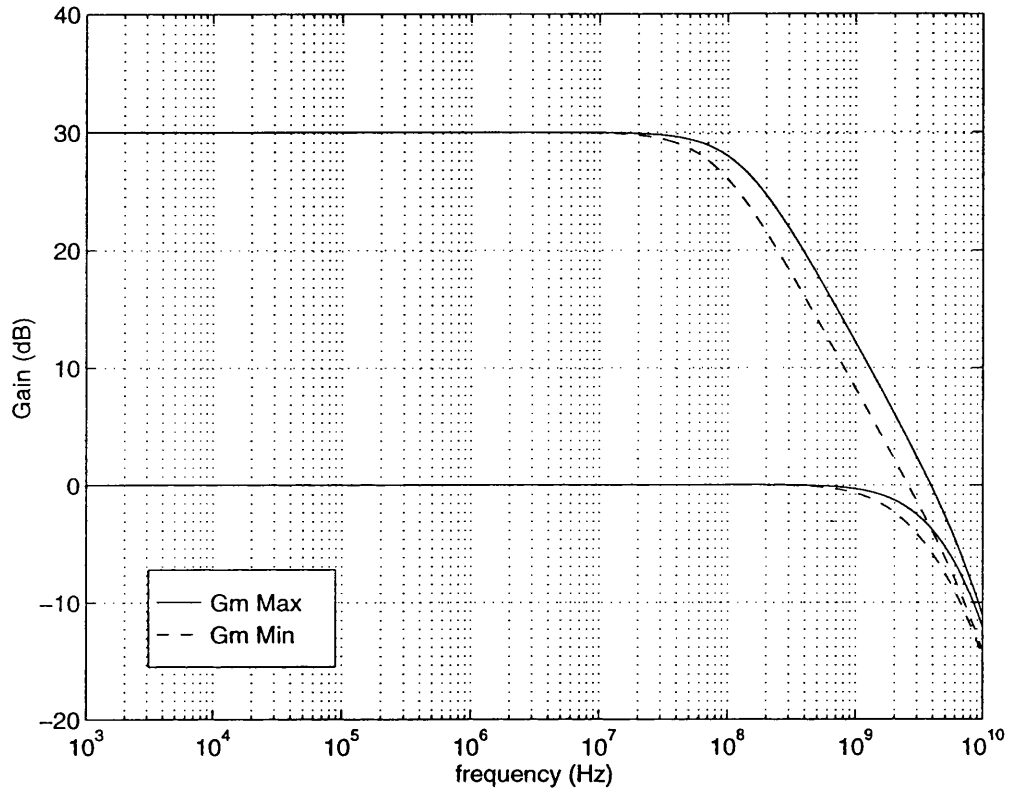


Fig. 5.6.3-1 Resistive Load (1/Gm) and Voltage Gain (30dB) Frequency Response (C_L=0)

In order to assess the linearity of the OTA, AC distortion measurements were carried out with the circuit connected in the three configurations discussed above and with sinusoidal inputs of amplitude 500mV and 100mV. Since the bandwidth of the OTA is different in each configuration, the linearity tests were carried out at 10% of the nominal -3dB frequency in each case so that the results were not affected by high frequency harmonic attenuation. As in the case of the bandwidth measurements, linearity was measured with Gm at the extremes of its range. The results are presented in Tables 5.6.3-1, 2 &3.

Single-Ended Gm (mA/V)	THD with output s/c @ 1GHz, Single-Ended (%)	
	Vin=500mV (pk)	Vin=100mV (pk)
1.99	1.68	0.32
1.64	1.31	0.20
1.29	1.41	0.19

(a)

THD with output s/c @ 1GHz, Fully Balanced (%)		Fully Balanced Gm (mA/V)
Vin=500mV (pk)	Vin=100mV (pk)	
1.09	0.03	8.03
0.75	0.03	6.63
1.01	0.04	5.09

(b)

Table 5.6.3-1 : Total Harmonic Distortion of OTA Transconductance Gm (short circuit output current) : (a) Single-Ended (b) Fully Balanced

Single-Ended Gm (mA/V)	THD with load=1/Gm Vin=100mV(pk) @ 400MHz, (%)
1.99	0.26
1.64	0.16
1.29	0.12

(a)

THD with load=1/Gm Vin=100mV(pk) @ 400MHz, (%)	Fully Balanced Gm (mA/V)
0.02	8.03
0.01	6.63
0.02	5.09

(b)

Table 5.6.3-2 : Total Harmonic Distortion of OTA Voltage Gain (1/Gm Resistive Load) : (a) Single-Ended (b) Fully Balanced

Single-Ended Gm (mA/V)	THD with Gm/Go=60 Vo=500mV(pk) @ 10MHz (%)
1.99	2.36
1.64	0.96
1.29	6.25

(a)

THD with Gm/Go=60 Vo=500mV(pk) @ 10MHz (%)	Fully Balanced Gm (mA/V)
0.21	8.03
0.15	6.63
0.44	5.09

(b)

Table 5.6.3-3 : Total Harmonic Distortion of OTA Voltage Gain (Load Open Circuit, Go) : (a) Single-Ended (b) Fully Balanced

The overall THD levels of the OTA, measured under a variety of conditions, are quite moderate. If the peak signal level (input for tests 1 & 2, output for test 3) is restricted to 100mV (peak), the THD levels are at most of the order of 1%. On the other hand, larger signal levels produce quite high levels of

THD, about 10% in some cases. If required, these levels can be reduced by employing source degeneration in the OTA. Alternatively, the use of the fully balanced version of the OTA, provides a more comprehensive solution to the reduction of THD levels.

5.7 Simulated Performance of Bandpass Filter

5.7.1 2nd Order CT Bandpass Filter

The proposed 2nd order bandpass section is shown in Fig 5.7.1-1. It consists of two Operational Transconductor-C amplifiers (OTA-C) of the type in Fig 5.6.1-1, configured as a two integrator loop giving a bandpass response.

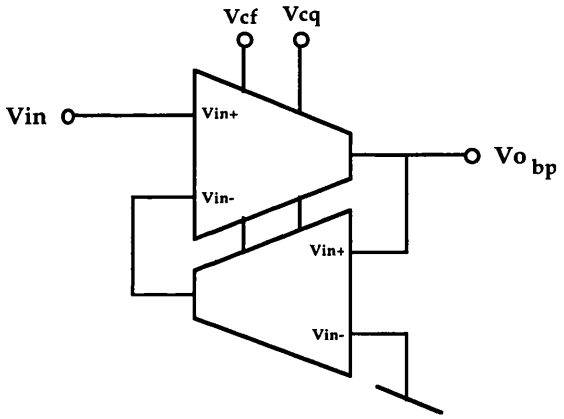


Fig 5.7.1-1 Fully Tunable 2nd Order Bandpass Section

The OTA-C integrators which feature independent control of the transconductance gain (G_m) and output conductance (G_o), enables high and variable DC gains to be achieved without the use of separate transconductors configured as linear resistors [94,100]. For the case of high gain (ie low loss, thus high Q) the bandpass section exhibits good dc stability.

The 2nd order transfer function T(s) (ignoring excess phase shifts due to amplifier bandwidths) is given by equation (5.7.1.1):

$$T(s) = \frac{\frac{Gm}{C_L}\left(s + \frac{Go}{C_L}\right)}{s^2 + \frac{2Go}{C_L}s + \frac{Gm^2 + Go^2}{C_L^2}} \qquad (5.7.1.1)$$

For the case of high Q, where Gm is much greater than Go, then the centre frequency F_O and Q can be shown to be governed by equations (5.7.1.2) & (5.7.1.3):-

$$f_o \cong \frac{Gm}{2\pi C_L} \qquad (5.7.1.2)$$

$$Q \cong \frac{Gm}{2Go} \qquad (5.7.1.3)$$

and so for $Q \leq 30$, we require that maximum gain $(Gm/Go) \leq 60$ (35dB).

5.7.2 Bandpass Filter Frequency Response with Tuning

The amplitude frequency response of the bandpass filter circuit of Fig 5.7.1-1 is shown by Figs 5.7.2-1a & b.

The frequency response of Fig 5.7.2-1a shows the tuning range of Q available with the application of a DC voltage varied -0.4V > Vcq-12.5V > -0.7V to control Go while maintaining Gm constant (ie centre frequency 'F_O' remains unaltered). The Q of the filter varies between 24 to 41.

The frequency response of Fig 5.7.2-1b shows the range of F_O available by the application of a dc voltage varied 0.6V > Vcf-2.5V > -1V controlling Gm while maintaining Go constant. Note that whereas Q can be varied independently of F_O, variation of F_O also varies Q to some extent, since Q=(Gm/2Go) to a 1st order. However, the independence of the Q control represents a considerable advantage in a system requiring automatic adaptive tuning.

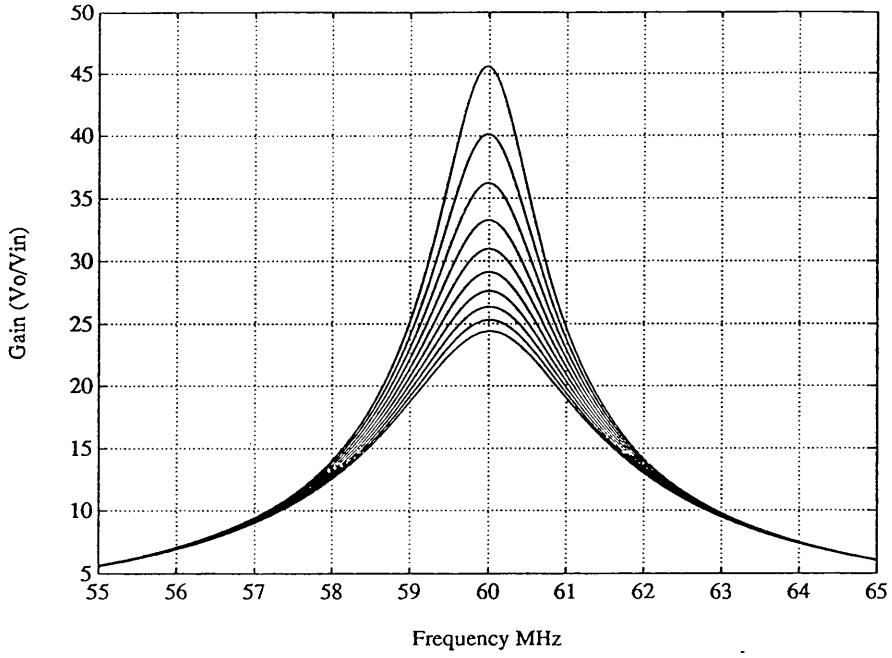


Fig 5.7.2-1a Q Tuning Frequency Response (G_m constant : G_o varied)

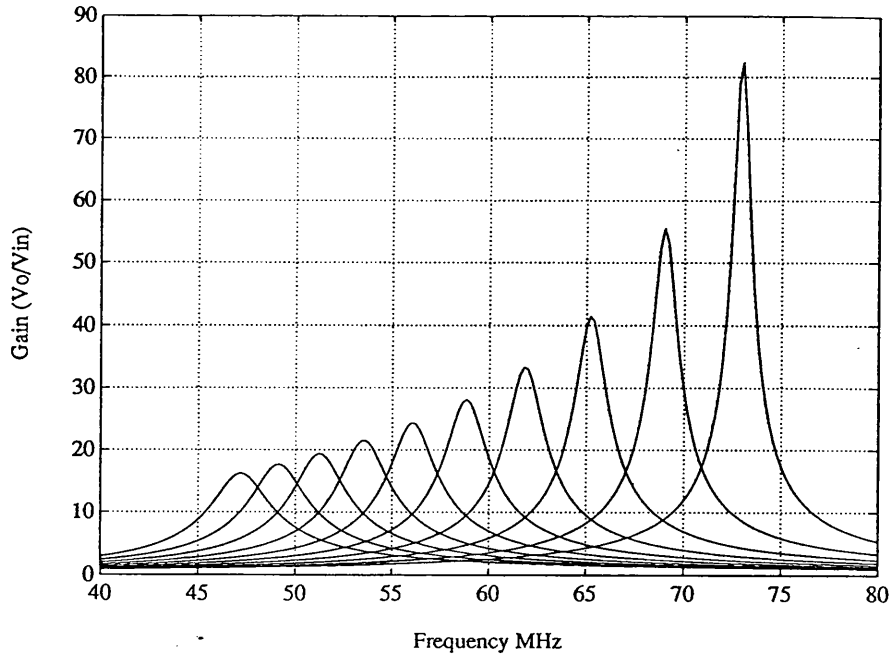


Fig 5.7.2-1b F_O Tuning Frequency Response (G_o constant : G_m varied)

Fig 5.7.2-1b also shows that the variation of F_O at higher frequencies varies Q in a non-linear manner, (ie $Q \neq Gm/2Go$), this is attributed to the finite bandwidth of the transconductance amplifiers causing a degree of Q-enhancement, an effect which is present in all active filter realisations.

Using this approach, a fully tunable, 2nd order bandpass filter with independent control of centre frequency and Q has been realised with only *two* OTA-C integrators.

5.7.3 Transfer Function Accuracy

The design of the fully tunable 2nd order bandpass filter is intended to be one section of a 12th order bandpass filter providing a Transitional Gaussian response centred at 60MHz. This class of filter is required to exhibit both accurate amplitude and group delay responses. The effects of finite excess phase in all active filter designs was explored in chapter three with a resulting specification on the required transfer function accuracy of a 2nd order bandpass filter. The amplitude and group delay responses of a 2nd order bandpass filter of Fig 5.7.1-1 using fully tunable integrators of Fig 5.6.1-1 is shown by Fig 5.7.3-1a & b.

As shown by Fig 5.7.3-1a & b the amplitude and group delay responses of the 2nd order bandpass filter are very closely matched to that of an ideal 2nd order response. To compare the differences more closely, the error between the two amplitude and group delay responses are shown by Fig 5.7.3-2a & b.

As shown by Fig 5.7.3-2a the highest amplitude error of 0.7% occurs at the extremes of frequency which is well within the acceptable error of 2.2% [chapter 3, 3.4.2]. In addition, the group delay is also with the required error, increasing only to a maximum of 3.5% at the extremes of frequency compared to an acceptable limit of 4.7% [chapter 3, 3.4.2].

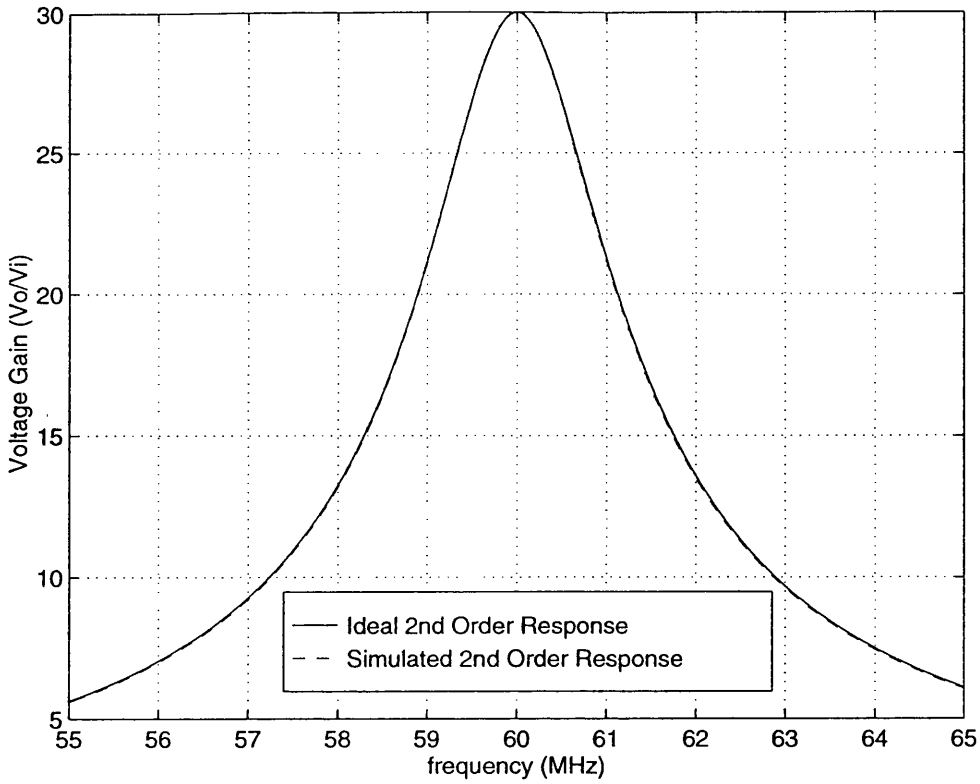


Fig 5.7.3-1a Amplitude Response of 2nd order bandpass Filter

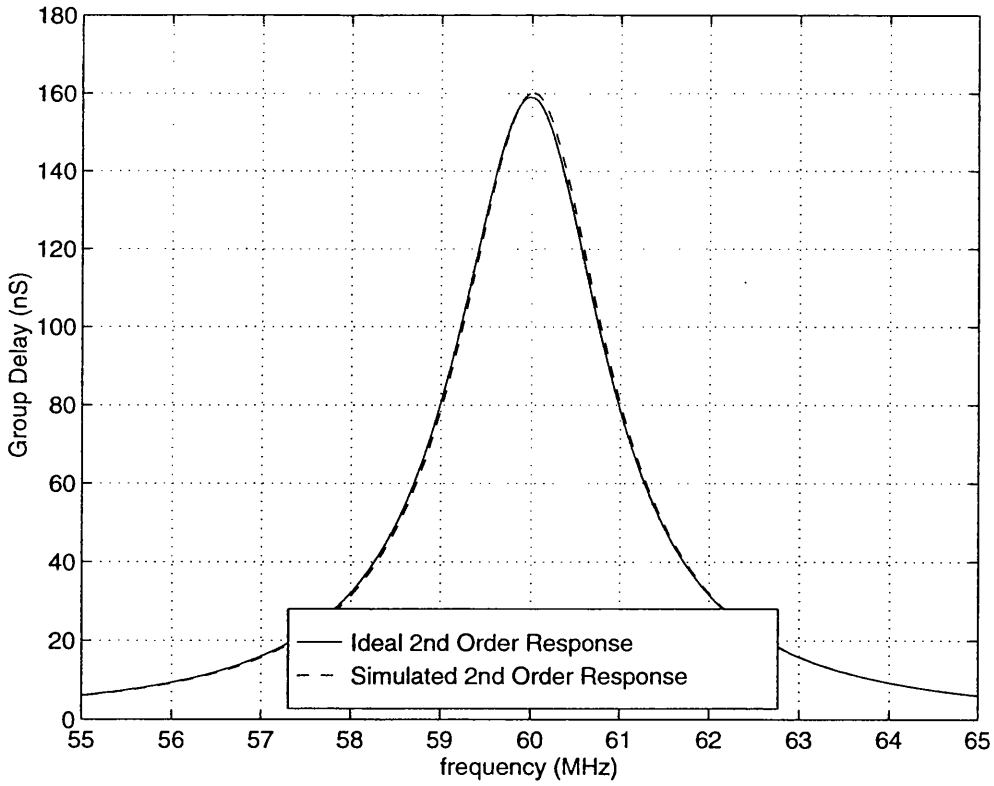


Fig 5.7.3-1b Group Delay Response of 2nd order bandpass Filter

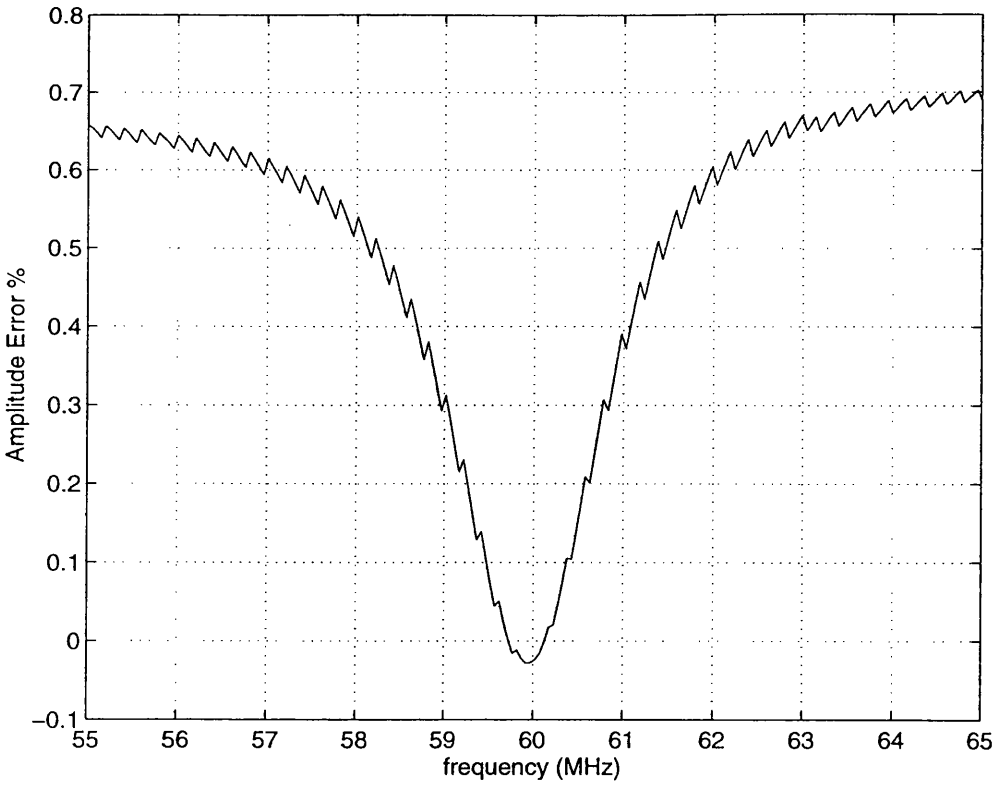


Fig 5.7.3-2a Error in Amplitude Response Compared to the Ideal

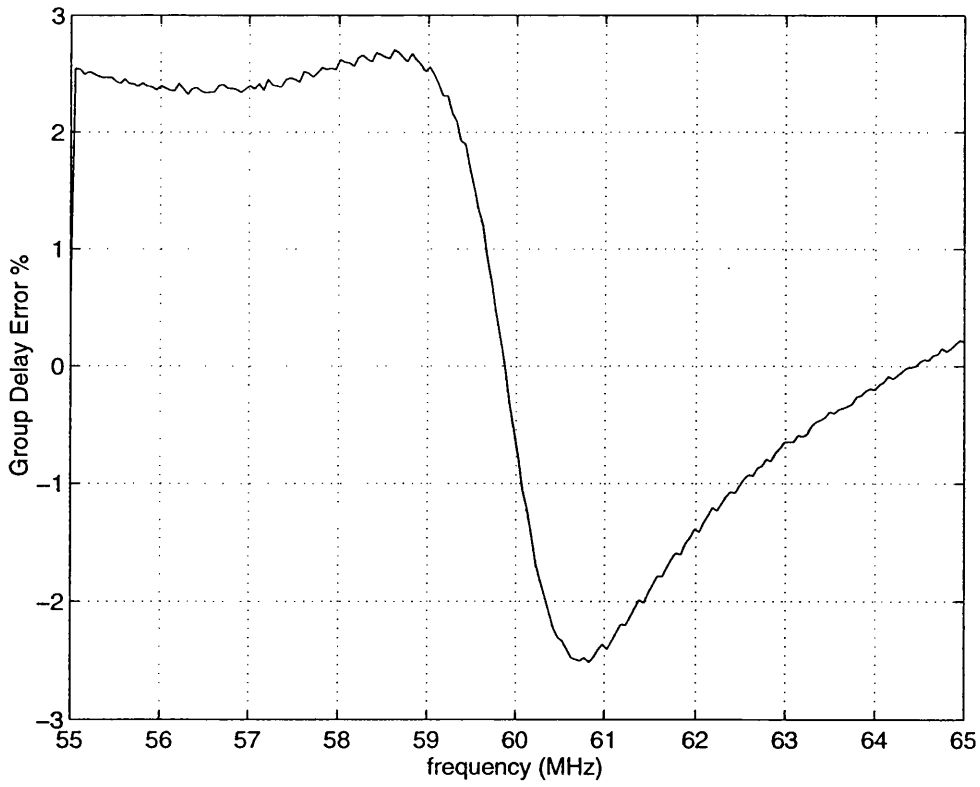


Fig 5.7.3-2b Error in Group Delay Response Compared to the Ideal

5.8 Conclusion

In this chapter the problems of designing high quality OTA-C integrators to be used to form bandpass filters has been reviewed. In addition, the restriction imposed on the design as a result of the use of the circuit simulator and the device model only compounds the problem.

A simulated design of a high quality OTA-C integrator implemented in GaAs MESFET technology which overcomes the difficulties that GaAs presents and in addition adheres to the self imposed restriction with one minor exception as a result of limited modelling data, has been presented.

This design represents the only OTA-C integrator realised to date, in GaAs MESFET technology with the use of a single geometry device, biased at a common operating point (with the exception of two triode devices) which is fully tunable. A novel method of variable voltage gain enhancement is presented without the reliance of early saturation techniques. In addition, independent transconductance tuning is presented without the need to alter DC bias conditions. This resulted in the realisation of a fully tunable 2nd order bandpass filter with only two OTA-C integrators.

The new 2nd order bandpass filter demonstrates independent centre frequency Fo and Q tuning. In addition, the simulated transfer function accuracy is within acceptable limits to facilitate the realisation of a 12th order Transitional Gaussian filter centred at 60MHz.

CHAPTER 6

Experimental Results of OTA-C Integrator and Bandpass Filter

6.1 Introduction

In this chapter the results of a set of fabricated fully tunable, single-ended OTA-C integrators and bandpass filters will be presented in order to evaluate the circuits design and tuning methods presented in chapter 5 of this thesis.

The full custom layout was designed using Silvar Lisco's 'Princess' system at UCL and fabricated in 0.5μm GaAs MESFET technology using the GEC-Marconi Materials Technology (Caswell) L20 Foundry Process [66]. The design of the evaluation printed circuit boards (PCB) and the bonding of the ICs where also undertaken at UCL.

In the following sections the test equipment used to evaluate the performance of the OTA-C integrator and the fully tunable bandpass filter are described separately.

6.2 Measured Performance of OTA-C Integrator

6.2.1 Single-Ended OTA-C Integrator

The fully tunable, single-ended OTA-C integrator presented in chapter five and shown in Fig 6.2.1-1 was fabricated using 0.5μm, -1v threshold, 20GHz f_t, GaAs MESFET technology with an integrating capacitor C_L chosen for a nominal unity gain frequency of 60MHz (C_L=4pF).

Although in theory the device widths can be scaled to any required value, they should be kept as small as possible in order to minimise power consumption. A device width of 20μm was used through out the design, which is the minimum width for which the foundry process is characterised. Fig 6.2.1-2a shows a photomicrograph of the die, which measures approximately 2mm x 1mm and Fig 6.2.1-2b shows the pin layout of the bonded IC.

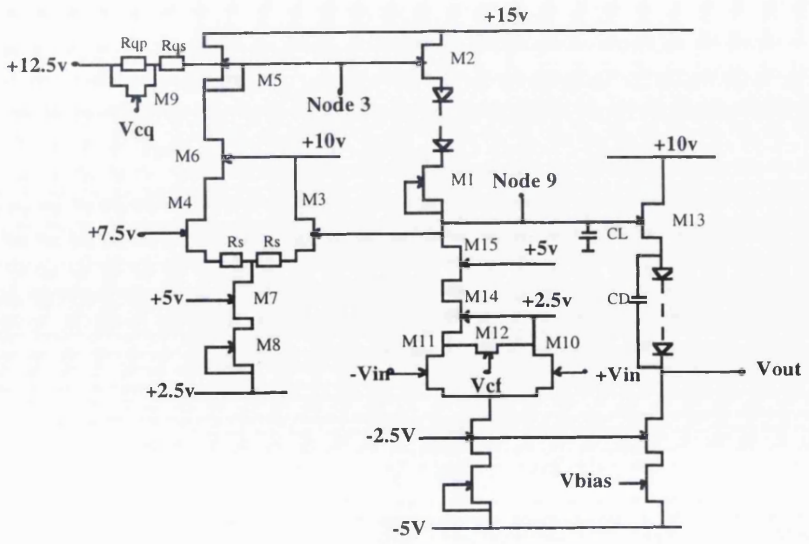


Fig 6.2.1-1 Complete Fully Tunable OTA-C Integrator with Independent Control of Gm and Go

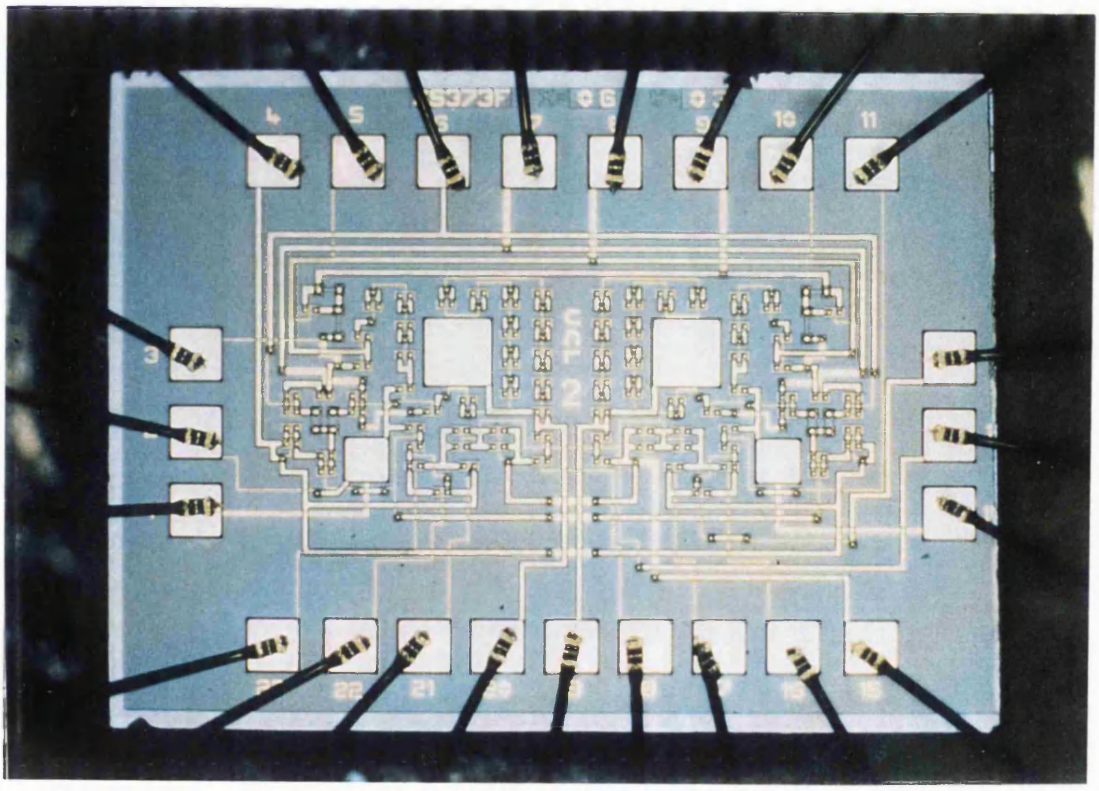


Fig 6.2.1-2a Photomicrograph of OTA-C Chip

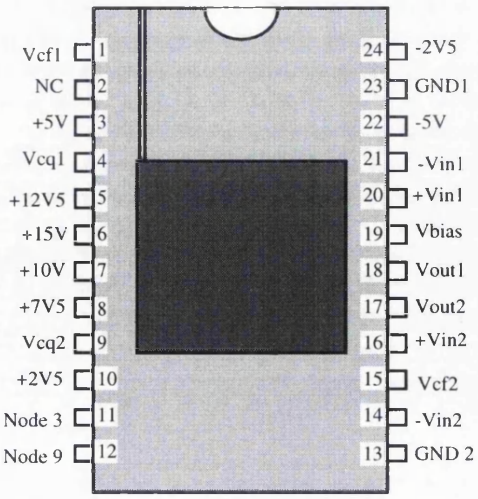


Fig 6.2.1-2b Pin Layout of Fabricated OTA-C Integrators

The chip contains two identical OTA-C integrators of the type shown in Fig 6.2.1-1. The two OTA-C integrators share common power supplies and the variable current source of the source followers is connected to one Vbias pad. The first (#1) OTA-C integrator is used to demonstrate the full high frequency tuning range that can be achieved by varying the transconductance gain Gm and the output conductance Go with regard to the unity gain frequency and low frequency gain respectively. The second (#2) OTA-C integrator has access to the high impedance nodes, shown on Fig 6.2.1-1 as nodes 3 and 9, allowing the DC voltages at these nodes to be set via Vbias, which in turn due to tracking, sets the DC voltages for the first OTA-C integrator. In addition, low frequency measurements of transconductance Gm at node (node 9) can also be carried out.

6.2.2 Experimental Evaluation Method

A purpose build test board was designed, layed out and built to evaluated the performance of the OTA-C integrators and is shown by Fig 6.2.2-1a and Fig 6.2.2-1b.

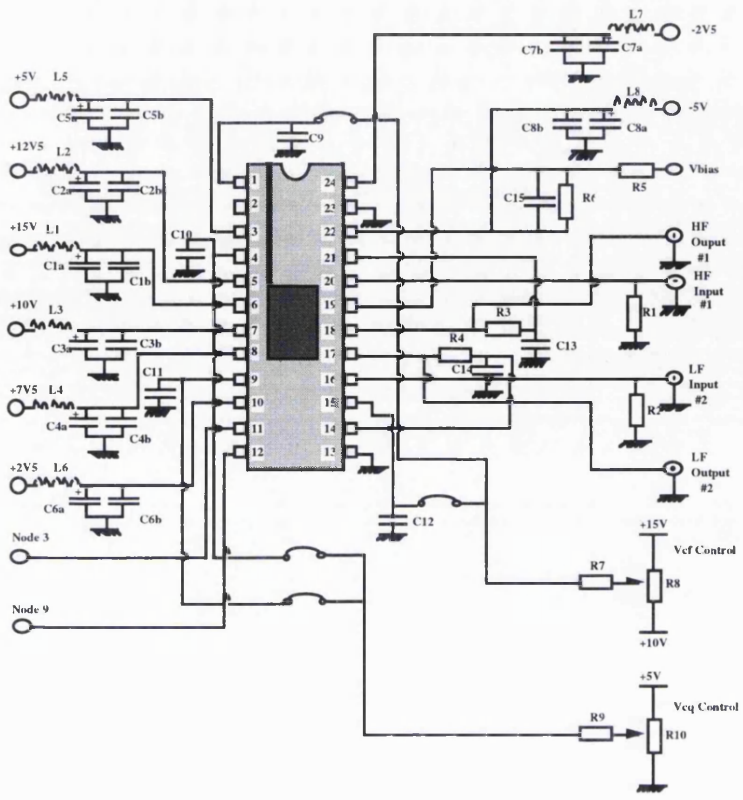


Fig 6.2.2-1a Purpose Build Test Board

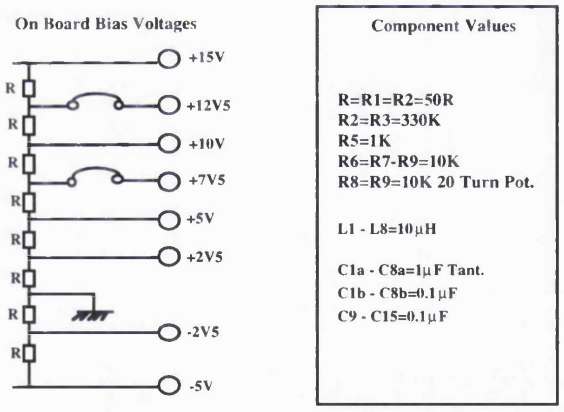


Fig 6.2.2-1b On Board Bias Voltages and Component Values

The purpose built test board was constructed using a 1.6mm double sided copper clad epoxy glass printed circuit board (PCB). The bottom layer connected the signal and power tracks, etched within an earth plane while the top layer, as far as possible maintained an unbroken earth plane. A simple resistor chain was used to provide the appropriate bias voltages, as shown by Fig 6.2.2-1b, with low values of resistance to maintain good

voltage regulation. Each power supply rail connected to the test IC was de-coupled via an LC network. A parallel combination of capacitors were used (ie C1a, C1b) to provide an enhanced broadband de-coupling. A large electrolytic capacitor was used to provide the low frequency de-coupling while a small surface mounted (SM) capacitor connected as close as possible to the appropriate pin provides the higher frequency de-coupling.

Linking options were also provided to isolate the control voltages which vary the transconductance gain Gm (Vcf) and the output conductance Go (Vcq) of each OTA-C integrator. The control voltages, Vcf and Vcq are provided by a potentiometer biased to the appropriate voltage sources. In addition, the +12.5V and +7.5V voltage rails which provide the correct bias conditions for the effective use of the variable gain bootstrap load, as shown by Fig 6.2.2-1a, may also be connected to an alternative power supply if found to be necessary.

The high frequency input port for the first integrator (#1) is provided by an SMA connector terminated with a 50Ω resistor as close as possible to the input pin of the IC. On board strip lines for the input and output ports were not used in favour of a simpler method of maintaining the track lengths as short as possible to prevent impedance mismatch. For convenience, the low frequency input and output ports of the second (#2) integrator were also provided with 50Ω SMA connectors, although this integrator would not be subjected to high frequency testing.

Both OTA-C integrators are DC stabilised by the application of negative DC feedback provided by the RC network formed by R3, C13, and R4, C14 as shown in Fig 6.2.2-1a. The feedback network has a low frequency pole at 5Hz, thus not affecting the integrator pole which is in the MHz region. The output offset null was achieved using a separate power supply connected to a resistive divider network with a ratio of 11:1, thus increasing the sensitivity by which Vbias can be controlled. A photograph of the purpose built test board is shown in Fig 6.2.2-2.

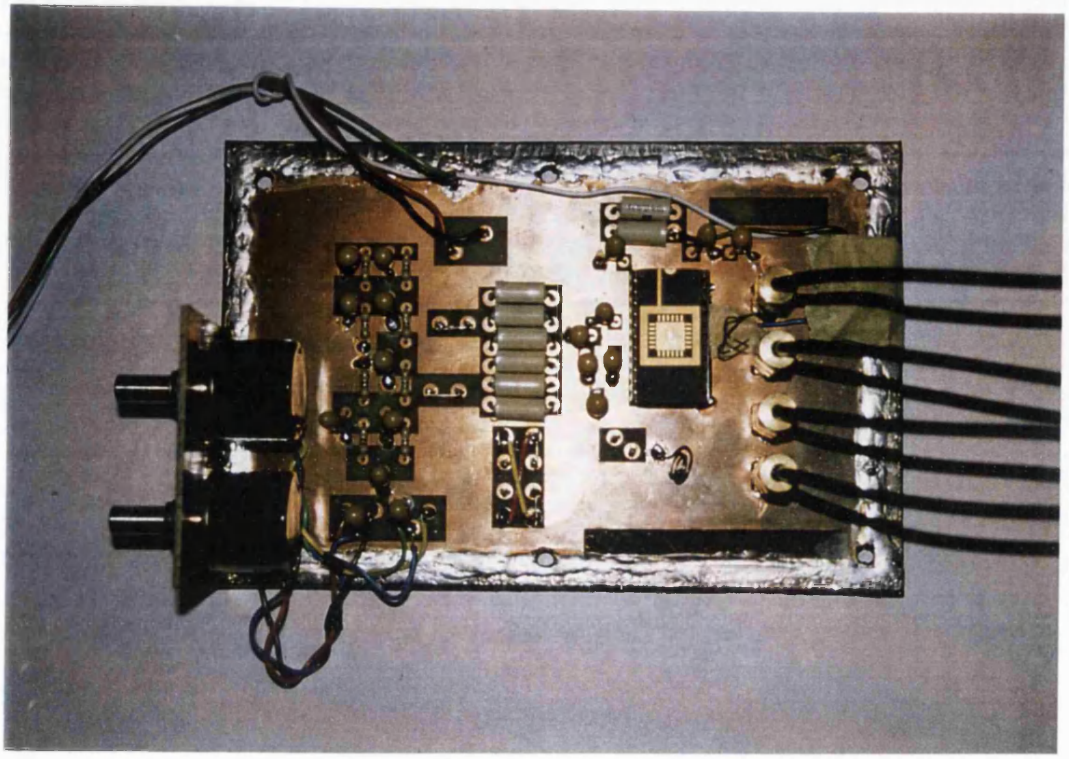


Fig 6.2.2-2 Photograph of Purpose Build Test Board with Test IC

The measurement apparatus for testing the performance of the OTA-C integrator is shown in Fig 6.2.2-3.

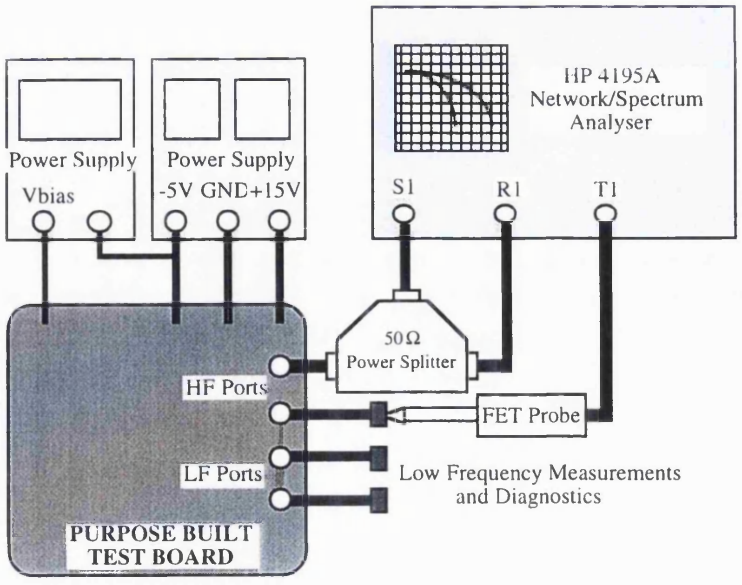


Fig 6.2.2-3 Measurement Apparatus For OTA-C Integrator Evaluation

A network/spectrum analyser (Hewlett Packard HP 4195A) was used to provide the sweeping source S1 which was applied to the OTA-C integrator under test from one port of a 50Ω power splitter (HP 11667A), the other port being applied to the reference input of the analyser R1. The output port of the OTA-C integrator under test was connected as close as possible (minimising impedance mismatch) to a high impedance FET probe (Tecktronic P6202A) which in turn was connected with the correct 50Ω impedance loading to the test input of the analyser T1. The low frequency OTA-C integrator (#2) ports were connected to low frequency diagnostic equipment for monitoring the DC bias conditions and for low frequency spectrum analysis.

The fabricated OTA-C integrators were designed to provide a low impedance output which presents the appropriate DC level shift and for ease of interconnection to form a cascaded high order filter. In addition the low impedance output port allows measurements to be made with a relatively high impedance, high frequency FET probe. Unfortunately at the frequencies of interest the probe exhibits a much lower (<1K) impedance relative to the OTA-C integrator output impedance (≈3K) which would cause the unity gain of the amplitude frequency response to occur at a lower defined frequency.

To overcome this problem, two uncommitted MESFETs (20μm and 40μm) were also fabricated which could be connected as a source follower and used to buffer the output of the OTA-C integrator to the FET probe as shown by Fig 6.2.2-4a, thus the FET probe would be connected to a source impedance of approximately 250Ω (1/gm).

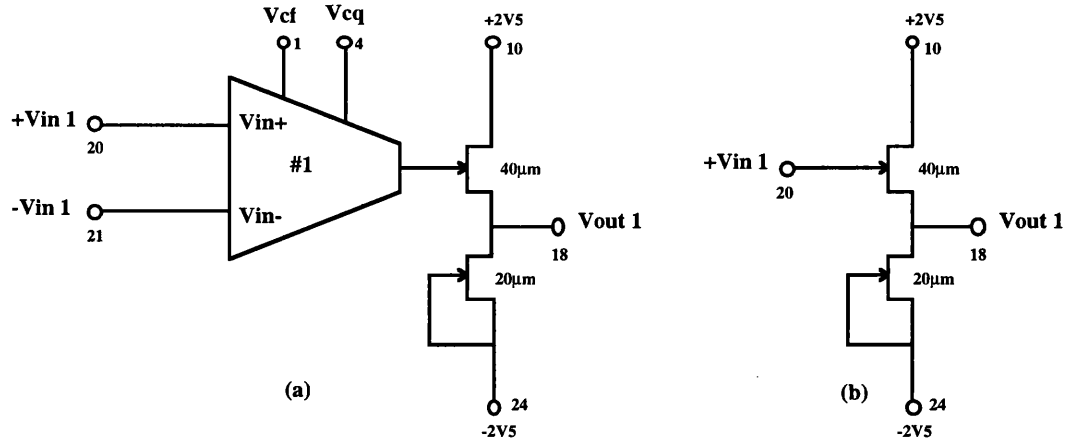


Fig 6.2.2-4 (a) OTA-C Integrator with Output Buffer
(b) Packaged Output Buffer for Calibration

In addition, another source follower output buffer was mounted in the same IC package as the OTA-C integrators. By sweeping over the required frequency range used for AC measurements, the measurement apparatus shown in Fig 6.2.2-3, including the purpose built test board and output buffer connected to the FET probe, were calibrated as shown in Fig 6.2.2-5a and b.

Once the correction for the measurement apparatus has been performed, the equipment used including the cables, FET probes and analyser setting must not be altered to make correct OTA-C integrator frequency measurements.

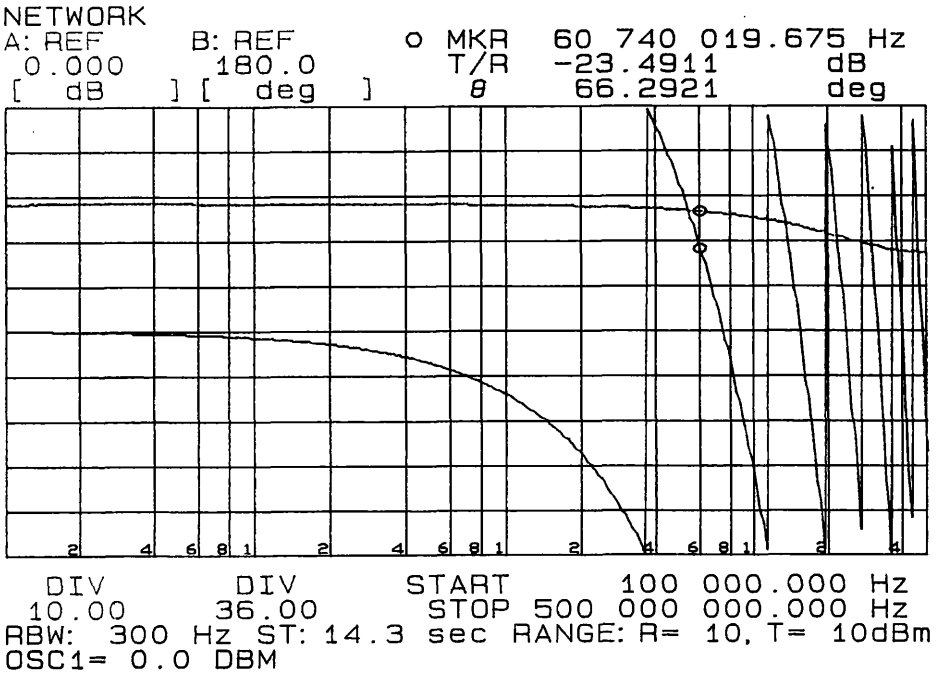


Fig 6.2.2-5a Frequency and Phase Response of Test Board and Output Buffer

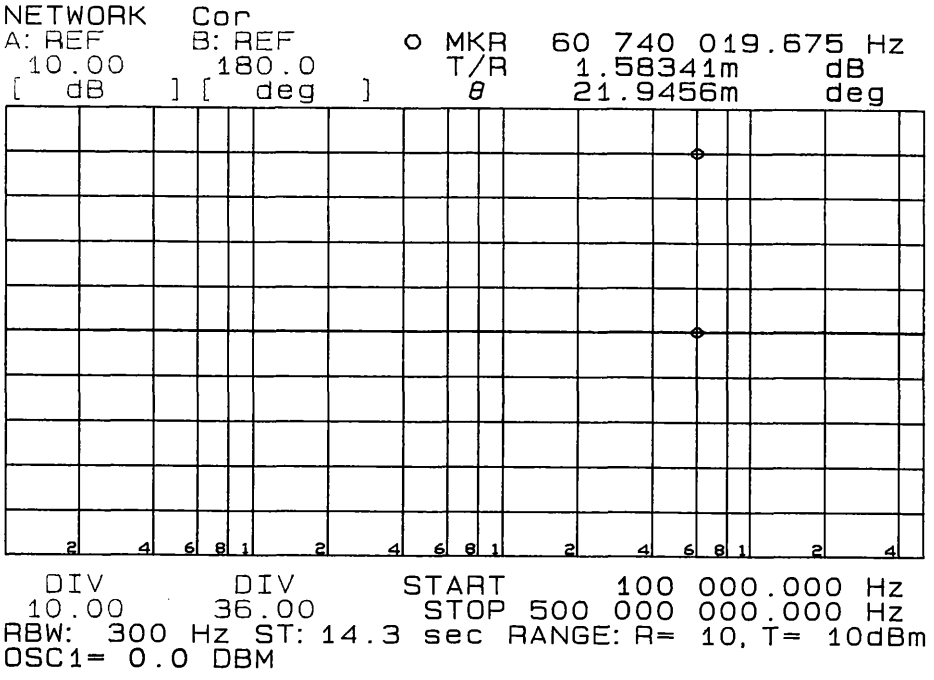


Fig 6.2.2-5b Frequency and Phase Response after calibration of Test Board and Output Buffer

6.2.3 Integrator Frequency Response Measurements

The forward transconductance gain, Gm of the OTA-C integrator was measured as a function of applied input voltage. This was achieved by using the second integrator, #2 on the chip, which has the transconductance point pinned out as node 9, shown on Fig 6.2.1-1 and connected to the appropriate power rail by means of a 56Ω resistor. Since the impedance at the transconductance point is much greater than 56Ω, the voltage across the resistor gives an accurate measure of the short circuit output current of the OTA. A frequency response measurement was made of Gm tuning range and is shown by Fig 6.2.3-1. For this measurement the calibration correction was not used, two FET probes were used to make a relative measurement between the input port (R1) and node 9 loaded with 56Ω (T1).

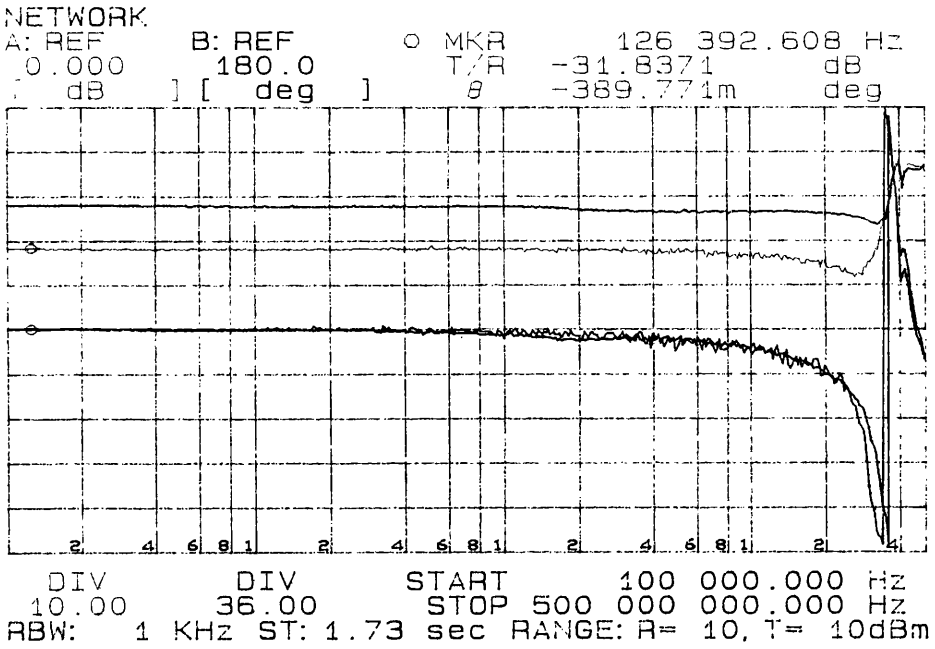


Fig 6.2.3-1 Gm Measurement, Frequency Response and Tuning Range

The frequency response of the Gm phase reaches -180° at 380MHz. The simulated Gm frequency response indicates that OTA has a high frequency pole at 14GHz. Therefore the phase shifts encountered are due to cable path length differences.

The test revealed that Gm could be varied in the range 0.45mS to 1.37mS, a tuning range of 67% (9.8dB) which should be compared to the range predicted by SPICE of 1.3mS to 2mS. The larger measured tuning range is attributable to a wider variation in the drain conductance of the 20μm x 0.5μm foundry GaAs MESFET as a function of Vgs in its linear region than that for the model. The difference of -31% in the measured maximum Gm, combined with the ±20% absolute foundry tolerance of C_L indicate that the measured maximum unity gain frequency of the OTA-C integrator would be between 45MHz to 68MHz.

The measured frequency response of the OTA-C integrator (#1) with C_L set at 4pF for a nominal unity gain frequency of 60MHz was presented in [101,102] and shown in Figs 6.2.3-2a and b. In Fig 6.2.3-2a, Go is varied across its full range while Gm is held constant at its maximum value. As indicated by the Gm measurements of Fig 6.2.3-1, the unity gain frequency is lower than expected. The Go variation causes the low frequency gain to vary from 33dB to 41dB without altering the unity gain frequency, which remains constant at its maximum value of 48MHz. This compares very favourably with the simulated low frequency gain range of 34dB to 37dB as presented in chapter 5 section 5.6.2.

In Fig 6.2.3-2b, Gm is varied across its full range, while Go is adjusted to maintain a constant low frequency gain of 33dB. The resulting tuning range of the unity gain frequency is 18MHz to 48MHz, which corresponds to the measured Gm tuning range, but differs from the SPICE predictions.

The considerable difference in the measured maximum unity gain frequency (-39%) of the integrator is attributable to the device gm (and hence OTA Gm) being lower than predicted by the model data. This arose because the circuit design was carried out in parallel with significant extensions to the foundry process. Certain modelling information supplied for circuit design and simulation purposes did not relate to the version of the process actually employed for the IC fabrication.

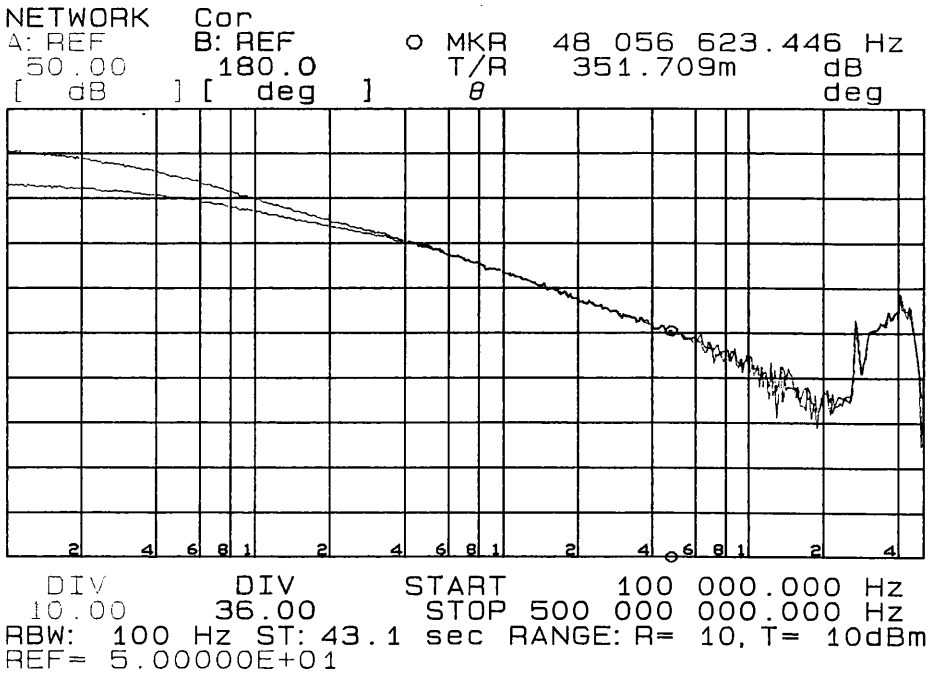


Fig 6.2.3-2a Amplitude Response of OTA-C Integrator
(Gm constant, Go varied)

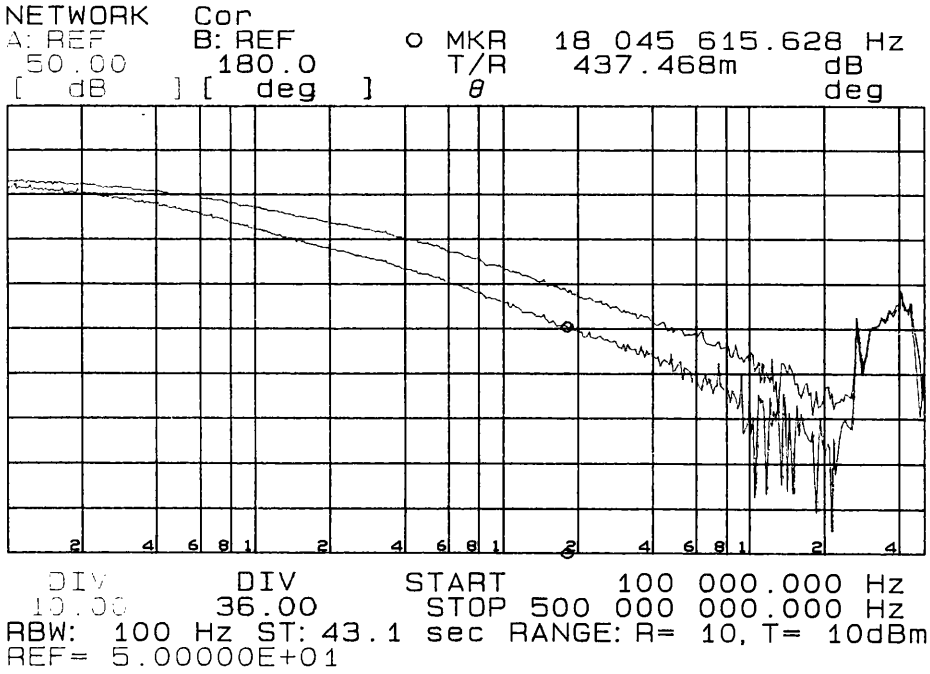


Fig 6.2.3-2b Amplitude Response of OTA-C Integrator
(Gm varied, Gm/Go constant)

In all other respects, the new method of independently tuning the unity gain frequency (Gm) with respect to the low frequency gain (Go) is proven.

6.2.4 Integrator Distortion Measurements

The harmonic distortion measurements were carried out on the second OTA-C integrator (#2) which enabled access to the transconductance point (node 9) of the IC. The reference signal was provided by an external source (HP 3325B Function Generator) while the output of the OTA-C integrator was applied to the spectrum analyser (HP 4195A). All the measurements were carried out at a frequency of 100KHz, the relatively low frequency being chosen to avoid attenuation of the harmonics by the integrating action of the circuit.

In order to determine if the output buffer introduced any significant distortion, an input signal of 1.2Vp-p was applied at 100KHz. The output spectrum of the buffer is shown by Fig 6.2.4-1 indicating a 2nd harmonic of -61.7dB.

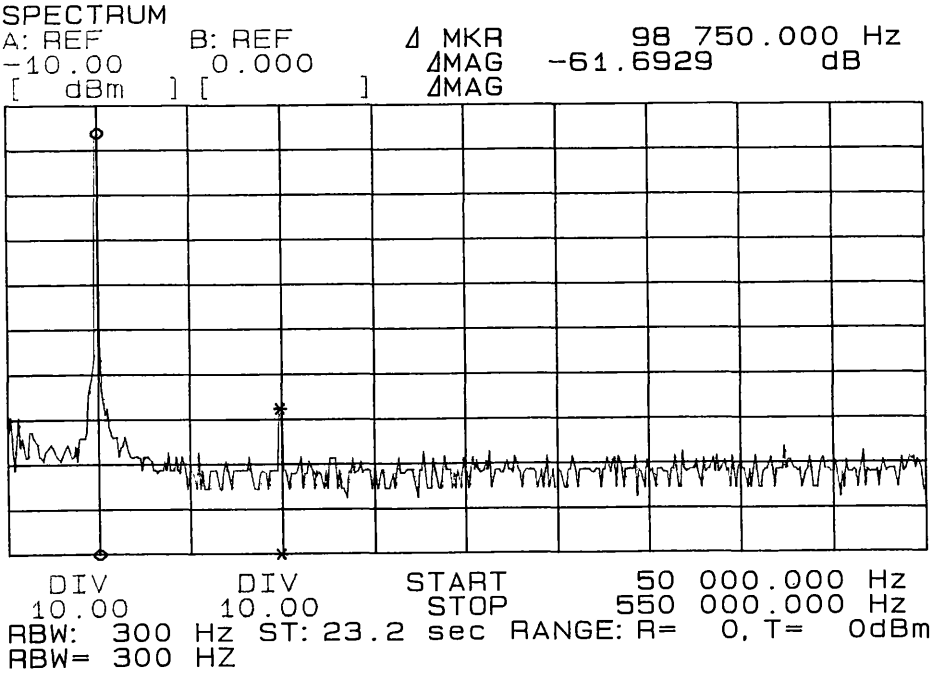


Fig 6.2.3-2b Output Spectrum of Output Buffer Subjected with an Input Signal of 1.2Vp-p

In assessing the total harmonic distortion (THD) of an OTA-C integrator, a method presented in chapter 5, section 5.6.3 was used. This comprehensive distortion test consists of the following set of *three* measurements of the output in response to a sinusoidal input:

(1) Short circuit output current ('S/C');
(2) Output voltage with a resistive load of 1/Gm ('1/Gm');
(3) Output voltage with load open circuit ('O/C')

Measure (1) is the traditional method of measuring the harmonic purity of the short circuit output current in response to a sinusoidal input voltage. This was achieved by connecting a 56Ω resistor to node 9 and the appropriate voltage rail and measuring the spectral *voltage* output at node 9. In measure (2) the OTA-C integrator load capacitor connected at node 9 was shunted with a variable resistive load and adjusted to the value of Gm, thus equal to the modulus of the load impedance of an OTA-C integrator at its unity gain frequency. The voltage output (Vout) was applied to the spectrum analyser. Measure (3) represents an extreme test in which the OTA-C integrator is effectively employed as a voltage amplifier with Go serving as load and as in (2) the voltage output (Vout) was applied to the spectrum analyser. The combination of these measurements gives a comprehensive indication of the performance of the OTA under a wide variety of operating conditions.

The THD measured results are presented in Tables 6.2.4-1 and 6.2.4-2. For convenience, the simulated THD levels from chapters 5 are represented for comparison. These compare the simulated and measured THD levels at maximum and minimum Gm. For the S/C and 1/Gm tests, sinusoidal input voltages of 500mV (peak) and 100mV (peak) were applied. The measured THD levels show good agreement with the SPICE simulation. The measured THD levels are small for the 100mV input (sometimes approaching the noise floor of the spectrum analyser, as indicated in the tables) but considerably higher (up to about 5%) for a peak input voltage

level of 500mV. These relatively high distortion levels are to be expected [88,97] since in this case the peak-to-peak input signal level (1V) approaches the 1-volt threshold of the MESFETs used in the OTA-C integrator.

	Simulated Fully-Balanced THD (%)		Simulated Single-Ended THD (%)		Measured Single-Ended THD (%)	
	V=500mV (pk)	V=100mV (pk)	V=500mV (pk)	V=100mV (pk)	V=500mV (pk)	V=100mV (pk)
S/C test	1.05	0.03	1.4	0.3	1.9	<0.5
1/Gm test	0.64	0.02	1.3	0.2	1.7	0.1
O/C test	0.06	0.02	2.4	0.5	2.5	<0.3

Table 6.2.4-1 OTA THD at Maximum Gm (f=100KHz, Vcf-2.5V=-1v)

	Simulated Fully-Balanced THD (%)		Simulated Single-Ended THD (%)		Measured Single-Ended THD (%)	
	V=500mV (pk)	V=100mV (pk)	V=500mV (pk)	V=100mV (pk)	V=500mV (pk)	V=100mV (pk)
S/C test	3.58	0.23	4.2	0.2	3.5	<0.5
1/Gm test	4.30	0.26	4.0	0.2	3.3	0.4
O/C test	0.40	0.12	12.7	2.3	14.6	3.5

Table 6.2.4-2 OTA THD at Minimum Gm (f=100KHz, Vcf-2.5V=0.6v)

The purpose of the third (O/C) test is to investigate the performance of the OTA effectively employed as a voltage amplifier. For this test, Gm/Go was set to 30dB and the sinusoidal input signal level adjusted to provide *output* levels of 100mV (peak) and 500mV (peak). The resulting THD levels at the chosen Gm tuning points are given in the Tables, Go being adjusted in each case to provide the same voltage gain (Gm/Go) for each Gm setting. The results follow the pattern set by the other two tests, ie., the measured and simulated values are similar, with the measured values being consistently slightly larger than those predicted by the SPICE simulation.

In summary, the overall THD levels of the OTA, measured under a variety of conditions, are quite moderate. If the peak signal level (input for tests 1 & 2, output for test 3) is restricted to 100mV (peak), the THD levels are in most cases on the order of 1%. On the other hand, larger signal levels produce quite high levels of THD, about 10% in some cases. If required, these levels can be reduced by employing source degeneration in the OTA. Alternatively, the use of the fully balanced version of the OTA described in chapter 5, section 5.5 provides a more comprehensive solution to the reduction of THD levels.

6.3 Measured Performance of Bandpass Filter

6.3.1 2nd Order CT Bandpass Filter

A fully tunable, 2nd order, state variable bandpass filter has been fabricated using single-ended OTA-C integrators of the type described in chapter 5. The filter architecture is shown in Fig 6.3.1-1 and consists of *two* OTA-C integrators of the type described above.

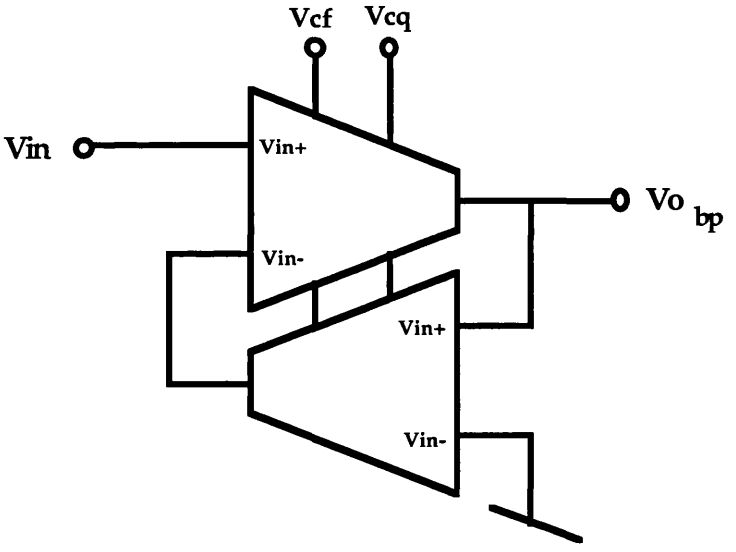


Fig 6.3.1-1 Fully Tunable 2nd Order Bandpass Filter

The filter was designed for a nominal centre frequency of 60MHz and a nominal Q of 30 and fabricated in the same 0.5μm GaAs MESFET technology as the OTA-C integrators described above with the exception that all internal high impedance nodes (ie nodes 3 and 9) are *not* pinned out and the triode

region devices, M9 and M12 are doubled in size (two connected in parallel) to increase the tuning range of the Q and centre frequency respectively. A photomicrograph of the die is shown in Fig 6.3.1-2a, which measures approximately 2mm X 1mm and Fig 6.3.1-2b shows the pin layout of the bonded IC.

The filter chip is identical in layout to the OTA-C integrator chip with the exception that two integrators are internally configured as a 2nd order bandpass filter. The two OTA-C integrators share common power supplies and the source follower variable current source is commonly controlled by one Vbias node for DC output offset nulling. In addition, the transconductance, Gm and output conductance, Go control nodes (Vcf and Vcq) of each OTA-C integrator are internally connected and biased off chip.

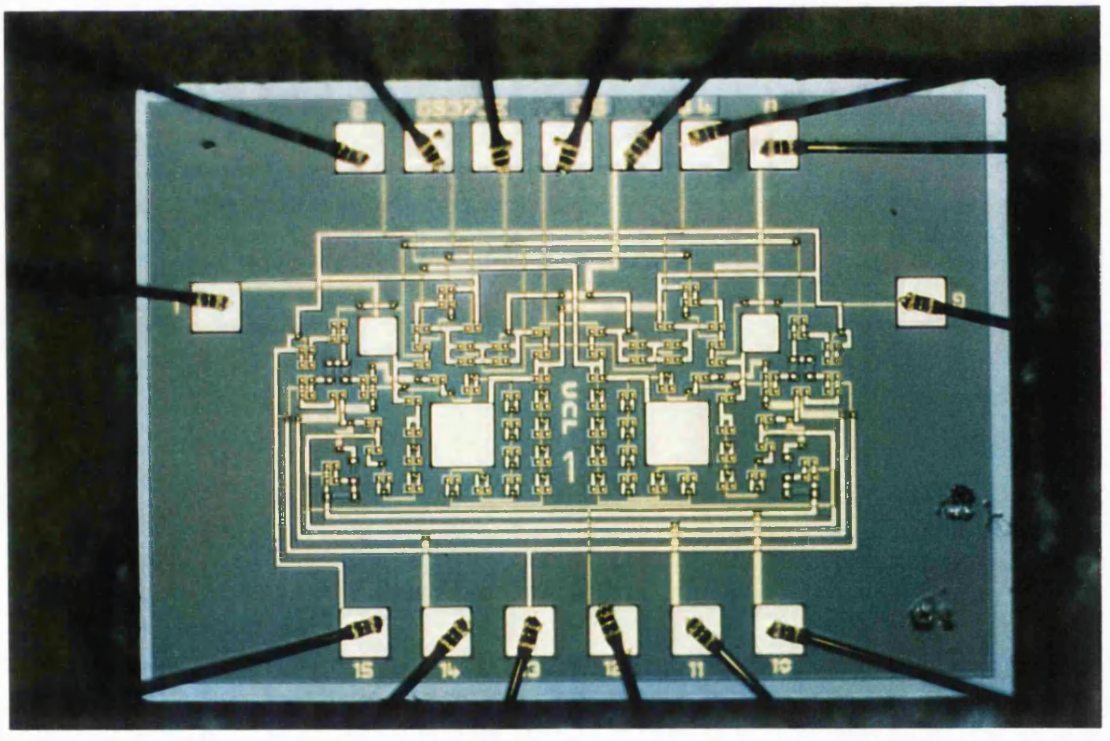


Fig 6.3.1-2a Photomicrograph of the Fully Tunable 2nd Order Bandpass Filter Chip

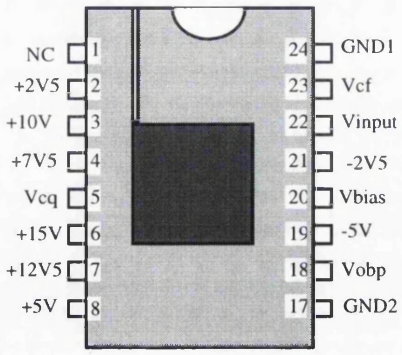


Fig 6.3.1-2b Pin Layout of Fabricated 2nd Order Bandpass Filter

6.3.2 Experimental Evaluation Method

A second purpose built test board was designed, layed out and built to evaluate the performance of the bandpass filter and it is shown by Fig 6.3.2-1.

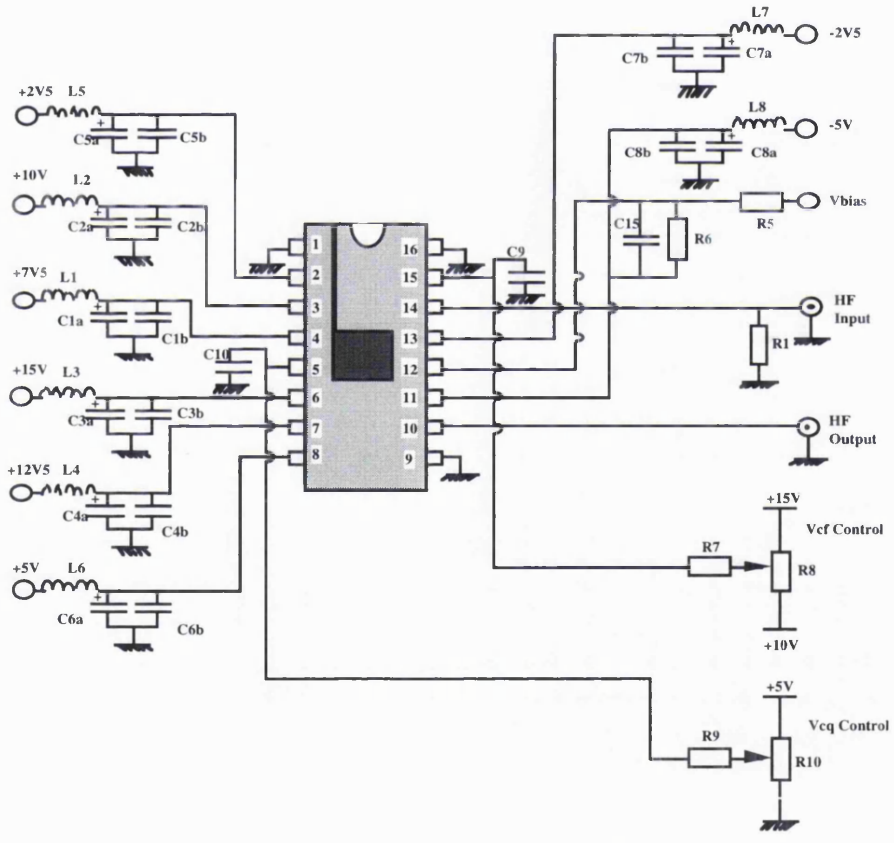


Fig 6.3.2-1 Purpose Built Test Board

The purpose built test board used to evaluate the bandpass response of the filter chip was designed and constructed in the same manner as the test

board for the OTA-C integrators (section 6.2.2). The simple resistor chain and component values shown in Fig 6.2.2-1b were used to provide the appropriate bias voltages required for the OTA-C integrators. The linking options provided for the +12.5V and +7.5V voltage rails were also repeated for this test board which may be sourced to an independent voltage source, but this was found to be unnecessary from the evaluation of the OTA-C integrators of section 6.2.

The high frequency input port for the bandpass filter is provided by an SMA connector terminated with a 50Ω resistor as close as possible to the input pin of the IC. On board strip lines for the input and output ports were not used in favour a simpler method of maintaining the track lengths as short as possible to prevent impedance mismatch. The output offset null was achieved using a separate power supply connected to a resistive divider network with a ratio of 11:1, thus increasing the sensitivity by which Vbias can be controlled. A photograph of the purpose build test board is shown in Fig 6.3.2-2.

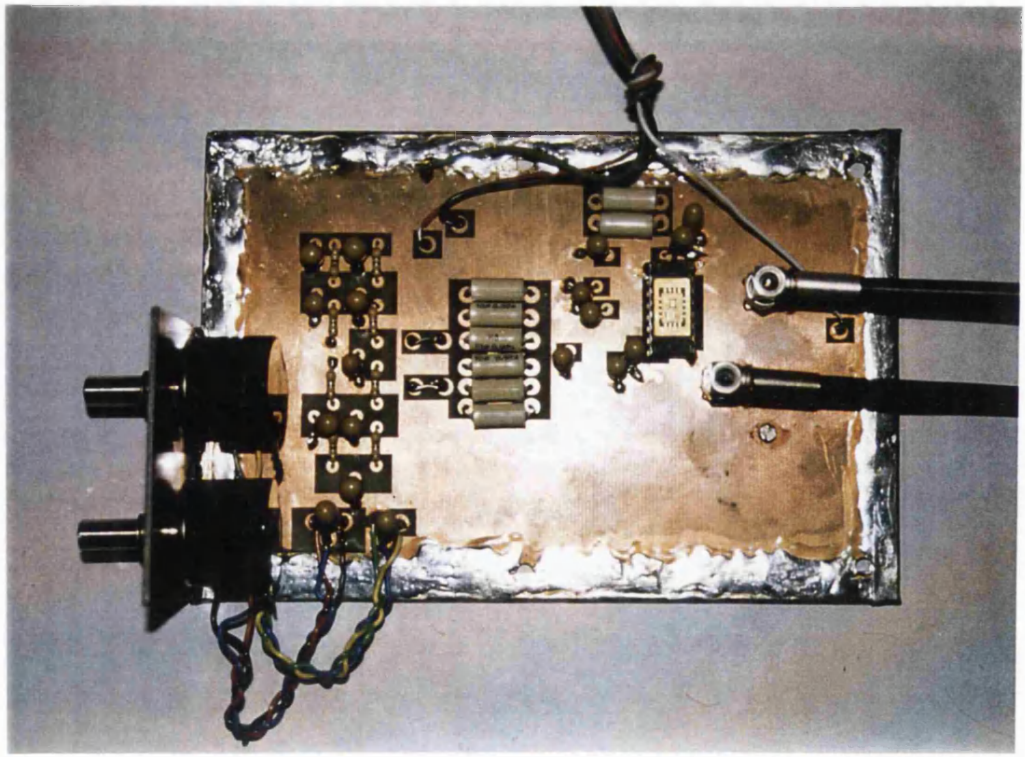


Fig 6.3.2-2 Photograph of Purpose Build Test Board with Test IC

The measurement apparatus for testing the performance of the 2nd Order bandpass filter is shown in Fig 6.3.2-3.

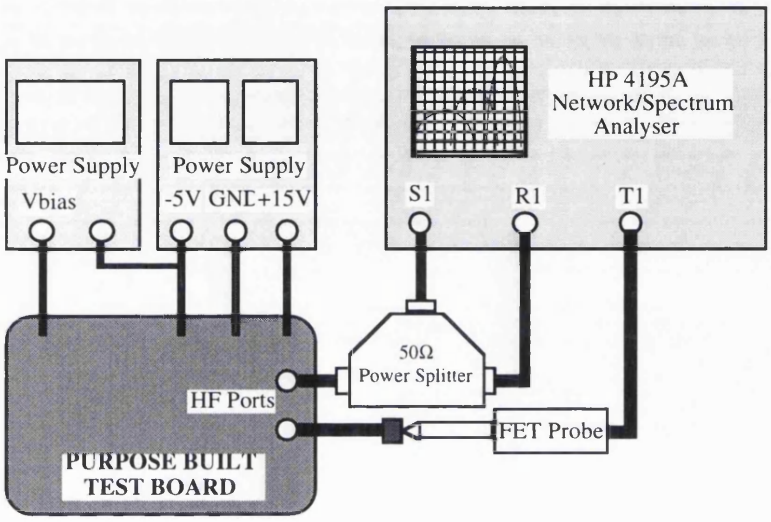


Fig 6.3.2-3 Measurement Apparatus For 2nd Order Bandpass Filter Evaluation

The network/spectrum analyser (Hewlett Packard HP 4195A) was used to provide the sweeping source S1 which was applied to the bandpass filter under test from one port of a 50Ω power splitter (HP 11667A), the other port being applied to the reference input of the analyser R1. The output port of the bandpass filter was connected as close as possible (minimising impedance mismatch) to a high impedance FET probe (Tecktronix P6202A) which in turn was connected with the correct 50Ω impedance loading to the test input of the analyser T1.

Unfortunately, the bandpass filter encountered a similar problem as the OTA-C integrator when connected to the FET probe. For the evaluation of the OTA-C integrators, the much lower (<1K) impedance of the FET probe relative to the integrator output impedance (≈3K) caused the unity gain of the amplitude frequency response to occur at a lower prescribed frequency. When evaluating the bandpass filter response, the effective loading of the FET capacitance (≈4pF) would cause the centre frequency of the filter to occur at a lower than prescribed frequency. The solution to this problem, as in the

case of the OTA-C integrator amplitude response, was to buffer the output of the bandpass filter to the FET probe using the fabricated, uncommitted MESFETs (20μm and 40μm) connected as a source follower as shown by Fig 6.3.2-4a. The buffer provides an input impedance of approximately 20fF to the bandpass filter, while the FET probe would be connected to an impedance of approximately 250Ω (1/gm).

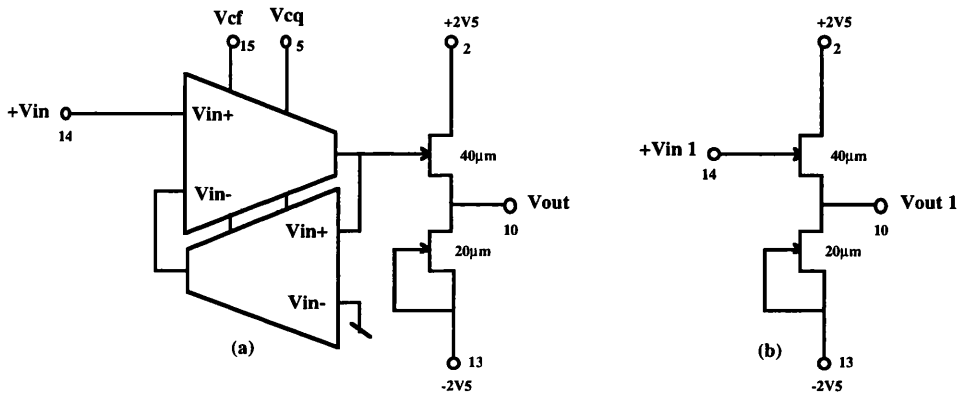


Fig 6.3.2-4 (a) Bandpass Filter with Output Buffer
(b) Packaged Output Buffer for Calibration

A second source follower buffer was mounted in the same IC package as the bandpass filter. By sweeping over the required frequency range used for AC measurements, the measurement apparatus shown by Fig 6.3.2-3, including the purpose built test board and output buffer connected to the FET probe, were calibrated and corrected as shown in Fig 6.3.2-5a and b.

Once the correction for the measurement apparatus has been performed, the equipment used including the cables, FET probes and analyser setting must not be altered to maintain accuracy of measurements.

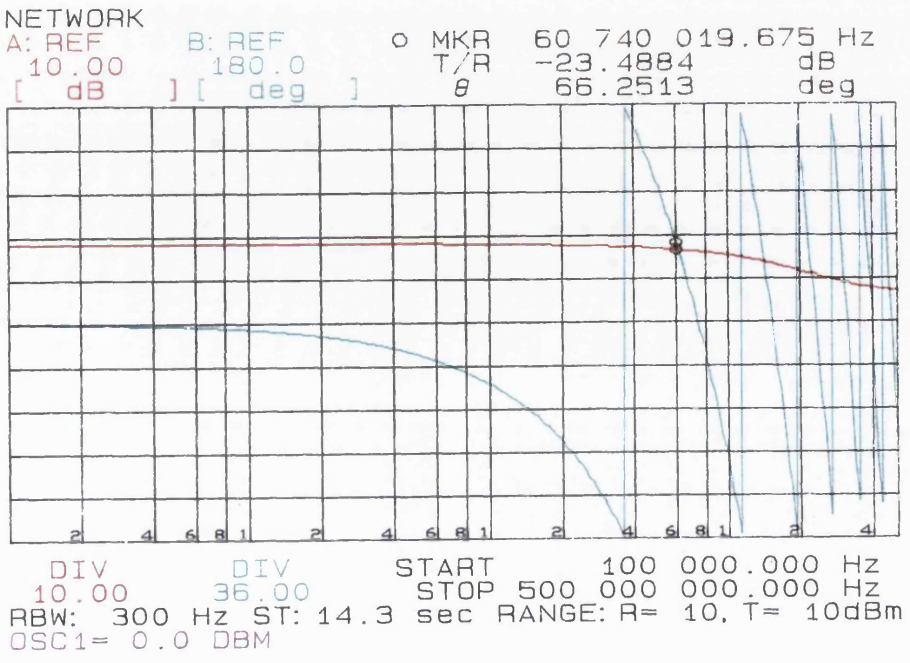


Fig 6.3.2-5a Frequency and Phase Response of Test Board and Output Buffer

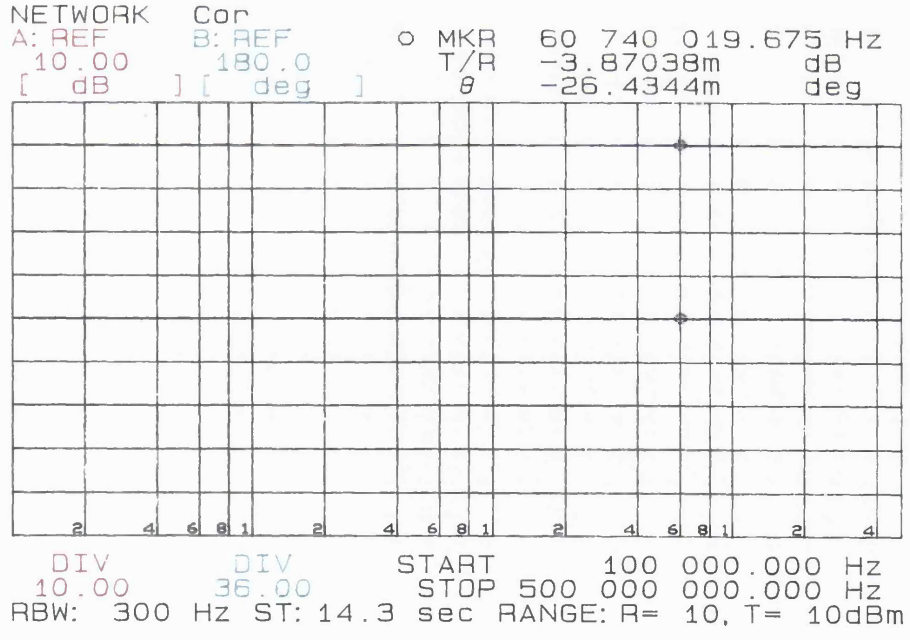


Fig 6.3.2-5b Frequency and Phase Response after calibration of Test Board and Output Buffer

6.3.3 Bandpass Filter Frequency Response Measurements

The measured frequency response of the 2nd order bandpass filter was presented in [103,104] and shown in Figs 6.3.3-1a and b.

In Fig 6.3.3-1a, the transconductance, Gm of the two OTA-C integrators are varied across its full range while Go is held constant. As indicated in section 6.2.3, the measured value of transconductance, Gm of the OTA was lower than predicted by SPICE which in turn demonstrated a correspondingly lower value of unity gain frequency of the OTA-C integrator. As such, the 2nd order bandpass filter exhibited a lower maximum centre frequency at 49MHz. The Gm tuning, however was able to vary the centre frequency, Fo (where $Fo=Gm/2\pi C_L$) from 11MHz to 50MHz, which represents a ±60% variation. The lower value of centre frequency is almost half the value of the lower unity gain frequency of the OTA-C integrator, which is a result of using two tuning devices (M12) connected in parallel. In addition, since the Q of the bandpass filter is dependent upon both Gm and Go (Q=Gm/Go), Q varies as the centre frequency is tuned through its range.

In Fig 6.3.3-1b, the centre frequency was adjusted to approximately the centre of its tuning range while Go is varied to demonstrate Q variation. By maintaining Gm constant for a centre frequency of 28MHz, any variation in centre frequency while tuning for Q would be observed. A Q variation of 4 to 60 shown in Fig 6.3.3-1b was achieved which represents a tuning range of ±87% with only minimal variation in centre frequency. Although the maximum value of Q shown is 60, higher values are obtainable since Go may be tuned to give a negative conductance. While tuning Q manually (ie open loop) maintaining precise control of Q with Q in excess of 100 was difficult.

In all other respects, the new method of independently controlling the centre frequency and Q of the bandpass filter using only two OTA-C integrators is proven.

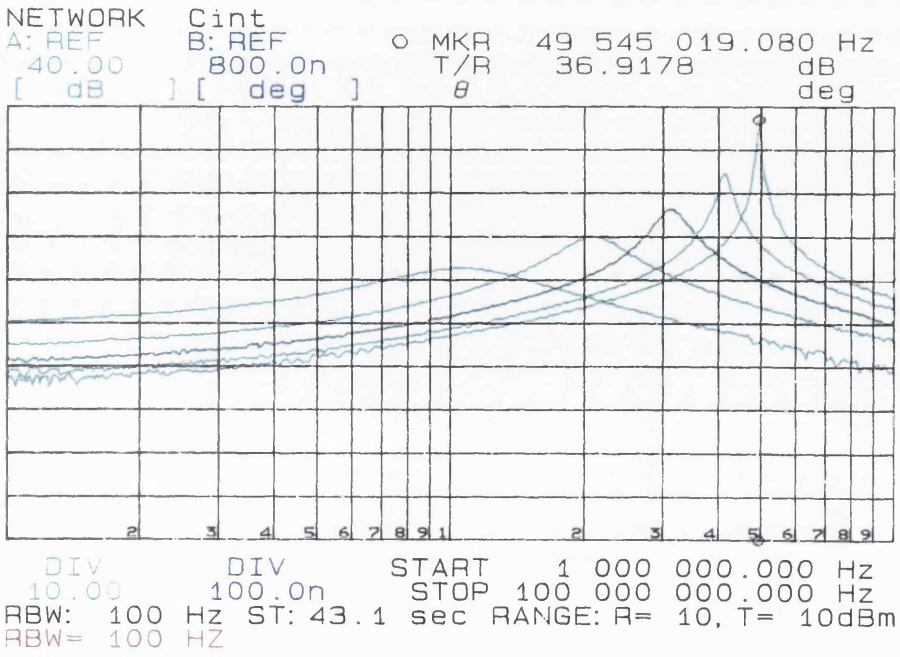


Fig 6.3.3-1a Amplitude Response of 2nd Order Bandpass Filter
(Gm varied, Go constant)

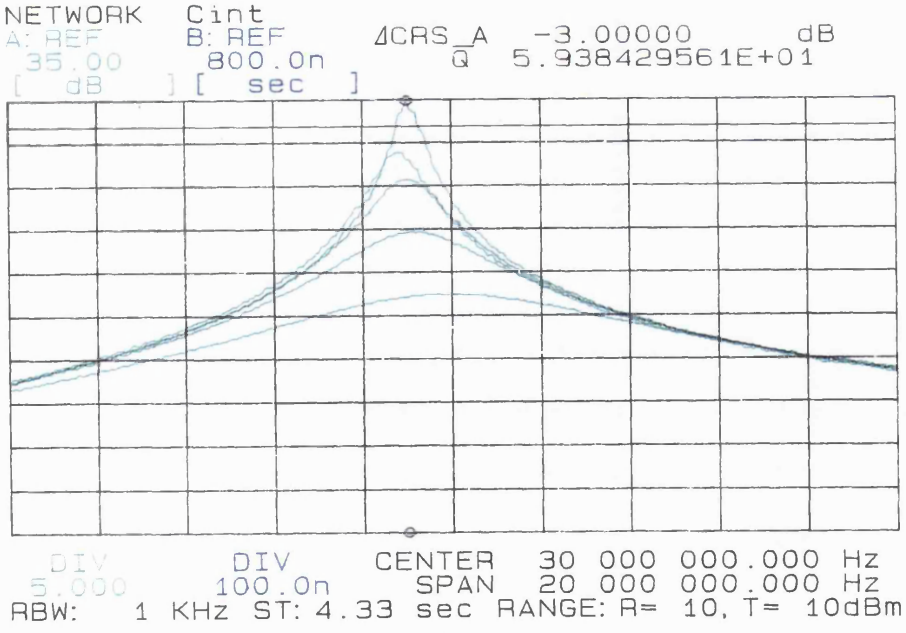


Fig 6.3.3-1b Amplitude Response of 2nd Order Bandpass Filter
(Gm constant, Go varied)

6.3.4 Intermodulation Distortion Measurements (IMD)

For this measurement a pair of tones of equal amplitude were applied to the filter in its passband, one tone at the centre frequency (Fo) and the other at the lower -3dB frequency (f1). The output harmonic for the IMD measurement purpose was the signal appearing at the upper -3dB frequency, at a frequency 2Fo-f1. Two separate sets of IMD measurements were carried out. In the first case, the amplitude of the output voltage for the fundamental to have an IMD of 1% (-43dB ie -40dB-3dB) was found as a function of Q . For this test, Q was varied in the range 4 to 60, while the centre frequency was held constant at a value close to the centre of its range (30MHz). For the second test, Q was held constant in the middle of its range (30) while Fo was varied in the range 12 to 50MHz. The results of these measurements are plotted in Fig 6.3.4-1a & Fig 6.3.4-1b.

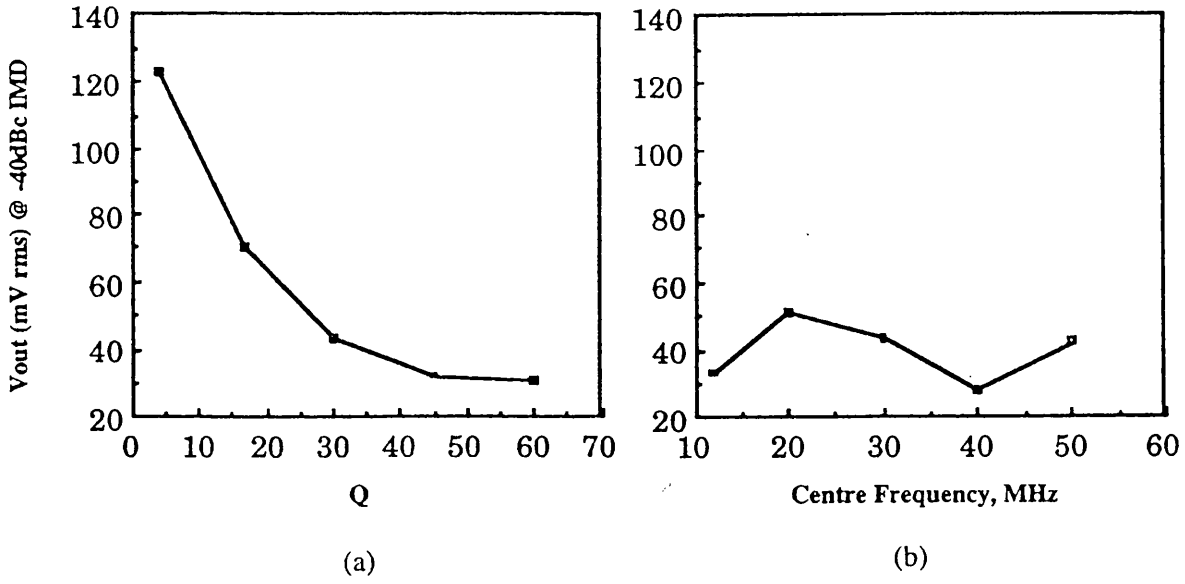


Fig 6.3.4-1 (a) IMD Measurements with Fo constant, Q variable
(b) IMD Measurements with Fo variable, Q constant

In the first case (Fig 6.3.4-1a), the signal handling capacity decreases rapidity with increasing Q as expected [47], while in the second case (Fig 6.3.4-1b), the signal-handling capacity is relatively independent of the bandpass centre frequency. If a larger signal handling capacity is required, the single-ended OTA-C integrator which forms the basis for the filter described in chapter 5 may be adapted very efficiently to a fully balanced version as illustrated in chapter 5 section 5.5, which may form a fully balanced tunable bandpass filter.

6.3.5 Transfer Function Accuracy

In an intended application the 2nd order bandpass filter would be used to form one section of a 12th order Transitional Gaussian filter [chapter 3] requiring accurate amplitude and group delay responses. As such, the 2nd order bandpass filter was tuned to the extremes of frequency (12MHz to 50MHz) while maintaining a Q of approximately 30. The amplitude and phase response of the bandpass filter under these conditions are shown by Fig 6.3.5-1a & b.

The measured amplitude response of the 2nd order bandpass filter shown by Figs 6.3.5-1a & b are compared to the *ideal* response at the extremes of the centre frequency tuning range and shown by Fig 6.3.5-2a & b.

As shown by Fig 6.3.5-2a and Fig 6.3.5-2b, the measured amplitude responses are very closely matched to the *ideal* response, even at the extremes of the centre frequency tuning range, while maintaining a constant Q of approximately 30. To compare the differences more closely, the error between the two responses within the passband are shown by Fig 6.3.5-3a & b.

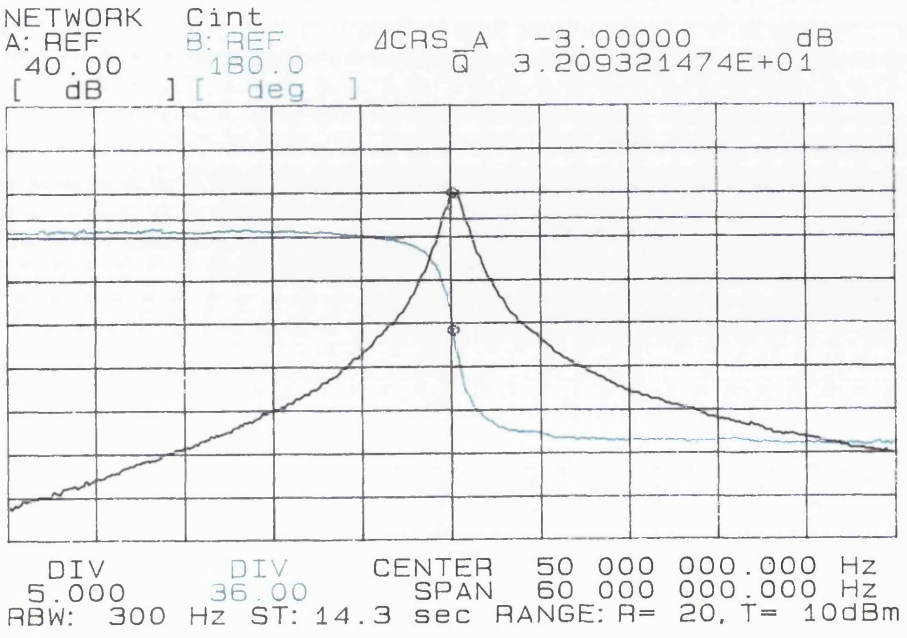


Fig 6.3.5-1a Amplitude and Phase Response of 2nd Order Bandpass Filter (Fo=50MHz, Q=32)

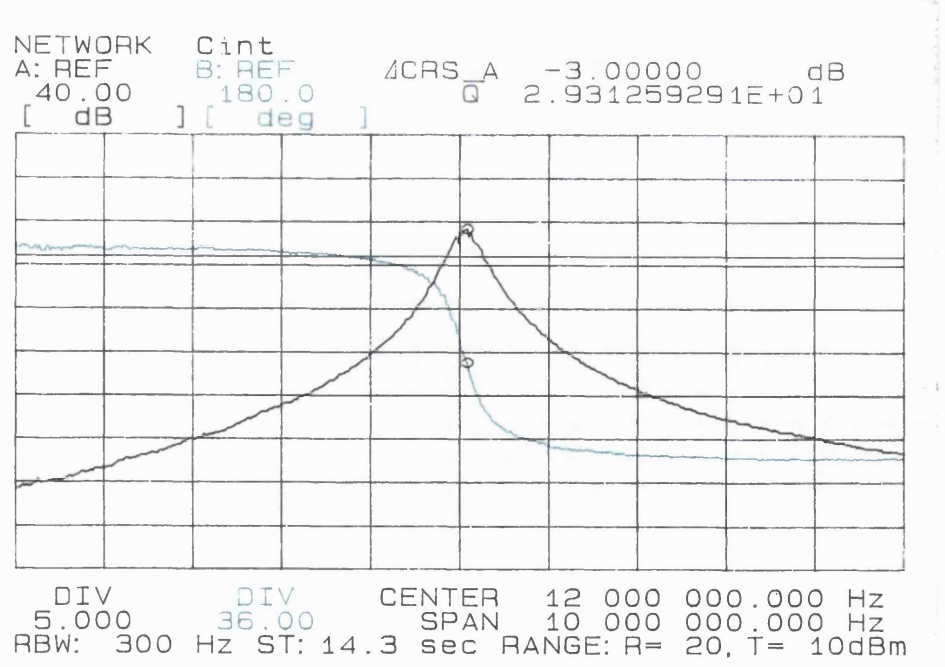


Fig 6.3.5-1b Amplitude and Phase Response of 2nd Order Bandpass Filter (Fo=12MHz, Q=29)

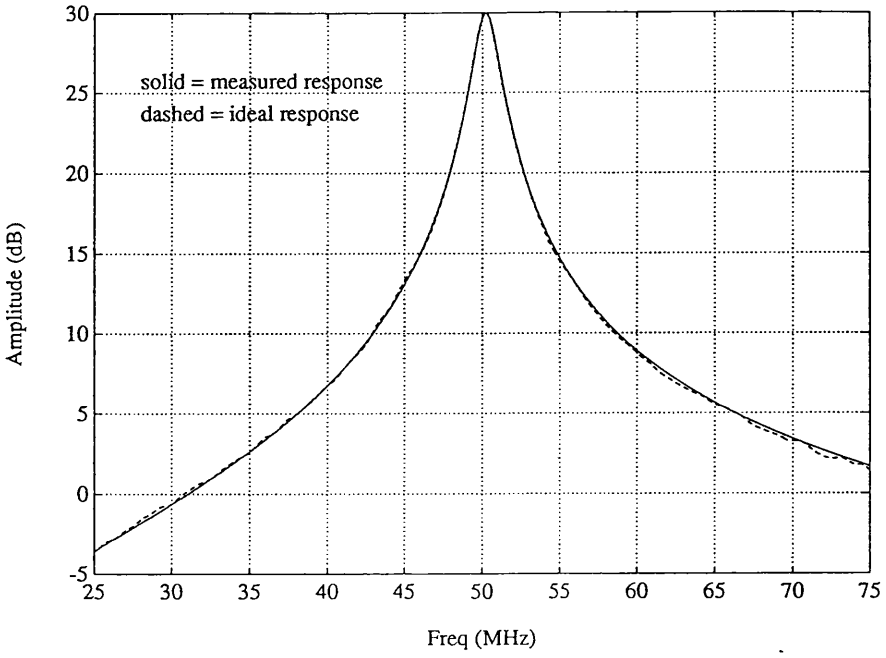


Fig 6.3.5-2a Amplitude Response of 2nd Order Bandpass Filter and Ideal Response at 50MHz

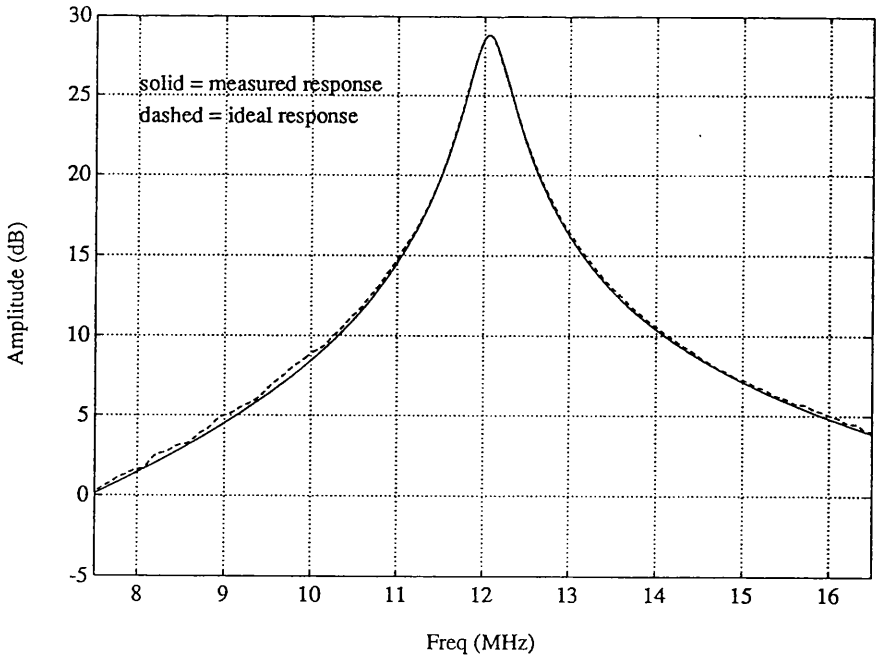


Fig 6.3.5-2b Amplitude Response of 2nd Order Bandpass Filter and Ideal Response at 12MHz

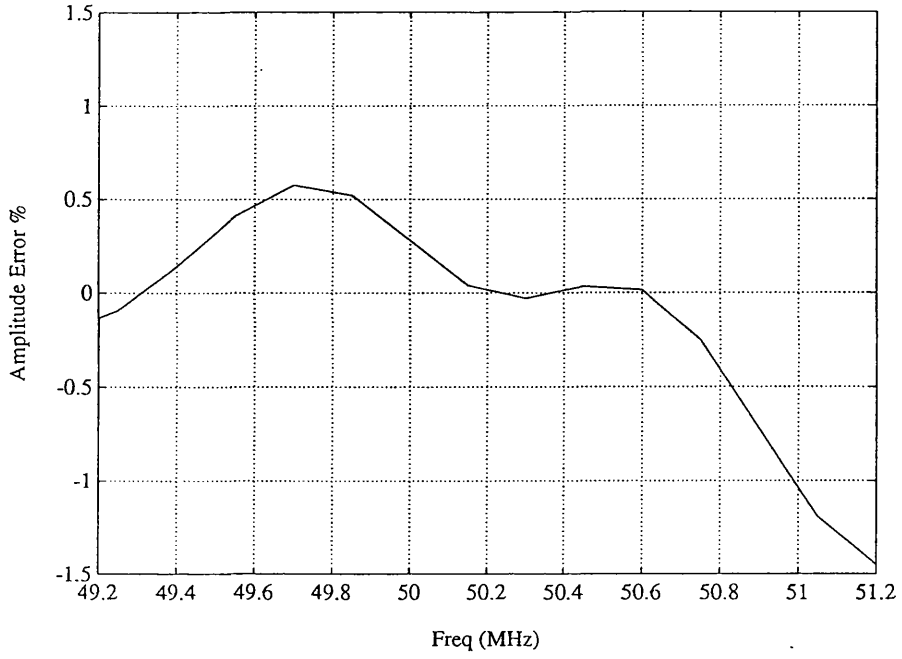


Fig 6.3.5-3a Error in Amplitude Response of 2nd Order Bandpass Filter at 50MHz

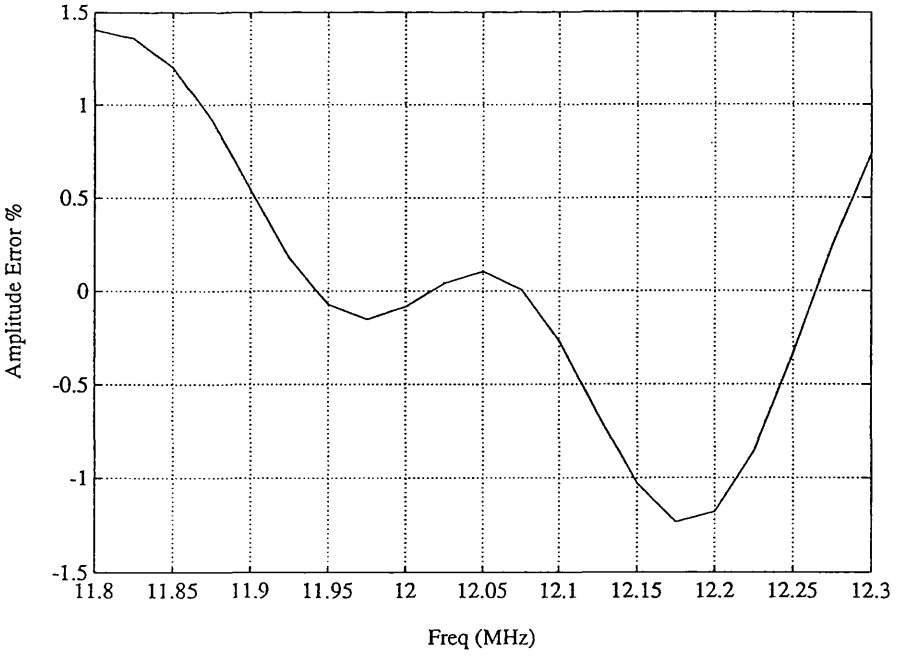


Fig 6.3.5-3b Error in Amplitude Response of 2nd Order Bandpass Filter at 12MHz

These responses indicate a maximum passband error of 1.5%, giving a good overall level of amplitude transfer function across the tuning range at a high Q.

In addition, the measured group delay responses of the 2nd order bandpass filter are compared to the *ideal* responses at the extremes of frequency tuning. Fig 6.3.5-4a and Fig 6.3.5-4b show group delay measurements corresponding to the amplitude responses of Fig 6.3.5-2a & b.

Since Q is relatively high, accurate measurement of group delay is difficult and problems were experienced with noise. As a result, the response shown in Fig 6.3.5-4a, in the range 25-75MHz have been smoothed to highlight the significant features of the comparison. The measurements carried out within the passband and shown in Fig 6.3.5-5b have *not* been subjected to smoothing and are presented as two separate responses rather than a proportional error as in the case of the amplitude response.

In view of the difficulties experienced with noise, it was felt that this method of presentation conveys the information most clearly. As in the case of the amplitude response, the use of a high-frequency technology is shown to minimise excess phase and hence maximise transfer function accuracy [104] at an FoQ figure of 1.5GHz.

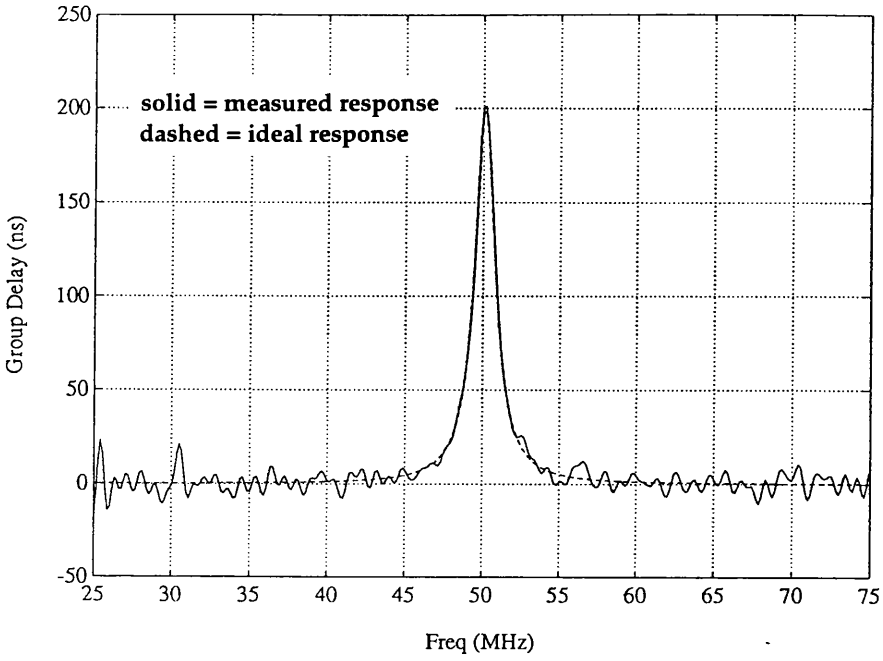


Fig 6.3.5-4a Group Delay Response of 2nd Order Bandpass Filter and Ideal Response at 50MHz

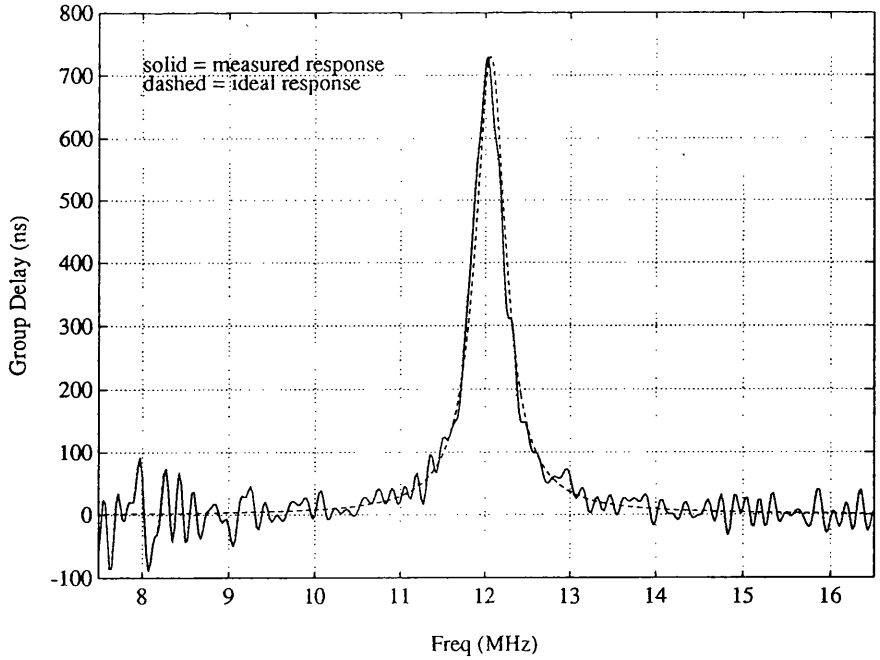


Fig 6.3.5-4b Group Delay Response of 2nd Order Bandpass Filter and Ideal Response at 12MHz

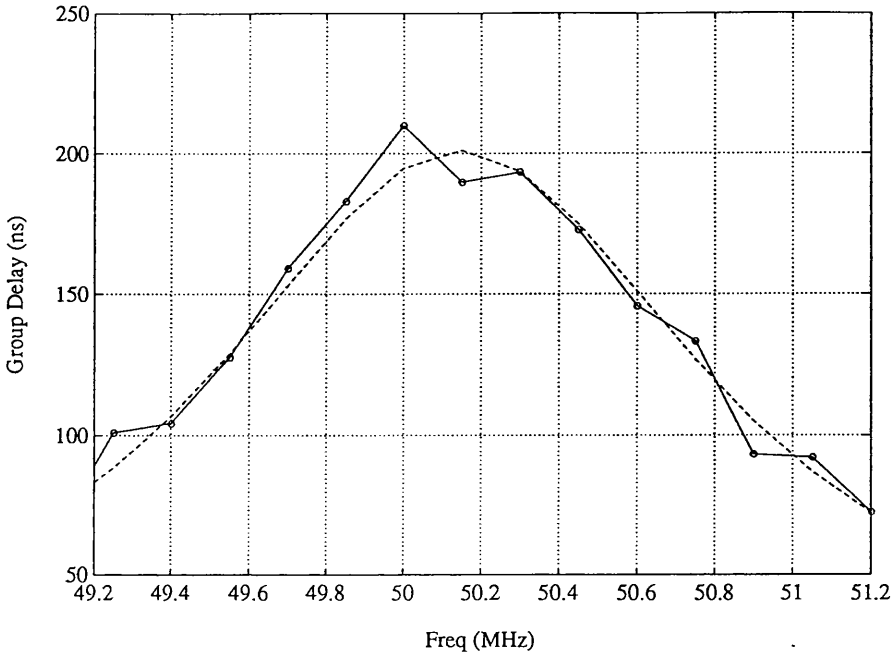


Fig 6.3.5-5a Group Delay Response of 2nd Order Bandpass Filter and Ideal Response with the passband at 50MHz

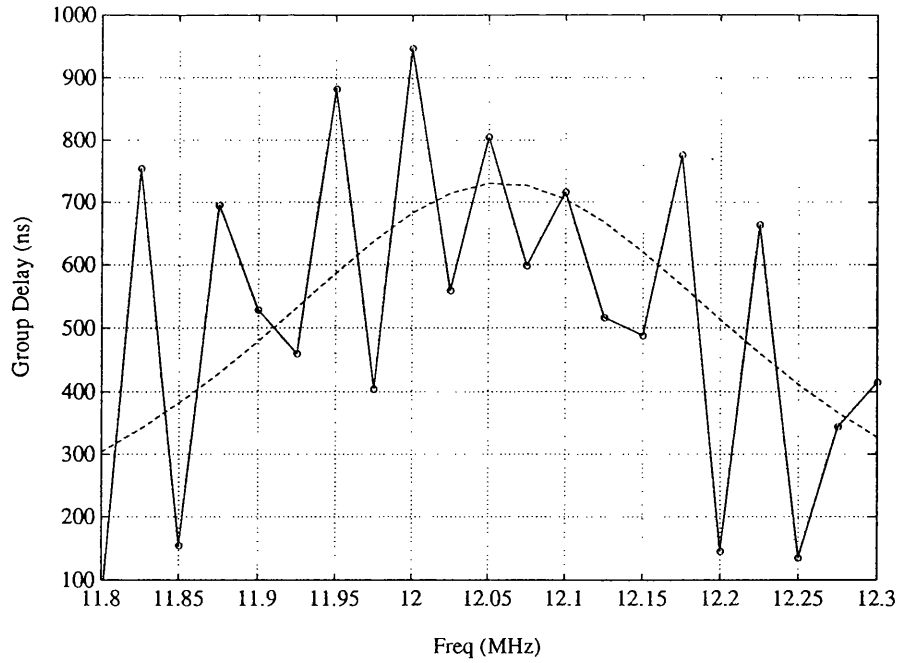


Fig 6.3.5-5b Group Delay Response of 2nd Order Bandpass Filter and Ideal Response with the passband at 12MHz

6.4 Conclusion

In this chapter the results of the fabricated OTA-C integrators and bandpass filters are presented and their performance compared to the simulated OTA-C integrator and 2nd order bandpass filters first presented in chapter 5.

The OTA-C integrator realised with a single geometry device biased at a common operating point proved to be successful. The simulated OTA-C integrator using the Shichman-Hodges model supported by SPICE proved to be able to predict the successful use of a new tuning method for Gm and Go. The frequency response of the integrator however was lower that that predicted by SPICE which was attributed to a smaller value of device gm. This was believed to be a result of a slightly different device used by the foundry when the OTA-C integrators were fabricated. However, the THD measurements also showed good agreement with the simulation which suggested that the use of a common biased device in deep saturation yields acceptable results when using a Shichman-Hodges model.

The use of only two OTA-C integrators to form a fully tunable 2nd order bandpass filter with independent control of centre frequency Fo and Q was also proven to be successful. The transfer function characteristics were compared to an ideal 2nd order response across the tuning range which has shown that a high degree of accuracy was achieved both in amplitude and group delay responses. Thus the presence of excess phase was kept at a minimum even at an FoQ figure as high as 1.5GHz.

CHAPTER 7

Conclusions and Future Work

7.1 Conclusions of Thesis

This thesis has described the design of a differential input OTA-C integrator intended to be used for high precision CT filtering. The OTA-C integrator was fabricated in 0.5μm, 20GHz GaAs MESFET technology and demonstrates a novel variable gain bootstrap circuit which overcomes several of the problems encountered when GaAs is employed in applications requiring low output conductance, Go. In addition, the OTA-C integrator features separate and novel method of transconductance, Gm tuning allowing independent control of Gm and Go. This allowed the implementation of a 2nd order, state variable bandpass filter using only two OTA-C integrators with independent control of Q and centre frequency.

The new OTA-C integrator is very linear and searching tests conducted over a wide range of Gm and at high input signal level reveal measured THD levels of the order of 1% depending on operating conditions. In addition, the single-ended circuit can be very economically extended to fully balanced, multiple input form with all the attendant advantages, including a more comprehensive solution to the reduction of THD. A fabricated, 2nd order CT bandpass filters using two OTA-C integrators demonstrated a measured centre frequency tuning range from 12MHz to 50MHz, which represents a ±60% variation. This represents the widest frequency tuning range reported in GaAs MESFET technology. In addition, the bandpass filter demonstrated a measured, controllable Q variation from 4 to 60 which represents a tuning range of ±87% with only minimal variation in centre frequency.

The 2nd order frequency response of the bandpass filter was compared to an ideal 2nd order response. The centre frequency of the filter was set to its maximum of 50MHz with the desired Q of 30. The amplitude response was compared to the ideal bandpass response and a maximum error of 1.5% in

the passband was measured. In addition, the group delay of the filter was measured and shows a good agreement compared to the response of an ideal 2nd order section. This indicates that the response of the filter is almost that of an ideal 2nd order bandpass section, even for high Qs, ie., it is virtually unaffected by phase errors introduced by the finite bandwidth of the OTA, which is an important property when used for its intended application as one section of a high order, constant group delay filter.

7.2 Suggestions for Future Work

This brief outline of the recommendations for further research work is intended to further the design goal of a practical, fully integrated 12th order Transitional Gaussian filter.

The design of the fully tunable OTA-C integrator was intend to form one bandpass section of a high precision, high-order filter. The problems of interconnecting each 2nd order section for optimum amplitude scaling must be investigated. The effects of excess phase introduced to the passband group delay must be taken into account. However, since the design of the OTA-C integrators offer a low impedance output via a source follower, the problem of inter-stage connection is somewhat alleviated.

The use of a fully balance architecture with all its advantages was suggested in this thesis and the final design of the CT filter using fully balanced OTA-C integrator should be considered. In addition, the design of appropriate on-chip single-ended to balanced converters for interfacing the integrated CT filter input/output ports to an external 50Ω environment is required

All integrated CT filters require some form of automatic on-chip tuning to maintain the filter characteristics which are subject to process tolerances and changes in operating conditions. The 2nd order bandpass section designed features independent control of Q and centre frequency which allows a simple control circuit to be designed. In addition, the type of control circuits (ie., amplitude or phase lock loops) employed to maintain correct centre

frequency and Q need to be investigated.

As a result of limited modelling information, very severe design restrictions were imposed to ensure correct operation of all the tuning methods introduced in this research. Although this did result in a robust design, with low dependence on a sophisticated foundry model, circuit performance in terms of temperature and noise are unknown. However, no specification of maximum voltage or power was provided at the time. Additional modelling information would be needed to optimise circuit design.

The accuracy of the transfer function of the 12th order Transitional Gaussian was investigated in chapter three. As indicated, the use of a wide band technology is necessary to preserve the accuracy of the transfer function and the control parameters. The fact that, although GaAs was used to demonstrate the tuning methods and transfer function accuracy of a 2nd order filter, wide band technologies such as Si Bipolar and the emergence of sub-micron CMOS used in some limited RF designs should also be considered. However, as the gate lengths of any (Si CMOS or GaAs) FET is lowered problems of high output conductance and the absence of a compatible complementary device become more critical. The tuning methods and gain enhancement techniques introduced in this thesis are applicable to all technologies.

Published Papers

The following is a list of published papers which have resulted directly from the work carried out on the project.

[1] P Visocchi, J Taylor, A Betts & D Haigh 'Novel Tunable GaAs MESFET OTA-C Integrator Suitable For High Precision Filtering Application', *Electron. Lett.*, Vol. 27, no.18, pp1671-1673, 29 August 1991.

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Appendix

Determination of voltage gain of bootstrap load amplifier from Chapter 5.3.3

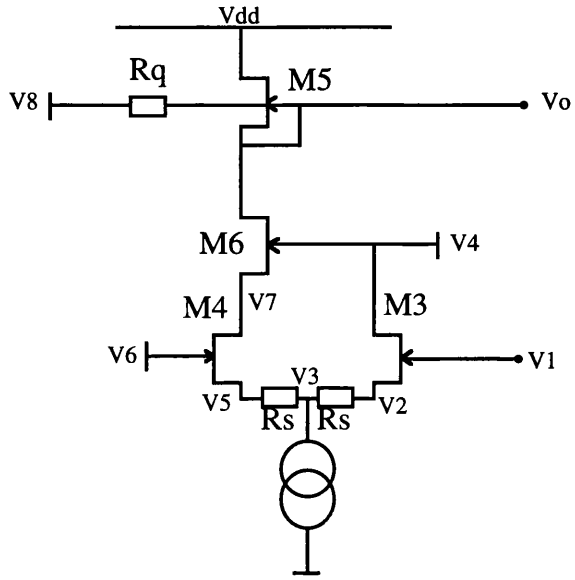

Fig A1 Variable Bootstrap Load from Chapter 5

From Fig A1 the voltage gain (vo/v1) of the amplifier is determined. Assuming all devices are of equal geometry and operating under common bias conditions:-

$$id = gm(v1 - v2) + go(v4 - v2) \qquad A1$$

and

$$-id = gm(v6 - v5) + go(v7 - v5) \qquad A2$$

also

$$id = \frac{(v2 - v3)}{Rs} \qquad A3$$

and

$$-id = \frac{(v5 - v3)}{Rs} \qquad A4$$

Since v4 and v6 are DC bias voltages, they may be considered AC grounds (ie v4=v6=0). Therefore, re-arranging equations A1 and A2 gives:-

$$id = gmv1 - (gm + go)v2 \qquad A5$$

and

$$-id = gov2 - (gm + go)v5 \qquad A6$$

By re-arranging equations A3 and A4, v2 and v5 are determined:-

$$v2 = idRs + v3 \qquad A7$$

and

$$v5 = v3 - idRs \qquad A8$$

By substituting equations A7 and A8 into equations A5 and A6 gives:-

$$id = gmv1 - (gm + go)idRs - (gm + go)v3 \qquad A9$$

and

$$-id = gov7 + (gm + go)idRs - (gm + go)v3 \qquad A10$$

By re-arranging equation A9 to determine v3:-

$$v3 = \frac{gmv1}{gm + go} - id\left[\frac{Rs(gm + go) + 1}{gm + go}\right] \qquad A11$$

By substituting equation A11 into equation A10 v7, is determined:-

$$v7 = \left(\frac{gm}{go}\right)v1 - 2id\left[\frac{Rs(gm + go) + 1}{go}\right] \qquad A12$$

The drain current, id of device M6 is determined:-

$$id = gm(v4 - v7) + go(vo - v7) \qquad A13$$

Since v4 is an AC ground (ie v4=0), equation A13 becomes:-

$$v7 = \frac{govo}{gm + go} - \frac{id}{gm + go} \qquad A14$$

By equating equation A12 and A14, id is determined:-

$$id = \frac{gm(gm + go)v1 - go^2vo}{2Rs(gm + go)^2 + gm} \qquad A15$$

The load of device M6 may be considered as the parallel combination of th

output conductance of M5 and the load resistor Rq, since v8 and vdd are regarded as AC grounds (ie v8=vdd=0). Therefore, vo can be determined as a function of id:-

$$id = \frac{vo(1+goRq)}{Rq} \qquad A16$$

Thus, by substituting equation A16 into equation A15, the voltage gain (vo/v1) is determined:-

$$\frac{vo}{v1} = A = \left(\frac{gm}{go}\right)\frac{go(gm+go)Rq}{2(1+goRq)(gmRs+goRs+1)(gm+go)-go} \qquad A17$$

From equation A17, assuming $2(1+goRq)(gmRs+goRs+1)(gm+go)\rangle\rangle go$, then A becomes:-

$$A \approx \left(\frac{gm}{go}\right)\frac{goRq}{2(1+goRq)(gmRs+goRs+1)} \qquad A18$$

From equation A18, assuming $goRs+1 \approx 1$, then A can be further reduced to:-

$$A \approx \left(\frac{gm}{go}\right)\frac{goRq}{2(1+goRq)(1+gmRs)} \qquad A19$$

To determine the sensitivity of the voltage gain A to changes in resistance value Rq, equation A19 is required to be differentiated with respect to Rq, giving:-

$$\frac{\partial A}{\partial Rq} = \frac{gm}{2(1+gmRs)(1+goRq)^2} \qquad A20$$

Thus, the first order differential sensitivity of A to a change in Rq can be determined:-

$$S_{Rq}^{A} = \frac{Rq}{A}\frac{\partial A}{\partial Rq} = \frac{1}{1+goRq} \qquad A21$$

However, if the resistors Rq and Rs are assumed to *track*, such that Rs=KRq, where K is a constant, then the voltage gain, A given by equation A19 becomes:-

$$A \approx \left(\frac{gm}{go}\right)\frac{goRq}{2(1+goRq)(1+KgmRq)} \qquad A22$$

To determine the sensitivity of the voltage gain A to changes in resistance value Rq, equation A22 is required to be differentiated with respect to Rq, giving:-

$$\frac{\partial A}{\partial Rq} = \frac{gm(1-KgmgoRq^2)}{2(1+goRq)^2(1+KgmRq)^2} \qquad A23$$

Thus, the first order differential sensitivity of A to a change in Rq can be determined:-

$$S_{Rq}^{A} = \frac{Rq}{A}\frac{\partial A}{\partial Rq} = \frac{1-KgmgoRq^2}{(1+goRq)(1+KgmRq)} \qquad A24$$