

Derivation of the Equivalent Input Noise of Multiplicative Distributed Amplifiers for Wideband Optical Receiver Applications

Temitope Odedeyi, and Izzat Darwazeh

Department of Electronic and Electrical Engineering, University College London, London United Kingdom
 {temitope.odedeyi.13, i.darwazeh}@ucl.ac.uk

Abstract—In this paper, we derive new models that describe the noise voltage and equivalent input noise current spectral densities for multiplicative distributed amplifiers. Based on the derived models, design optimisation techniques to minimise the noise contribution of transimpedance amplifiers based on the multiplicative DA topologies are proposed.

Index Terms—Distributed amplification, Multiplicative distributed amplifier, Ultra-wideband amplifier, Optical Receiver, Transimpedance amplifier.

I. INTRODUCTION

The potential of multiplicative distributed amplifiers (DAs) - comprising of the cascaded single-stage DA (C-SSDA) [1] and the matrix single-stage DA (M-SSDA) [2] - for remarkable gain-bandwidth performance has been established [1]–[9]. However, their noise characteristics, which is important for the appraisal of their utility in different systems, remain largely unexplored. Analysis of the noise figure of multiplicative DA was presented in [10], however, as by definition, the noise figure applies only to amplifiers that are excited by a purely resistive signal source, the noise figure is not applicable when the signal source impedance contains a reactive component [11]. An example of such applications is the optical receiver front-end (RFE), with a photo-diode capacitive input [12]. For such applications, it is more useful to consider the total output port noise, referred to the input of the amplifier [13]. For the RFE, the equivalent input noise current spectral density (EINCS) is of primary interest as it allows the front-end noise to be compared directly with the current signal generated by the photodiode [14]–[17]. In this paper, we derive expressions to obtain the EINCS of a FET based multiplicative DA. Our approach follows [14], in that we firstly derive the noise voltage spectral density (NVSD) at the output of the amplifier and refer this to the input, by dividing by the the amplifier transimpedance gain, thus obtaining the EINCS.

II. MODELLING OF EINCS IN MULTIPLICATIVE DAS

Fig. 1 shows the schematic of a multiplicative DA with m -tiers, based on the M-SSDA topology.

A. Evaluating Single Stage EINCS

Fig. 2 shows a simplified equivalent circuit for a MES-FET/HEMT featuring its associated Van der Ziel gate and drain noise sources [18]. The squares of the single-sided gate and drain noise current spectral densities (NCS), measured in $A/\sqrt{\text{Hz}}$ are given, respectively, by [19]

$$|i_g|^2 = \frac{4kT_o C_{gs}^2 \omega^2 R}{g_m} \quad (1)$$

and

$$|i_d|^2 = 4kT_o g_m P \quad (2)$$

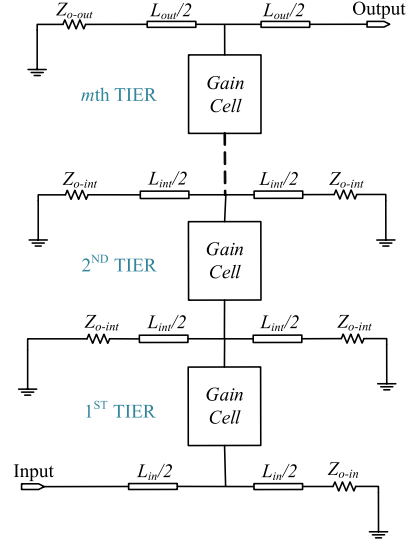


Fig. 1: Schematic of m -tier multiplicative DA.

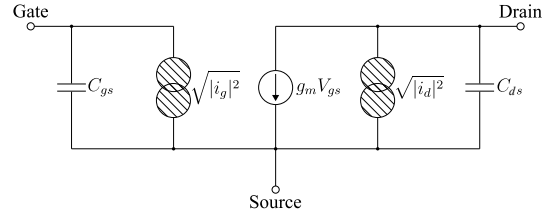


Fig. 2: Simplified intrinsic equivalent circuit of a MES-FET/HEMT with its associated gate and drain noise sources.

where k is Boltzmann's constant (1.38×10^{-23} J/K), T_o is 290 K, ω is angular frequency, C_{gs} is the FET gate-source junction capacitance, and R and P are dimensionless coefficients from Van der Ziel's FET noise behaviour model that depend on bias conditions, device geometry and other technological parameters [18], [20], [21]. For a single stage DA based on a simplified equivalent FET model as shown in Fig. 2, three noise sources may be defined - the input terminating impedance; the output terminating impedance; and the FET gate and drain noise sources. The noise voltage spectral density (NVSD, measured in $V/\sqrt{\text{Hz}}$) due to each of these current sources - v_{o1} , v_{o2} and v_{o3} , respectively, is subsequently defined, after which the expression is extended to define the noise voltage of the multiplicative amplifier.

The EINCS (i_{neq}) is obtained by dividing the total noise voltage at the output v_{nout} by the amplifier transimpedance A_{tz} (in Ω)

$$i_{neq} = \frac{v_{nout}}{|A_{tz}|} \quad (3)$$

where v_{nout} is given by

$$v_{nout} = \sqrt{|v_{o1}|^2 + |v_{o2}|^2 + |v_{o3}|^2} \quad (4)$$

For as single stage DA with equal terminating impedances, A_{tz} is the same in both forward i.e. at the terminating load (Z_f) and the reverse direction i.e. at the drain termination (Z_r), and is given by [19]

$$A_{TZ} = Z_f = Z_r = \frac{g_m Z_{\pi g} Z_{\pi d}}{2} \quad (5)$$

where $Z_{\pi g}$ and $Z_{\pi d}$ are the π -image impedances of the input and output artificial transmission lines (ATLs) of the DA, respectively [19], [22], [23]. Image impedance, $Z_{\pi} = \sqrt{(L/C)/(1 - (\omega/\omega_c)^2)}$, where L , C and ω_c are the inductance, capacitance and cut-off frequency of the ATL, respectively.

Noise voltage contribution from input terminating impedance Z_g : The NCS generated by Z_g is given by [16]

$$|i_{Zg}|^2 = \frac{4kT_0}{Z_g} \quad (6)$$

For a single stage DA, half of the noise current $i_{Z\pi g}$ is directly absorbed by $Z_{\pi g}$ itself, while the other half travels toward the input. As this is ideally an open circuit (current source), this signal gets totally reflected. The total voltage that appear at the output due to this source is given by

$$v_{o1} = i_{Zg} A_{TZ} (1 + e^{-j\frac{\phi}{2}}) \quad (7)$$

where $\phi = \omega\sqrt{L_g C_{gs}}$ is the propagation delay of the input ATL [24].

Noise voltage contribution from output terminating impedance Z_d : The NCS generated by Z_d is given by [16]

$$|i_{Zd}|^2 = \frac{4kT_0}{Z_d} \quad (8)$$

Half of the noise current from the drain termination is dissipated in $Z_{\pi d}$ itself while the other half travels down the drain line and gets dissipated in the output, producing a noise voltage, v_{o2} ,

$$v_{o2} = \frac{i_{Zd}}{2} Z_d e^{-j\frac{\rho}{2}} \quad (9)$$

where $\rho = \omega\sqrt{L_d C_{ds}}$ is the propagation delay of the output ATL, and C_{ds} is the FET drain-source capacitance [24].

Noise voltage contribution from FET: The noise current sources for a FET transistor, as previously defined are the gate noise source given in (1) and the drain noise source given in (2). The gate noise contribution may be separated into two components: the first component is the forward travelling wave which will produce an output voltage with a forward transimpedance gain. The second component is the reflected wave, due to the reverse wave reflecting off the open circuit at the input. This wave will also produce a voltage with the reverse transimpedance gain [19], such that the total output noise voltage due to i_g is given by

$$v_{out}^g = \frac{i_g}{2} Z_f + \frac{i_g}{2} Z_r = i_g A_{TZ} \quad (10)$$

For the drain noise, half of the drain noise current travels toward the drain termination (Z_d) and is absorbed, while the other half travels toward the load and produces a corresponding output voltage, such that total current due to i_g can be written as

$$i_{out}^d = \frac{i_d}{2} e^{-j\frac{\rho}{2}} \quad (11)$$

with corresponding output voltage given by

$$v_{out}^d = i_{out}^d Z_d = \frac{i_d}{2} Z_d e^{-j\frac{\rho}{2}} \quad (12)$$

The square of the overall output noise voltage due to the FET noise (v_{o3}) is therefore given by

$$v_{o3}^2 = |i_g A_{TZ}|^2 + \left| \frac{i_d}{2} Z_d e^{-j\frac{\rho}{2}} \right|^2 \quad (13)$$

Hence, substituting (7), (9) and (13) in (4),

$$v_{nout} = \sqrt{|i_{Zg} A_{TZ} (1 + e^{-j\frac{\phi}{2}})|^2 + \left| \frac{i_{Zd}}{2} Z_d e^{-j\frac{\rho}{2}} \right|^2 + |i_g A_{TZ}|^2 + \left| \frac{i_d}{2} Z_d e^{-j\frac{\rho}{2}} \right|^2} \quad (14)$$

and the EINCSD (i_{neq}) is obtained by dividing v_{nout} given by (14), by the amplifier transimpedance A_{tz} given by (5). The input noise current contributions due to v_{o1} , v_{o2} and v_{o3} may also be individually determined by dividing each by A_{tz} .

Fig. 3 shows the input noise current contributions from the gate termination (i_{n1}), the drain termination (i_{n2}), and the FET (i_{n3}) to total EINCSD for a single stage FET DA with terminations $Z_g = Z_d = 50 \Omega$, and a simplified equivalent model based on Fig. 2 is used as gain cell, where g_m of 50 mS; C_{gs} and C_{ds} of 50 fF and 5 fF, respectively; and FET transistor parameters R and P of 0.2 and 0.6, respectively. As seen in Fig. 3, the major noise contributor in the low frequencies is the gate line termination, with minimal noise contribution from the drain (output) line termination. The noise contribution from the active device is dominated in the lower frequencies by the drain noise component ($|i_d|$). However, at higher frequencies, the gate noise component ($|i_d|$) dominates, due to the presence of the ω^2 factor, which also explains the continuous rise of the FET noise contribution beyond cut-off (Fig. 3)

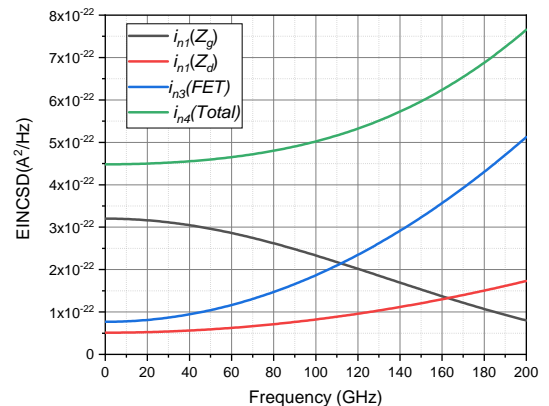


Fig. 3: Components of the total EINCSD of the SSDA.

B. EINCSD for Multiplicative DAs

To extend (4) to multiplicative DAs, the noise voltage for the terminations $Z_{\pi-int}$ on the intermediate ATLS - which we denote as v_{o-int} - must be included. The last term in (4), v_{o3} , which represents the FET noise contribution must also be expanded to include all the gain tiers of the multiplicative DA. First, we define the transimpedance gain of the multiplicative DA with m gain tiers (A_{tz}^{mlt}), which for the multiplicative DA is equal in both the forward (Z_f^{mlt}) and reverse (Z_r^{mlt}) direction and is given by

$$A_{TZ}^{mlt} = Z_f^{mlt} = Z_r^{mlt} = \frac{g_m^m}{2^m} Z_{\pi g} Z_{\pi d} Z_{\pi-int}^{(m-1)} \quad (15)$$

where $Z_{\pi-int}$ is the image impedance of the intermediate ATLS, and the superscript *-mlt-* reflects that this refers to a multiplicative DA.

The total noise voltage at the output of the multiplicative DA, v_{nout}^{mlt} is given by

$$v_{nout}^{mlt} = \sqrt{|v_{o1}^{mlt}|^2 + |\sum v_{o-int}^{mlt}|^2 + |v_{o2}^{mlt}|^2 + |\sum v_{o3}^{mlt}|^2} \quad (16)$$

where v_{o1}^{mlt} and v_{o2}^{mlt} are the noise voltages due to the input and output line terminations, respectively; and $\sum v_{o-int}^{mlt}$ and $\sum v_{o3}^{mlt}$ are the sums of noise voltages from the intermediate line terminations and FET, respectively, and i_{neq}^{mlt} which is the EINCSD is given by

$$i_{neq}^{mlt} = \frac{v_{nout}^{mlt}}{A_{TZ}^{mlt}} \quad (17)$$

Noise voltage contribution from input and output terminating impedance: The noise voltage contribution of the input terminating impedance for a multiplicative DA with m stages - v_{o1}^{mlt} - is the noise current multiplied by transimpedance gain,

$$v_{o1}^{mlt} = i_{Z_g} A_{TZ}^{mlt} (1 + e^{-j\frac{\phi}{2}}) \quad (18)$$

The noise voltage due to the output terminating impedance, as is to be expected, remains unchanged for the multiplicative DA. However in keeping with a consistent convention, this is rewritten as v_{o2}^{mlt} , with

$$v_{o2}^{mlt} = \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\phi}{2}} \quad (19)$$

Noise voltage contribution from intermediate terminating impedance: The noise voltage contributions from the terminating impedances on the intermediate lines Z_{int} is derived by considering a two-tiered multiplicative DA, which has only one intermediate ATL. Assuming purely resistive terminations, the square of the NCSN of the thermal noise generated by each terminating resistor is given by

$$|i_{Z_{int}}|^2 = \frac{4kT_o}{Z_{int}} \quad (20)$$

with corresponding voltage $v_{Z_{int}}$ being the product of the intermediate line current and the transimpedance gain at that point relative to the input

$$v_{Z_{int}} = \frac{i_{Z_{int}}}{4} g_m Z_{\pi d} Z_{int} \quad (21)$$

Unlike on the output (drain) line where half of the termination noise current gets absorbed by the termination itself while the other half travels towards and gets dissipated in the output, the presence of two terminating resistances at opposite ends of the intermediate line results in a voltage noise source, $v_{o-int}^{mlt} = \sqrt{2v_{Z_{int}}^2}$, when both terminating impedances on the intermediate line are equal. We may extend (21) for a multiplicative DA with m tiers and $(m - 1)$ intermediate ATLS as

$$v_{o-int}^{mlt} = \sqrt{\sum_{p=1}^{m-1} \left| \frac{i_{Z_{int}}}{2^p} g_m^p Z_{\pi d} Z_{int}^p \right|^2} \quad (22)$$

Noise voltage contribution from FET: We extend (13) to the multiplicative DA by taking a sum of all the noise voltage excitations due to the FET noise current sources for each tier, which essentially is the noise current multiplied by the transimpedance gain relative to the output. The overall output noise voltage due to the FETs in the multiplicative amplifier with m gain tiers - v_{o3}^{mlt} - is given by

$$v_{o3}^{mlt} = \sqrt{\sum_{p=1}^m \left| \frac{i_g}{2^p} g_m^p Z_{\pi g} Z_{\pi d} Z_{int}^{(p-1)} \right|^2 + \sum_{p=1}^m \left| \frac{i_d}{2^p} g_m^{(p-1)} Z_{\pi d} Z_{int}^{(p-1)} \right|^2} \quad (23)$$

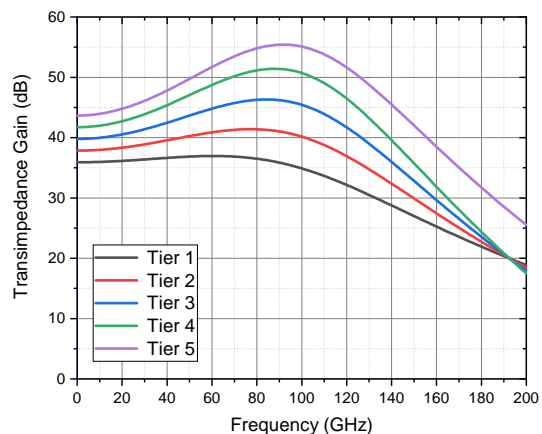
Substituting (18), (22), (19) and (23) in (16),

$$v_{nout}^{mlt} = \sqrt{|i_{Z_g} A_{TZ}^{mlt} (1 + e^{-j\frac{\phi}{2}})|^2 + \left| \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\phi}{2}} \right|^2 + \sum_{p=1}^{m-1} \left| \frac{i_{Z_{int}}}{2^p} g_m^p Z_{\pi d} Z_{int}^p \right|^2 + \sum_{p=1}^m \left| \frac{i_g}{2^p} g_m^p Z_{\pi g} Z_{\pi d} Z_{int}^{(p-1)} \right|^2 + \sum_{p=1}^m \left| \frac{i_d}{2^p} g_m^{(p-1)} Z_{\pi d} Z_{int}^{(p-1)} \right|^2} \quad (24)$$

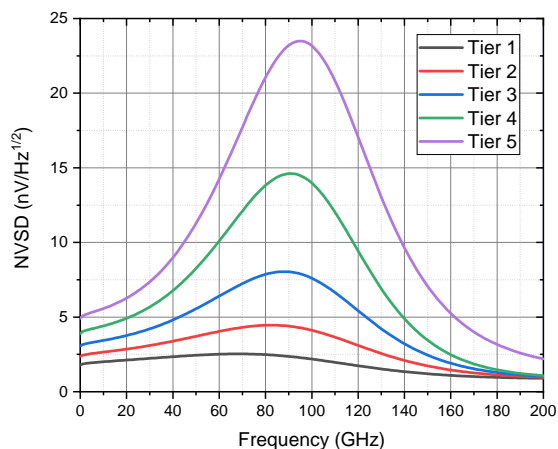
such that i_{neq}^{mlt} which is the sought expression is obtained by dividing v_{nout}^{mlt} in (24) by the transimpedance gain of the multiplicative DA, given in (15).

Fig. 4 (a), (b) and (c) show the transimpedance gain, total RMS NVSD at the output port and the EINCSD at each stage of a 5-tier M-SSDA, using the same equivalent circuit parameters as used in Fig. 3. This demonstrates how the EINCSD scales with additional gain tiers in multiplicative DAs. The M-SSDA features conventional 50 Ω input, output and intermediate ATL terminations. Similar to the observation from the noise figure analysis in [10], more than 70% of the total EINCSD for the five gain tiers of the amplifier is contributed by the first stage.

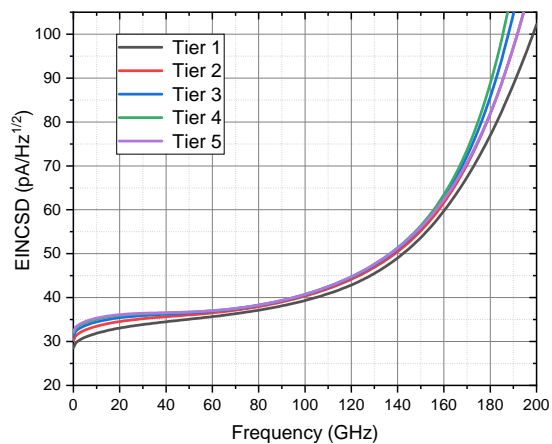
The dominant contribution of $i_{Z_{\pi g}}$ to the overall NVSD and EINCSD may be observed in the first term of (24), as it is multiplied by the full forward transimpedance gain of



(a) Transimpedance gain



(b) NVSD at output port



(c) EINCSD at input

Fig. 4: The scaling of transimpedance, noise voltage and noise current spectral densities in a multiplicative DA with 5 tiers, based on a simplified equivalent HEMT model as gain cell.

the amplifier. This effect may be observed in Fig. 5, which shows the EINCSD for various values of input terminating impedance. The FET gate noise i_g also occupies a similar position, however due to its frequency dependence (as seen in (1)), its noise contribution at low frequencies is minimal, and increases as the amplifier approaches cut-off.

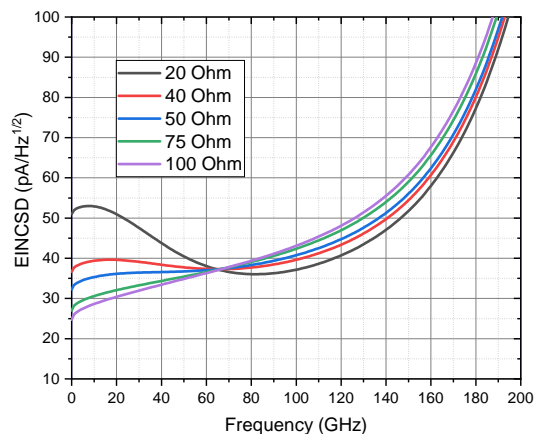


Fig. 5: Effect of different values of input termination EINCSD for a 5-tier M-SSDA.

III. EINCSD OPTIMISATION FOR MULTIPLICATIVE DAS

From the EINCSD analysis, it may be noted that as m increases, the noise current contribution from successive ATLs of the multiplicative DA reduces, with the least contribution coming from the output line. This we observe, by considering that in (24), only the noise contribution from the input termination noise source is multiplied by the full transimpedance gain of the amplifier, with the contributions from higher tiers multiplied by lower gain values based on their position relative to the output. This, again, supports the approach of maximising the gain of the first stage and designing the input line for minimum noise contribution by making the input line impedance as large as design bandwidth specifications would allow. The design optimization proposed in [10], which involves the adoption of a transistor with a higher bandwidth potential in the first stage, will also be beneficial. This would allow for the input ATL to be designed at a higher impedance without sacrificing bandwidth.

It is important to note that while this derivations have been made using a FET equivalent circuit, the derivations can also be easily extended to cover multiplicative DAs based on bipolar devices. The EINCSD optimisation techniques are also applicable in both contexts.

IV. CONCLUSION

This paper presents new models that describe the noise voltage spectral density and the equivalent input noise current spectral density of the multiplicative DA based on a FET equivalent circuit, for application in wideband optical receiver design. These models provide information on the scaling of noise in the multiplicative DA and techniques for performance optimisation, which are applicable in both FET and bipolar contexts.

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