Self Electro-optic Effect Devices and their use in optical switching and communications systems

A thesis by

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To Mum and Dad

To Jane

ABSTRACT

This thesis concerns itself with the optimisation and potential use of the symmetric self electro-optic effect device (S-SEED), a bistable optoelectronic logic device.

The SEED utilises the change in absorption of light, of semiconductor multiple quantum wells, when an electric field is applied perpendicularly to their layers (ie. the quantum confined Stark effect). These multiple quantum wells, incorporated into the intrinsic region of a pin diode type structure, can be used to modulate an incident light beam by varying an applied electric field. Under certain conditions, the SEED can be operated under positive feedback and is bistable in the intensity of its input beams. By using the modulation enhancing characteristics of an asymmetric Fabry-Perot cavity, these devices can exhibit very high switching contrasts for low operating voltages. A high contrast SEED is demonstrated. These devices can also operate as linear modulators or optical 'taps' in which the tap absorbs only sufficient incident optical power to satisfy a current drive, with the remainder of the optical power reflected. An high contrast linear modulator and its functionality as an optical tap is demonstrated. This device's application for use in a self-adjusting, optical to electronic, serial to parallel convertor is also proposed.

A limitation of current optical switching devices is that they are either relational devices with high bandwidth and no bit-sensitivity, or they are purely logic devices with bit-sensitivity but much lower bandwidth. A new way of operating the S-SEED is shown which combines the advantages of both groups of optical switching device. This 'enhanced intelligence' S-SEED can be operated in such a way as to yield functionality similar to that required in self-routeing optical packet switches. A discussion is also made of optimum SEED device characteristics and limitations with respect to speed and signal tolerances in S-SEED systems applications.

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CHAPTER 1

Introduction

1.1 Introduction

Optical technology has much to offer the areas of telecommunications and computing [1]. Optical fibre has now, due to its high capacity and cost, almost entirely displaced co-axial cable in the long distance terrestrial trunk telecommunications network [2]. The high bandwidth capacity and the low signal losses of optical fibre has led to it being the preferred transfer medium for very high bit-rate services such as high definition television (HDTV) and pay per view television etc.[3]. Its presence has been felt in metropolitan area networks (MANs), local access networks (LANs) and its penetration is now spreading towards the network perimeters. Currently there are a number of studies going on around the world to investigate the feasibility of 'fibre-to-the-home' [4], in which a single optical fibre would be able to handle all our information and home entertainment requirements. However, it is not just in long distance communication applications that optics is expected to play an increasingly important part.

As very large scale integration (VLSI) technology becomes more mature, ever increasing integrated circuit packing densities are achieved. Circuits providing even greater functionality can be constructed in the same die area due to the increased packing density of devices and wires. These circuits can be made to operate at, or are 'clocked' at, higher and higher bit-rates as a direct result of integration and the associated increased device capabilities and decreased parasitic capacitance that can be achieved. However in the face of increased functionality per unit area and increased operating speeds, these improvements are constrained by the problem of getting more and more data into and out of the chip in order to meet its increased information needs [5-7]. As the functionality of a single chip system increases, greater demands are made on the number of chip input and output channels. This trend can be seen for example in microprocessor systems design: As higher power processor chips with greater utility become available, wider data and address paths have been adopted. In addition, special purpose co-processors requiring high speed co-processor interfaces have become quite common [6]. Therefore it is seen that interconnection and communication within a digital system is fast becoming a fundamental system performance limitation. This is especially true in the case of certain signal processing applications where the amount of actual computation per sample is relatively small and hence the system is often input/output bound rather than processing bound [5, 6].

As the trend towards increasing complexity and increasing pin count continues, a problem arises due to the fact that the pin count in an integrated circuit does not scale with increasing levels of integration. Bonding pad size and die perimeters remain constant, thereby constraining the number of pins available for input and output. Also, as

system clock speeds get faster, data needs to be moved on and off the chip at higher speeds. Off-chip load capacitances caused by bond pads, pins and board circuit tracks unfortunately however do not decrease with decreased linewidths [7]. Increasing the data rate therefore becomes expensive both in terms of power consumption and the chip area required for driving the electrical tracks for communication. A typical metal conducting path at chip level presents itself to the drive circuit as a capacitor to be charged and discharged according to the required logic level. The power consumed in this process increases with increasing track lengths and for higher bit-rates. The pin out/ communication issue in VLSI design is fast becoming a bottleneck which is constraining future system performance. A number of studies have been carried out which compare the power requirements for communication over electrical tracks and using optical techniques. These studies suggest that in power terms, optical communication links are superior to electrical ones over distances longer than approximately 1mm at bit rates of 1 GHz [8,9]. These arguments lead to the conclusion that an optimum architecture which exploits the high capacity interconnect capabilities of optics and the processing power of electronics, consists of small electronic 'islands' interconnected by high speed optics [10]. These electronic islands or 'smart pixels' do their internal communication and processing at very high speeds because of the short electrical interconnection lengths involved. Inter-island communication over longer distances is performed optically and makes use of the high speed and low power requirements of optical communication links to solve the input/output bottleneck of conventional electronic systems.

Another method of increasing the capacity of processing systems, in addition to operating at higher speeds, is to operate on information in parallel, instead of in series. Optical technology readily lends itself to this type of application because of the low crosstalk and interference of very closely spaced optical beams. Many optical beams can be placed in close proximity, with very little interference, to form very high bit-rate, massively parallel communication links. Optical logic devices have been made which can perform processing and Boolean logic operations on input optical signals. However these devices are currently too limited in their speed and energy requirements to be a serious contender for the replacement of VLSI technology [10]. The 'electronic islands' or 'smart pixel' type architectures could take advantage of these concepts, with large arrays of small high speed electronic processing units or islands, interconnected optically in parallel. All the I/O in such a configuration is thus done optically, with a large possible pin-out of very high bandwidth. The processing function of the system is achieved electronically, communication is optical, and thus advantage is taken of the strengths of the two respective technologies. The incoming signal can be converted from the optical to the electronic domain by using photodetectors which can also act as modulators in order to modulate a constant power incident optical beam, thereby performing a pin-out function. The laser light source used, can be located off-chip to reduce on-chip power consumption and can be split into a number of parallel optical communication paths. Further advantage can be obtained reducing clock timing skew by using optical techniques to distribute the clock signal within a digital processing system [11]. Photodetector/modulators can be made very small and many devices of say 10μm x 10μm could be fitted in the surface area of a conventional electronic bond bad (200μm x

200μm). Also, due to these devices' very small capacitances, much less driver circuitry is required to drive an electroabsorption modulator when compared to bond pads, pins and printed circuit board electrical tracks. Surface emitting laser technology could also be used as a source for the optical interconnect [12]. Considerable attention is now being paid to the issue of optical 'wiring' in this type of system configuration. The problems associated with interconnecting large arrays of cascaded devices are not insignificant however and these systems require very precise mechanical optical alignment systems. New architectures are being investigated which might make use of the inherent parallelism of interconnection using free-space optics [13].

Until recently, one of the weaknesses of the use of optical fibre in the trunk telecommunications network was that the optical signal needed to be amplified at certain intervals due to signal attenuation down the fibre. This was achieved by electronically detecting the signal, amplifying it and then reconverting the reconstructed electrical signal back to an optical one. This however limited the maximum bit rate of the transmission system to that of the speed of the repeater electronics. Increasing the communication link bit rate was difficult since it required the replacement of the repeater electronics. Also very little of the optical bandwidth was used, since the electronic detection and amplification process made it difficult to use different wavelength signals (wavelength division multiplexing, WDM) in a communications link. However, the advent of the optical fibre amplifier [14] has meant that optical signals can be regenerated all optically without having to have recourse to the electronic domain. It is now possible to build a most desirable transmission channel in which all optical data can be sent transparently from end-to-end. This transparent optical 'pipe' is only limited by the terminal electronics. If system capacity needs to be increased then the terminals are simply replaced. The optical amplifier also has the property that it allows a passband of approximately 50nm (@ 1.55μm) which corresponds to an optical bandwidth of greater than 6×10^{12} Hz. This opens up the huge bandwidth potential of optical communication and leads the way to using dense wavelength division multiplexing [15] and coherent communication techniques [16] (the optical analog of frequency multplexion in radio communication). Given that we now have transparent optical pipes of virtually unlimited bandwidth it would be nice to be able to route or switch optical signals to their destinations without having recourse to speed limiting electronics.

A number of technologies exist that can switch or route optical signals. These can be divided into two main categories based on their device characteristics in photonic switching architectures [17-18]. Firstly, 'logic' devices are devices in which an optical signal interacts with the device in such a way that controls the state of the switching device (ie. ON or OFF). These devices have the ability to sense and interact with individual bits in a bitstream and can perform boolean logic operations. However, because of their strong interaction with individual bits, the maximum transmitted bit-rate that may be conveyed is limited because of the need that some of the devices in a system must be able to change states or switch as fast, or faster than the signal bit-rate. A device structure which has been investigated to perform optical logic operations is the nonlinear Fabry-Perot etalon. This device structure makes use of a non linearity eg. thermal [19], or an absorption related change in refractive index [20] which enables logic operations to be

performed. However, these devices have strict requirements on their bias beam stability which puts very strict restrictions on the thermal control of these devices [21]. The use of these devices in systems applications is limited by the requirement that they are critically biased and the need for a high degree of system temperature stability. Because of this they are intolerant to fluctuations in signal strength, thermal noise and are difficult to cascade into useful systems. Another type of optical logic device is the bistable Self Electro-optic Effect Device (SEED) [22], which uses the quantum confined Stark effect (QCSE) [23] in semiconductor multiple quantum wells to alter its absorption of light. A refinement of this device is the Symmetric or S-SEED [24-25] in which two mqw modulators are reverse biased in series and in the presence of positive feedback, these devices are bistable in the ratio of two input power beams. If one input is greater than the other, then the device operates in one state with one output reflected (or suppressed) with respect to the other. If the converse is true, the device operates in its other stable state. This has the advantage that operation is possible over many decades of input power range and since the inputs are differential in nature, there is no need for critical biasing. It is the optimisation and practical application of the SEED logic device which is the main subject of this thesis. The switching contrast ratio can be dramatically enhanced and operating voltages reduced by incorporating the device structure within the confines of an asymmetric Fabry-Perot cavity (chapter 2). System speed performance and signal tolerancing can be enhanced by applications using this type of device with its increased contrast. Ideal SEED device characteristics for use in photonic switching applications are quantified and discussed (chapter 5).

The second category of optical switches are 'relational' or 'passive' devices. These are optical switches that perform a mapping function between given inputs and outputs depending on the state of some control signal. These devices are transparent to the service bit-rate passing through them and therefore their bandwidth can be very large. However, these switches have no ability to extract information from the bits throughput: They are bit insensitive. Optical switches of this kind would include mechanical fibre switches [26], planar waveguide switches, for example in $LiNbO_3$ [27] or spatial light modulators (SLMs) [28]. Mechanical fibre switches operate by electro-mechanically moving the end of an optical fibre to couple light in from one source to another. Switching time is slow, due to having to physically move the fibre, but this switch can be useful in applications having slow reconfiguration times, eg. route protection in a telecommunications network. A more sophisticated relational optical switch is that of a directional coupler. The most advanced implementations of these have been achieved using $LiNbO_3$ technology. Demonstrations of a 128 x 128 switch have been implemented [29]. These demonstrations make use of over 8000 directional couplers and 800 laser amplifiers to cope with signal attenuation on passing through the switch. One of the main disadvantages of $LiNbO_3$ technology and of directional couplers as a whole however, is that long interaction lengths (order of a few mm's) are required for efficient coupling of light from one signal path to the other. This limits the degree of integration that can be obtained and is costly in terms of chip 'real estate'. Also these devices require high operating voltages and dual rail voltage control which limits switching speed and switch reconfiguration times. Also, the need for polarisation maintaining fibre and

connections adds considerably to system cost and complexity. However, the main advantage of directional couplers and relational devices, is their ability to pass a huge bandwidth of optical signal. Once set up, these switches remain in whatever state, passively relating their inputs to their outputs. The transparency of the switch to the signal passing through it enables very high throughput signal routeing to be implemented. However the switch is wholly insensitive to the bits passing through it, so that no form of optical processing logic can be carried out. Control of the switch is therefore electronic and therefore its speed is limited to that of electronic controlling elements [30].

As higher and higher bit rate transmission systems are being developed, there is a pressure to build faster and faster switching systems to switch these complex signals. In transmission systems, the high bit rate signal only passes through a few elements as it is generated or processed. This allows quite high speed operation, since all the controlling electronics can be placed in close proximity, allowing high data processing rates over small interconnection distances. In a switching system however, the signal must pass through a large number of switching elements which are spread over a much larger area. This makes high bit rate electronic switching much more difficult. A partial solution to this problem is to trade-off between the complexity of the transmission and the switching systems used [17]. One solution which is currently being implemented is that of the Synchronous Digital Hierarchy (SDH) or the Synchronous Optical NETwork (SONET) [31], where the transmitted signal format is of a block-multiplexed format rather than a byte or bit-multiplexed time division format. In this transmission hierarchy, the switching system can operate on a signal or block directly, rather than having to demultiplex the information and switch at very high bit-rates. This synchronous architecture removes the need for requiring large demultiplexer/multiplexer mountains to remove or add a signal to the high bit rate stream at each node in a network. Switching is also carried out at much lower bit rates as large blocks of data (2430 bytes: SDH STM-1) can be switched at 125μs rather than the bit or byte switching of data in ns's.

Another proposed transfer mode is known as Fast Packet Switching (FPS) [32] or Asynchronous Transfer Mode (ATM) [33]. ATM is the CCITT (International Consultative Committee for Telephone and Telegraph) target transfer mode for broadband ISDN (ie. the transmission of broadband multiple bit-rate services). This is a fixed size packet based architecture in which packets or cells of 53 bytes (5 bytes destination address and 48 byte information payload) are statistically multiplexed on to high bit-rate carrier channels. Each cell is conveyed to its destination address over the network in exactly the same way, regardless of its service source. Higher bit-rate services simply transmit more cells in order to satisfy their higher bit-rate demands. Loss sensitive services such as computer data or delay sensitive cells, perhaps originating from telephony calls, can be assigned 'priorities' ensuring their safe and timely delivery.

An evolutionary step towards a full asynchronous transfer network is the mapping of ATM cell streams onto the payload of a much larger synchronous packet or time frame which provides an intermediate solution which allows the statistical multiplexing of asynchronous cells on to a synchronous framework which is compatible with the current

telecommunications network. A number of ATM cells destined for the same destination are grouped together and placed in the Synchronous Payload Envelope (SPE) of a larger, synchronous packet or cell [31]. This allows the network switching speed constraints to be relaxed as frames consisting of many ATM cells are switched at say the current 125μs (8000 Hz) rate as opposed to individual cells (of 53 bytes) being switched at much higher rates.

Given the dramatic increase in processing overhead by switching individual ATM cells rather than using current circuit switched techniques, it would be very desirable for individual ATM cells to be able to self-route through a switch to their network destinations. One such switch type is the Batcher-Banyan routing network of which the 'Starlite' switch is an example [34]. At each stage in this switch, a simple logical operation is performed on the cell header which determines whether the cell is exchanged or bypassed. This is a non-blocking switch architecture whose size scales very favourably with switch size. It would of course be very convenient to be able to perform this logical operation and self-routeing, optically and 'on-the-fly', thereby distributing control of the switch and the routeing of cells over the entire switch fabric. To implement in electronics, this normally requires a small processor with order of 100 gates per exchange-bypass stage.

The problem in implementing a packet switching system using relational devices (eg. directional couplers) is that a packet header or destination address has to be read and some decision made, in order to determine whether the packet should be routed through the switch (ie. exchanged or bypassed). This can be achieved by the use of an electrical overlay network which controls the routeing of the optical signals through the switching fabric (figure 1.1) [35]. A portion of the optical power is stripped off from the incoming optical signal and the packet header is monitored electronically with the state of the relational switch being set accordingly. The header information could be at a lower bit rate than the ensuing data so that the electronic processing could be done at reasonably low operating speeds allowing the slower speed electronics to switch an higher bit rate optical signal. However, if the header bit-rate is the same as the data, then the speed of the switch is limited by the speed of the electronic control overlay network. The cost of such a system is mainly that a large amount of electronics surrounds and controls a small number of photonic switching devices. For this to be economical, large packet lengths are required so that the amount of processing required per bit transmitted is reduced.

If however a photonic relational device existed that exhibited sufficient 'intelligence' to be able to perform a simple routeing operation, then it might be worth while doing the packet switching entirely optically rather than having to expensively integrate the two technologies side by side. Even though electronics is the main contender for processing applications, if the operation is simple enough, (ie. the system is I/O bound rather than processor bound), then optical processing logic might prove more advantageous rather than having to combine the two types of switching technology. What is required is a device that combines the advantages of relational switches (ie. high bandwidth and transparency) with those of optical logic switches which are bit sensitive and have the potential for logical operation.

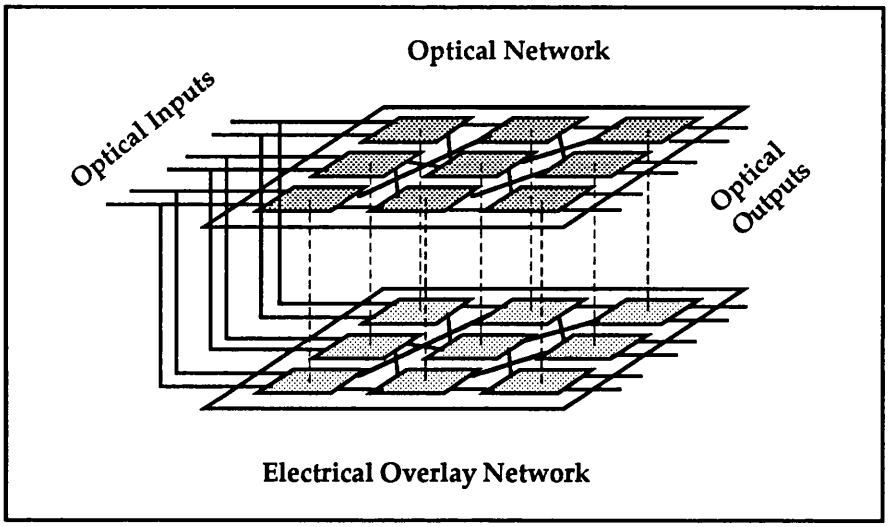

Figure 1.1 Electrical overlay of an optical network

The characteristics of the various logic devices available, ie. relational devices (high bandwidth and data transparency, but no logical operation) and logical devices (optical processing functionality but much lower bandwidth) are such that neither class of device offers the perfect switching solution: ie. Bandwidth and Intelligence. This leads to the question that perhaps the advantages of both can be used in some 'hybrid' device based, switching fabric. Up until quite recently however, it has been difficult to consider the usage of current optical logic devices in real systems applications. High power, critical biasing and accurate temperature control device requirements have meant the slow evolution of these devices from the laboratory into practical systems. However, the SEED and in particular the symmetric or S-SEED, overcome many of these difficulties [24]. Its dual-rail differential logic operation, low switching energies and wide bistable hysteresis width lend it to some very interesting systems applications. The S-SEED has already been proven useful in optical computing applications such as optical clock extraction [36] and wavelength modulation/conversion [37]. It can also be used as a self-linearised modulator [38] or an optical 'tap' [39]. A whole range of SEED devices can now be fabricated in large arrays [40] and with varying operating characteristics, such as very high contrast [41] and low operating voltage [42]. It is shown in chapter 4 of this thesis how the S-SEED can be used in a manner which gives to it, the properties of a combined logic and relational device (ie. passive or relational switching with intelligence). For this device, functionality very similar to that required in a self-routeing, all-optical packet switch is demonstrated [43-44]. Optimisations, switching speeds and other systems considerations for S-SEEDs operating in such a dual mode are also discussed.

As optical interconnection technologies mature, the distances over which optics is used to enhance electronic processing will reduce. High speed optical fibre backplanes have been made for computer rack systems and the optical 'printed circuit board' is virtually a reality [45]. In these optical bus implementations it is extremely desirable to be able to see into or 'tap' a portion of an optical bit stream without destroying it. Such a

'tap' can be implemented using SEED technology and is proposed and demonstrated in chapter 3 of this thesis [39]. This device configuration can 'tap' as much or as little of an incident optical signal as is required without destroying the signal. This device can also be controlled in such a way as to be able to give high contrast linear modulation characteristics so that the same device can act as a receiver or a transmitter node in an optical bus configuration. Thus this highly functional element can be used in a dual mode (receive or transmit) in the node interface of say an optical bus or rail-tap system. Also, a very compact and useful systems application is proposed which uses the SEED tap in a single stage, self-configuring, optical to electronic, serial to parallel convertor. This architecture serves as a demonstration of how optical technologies may be applied, in order to implement functions much more simply and elegantly than by using conventional electronics-only techniques.

It is indisputable that optics will continue to play an increasingly important role in communication and processing systems, where current systems are reaching certain electronic systems limitations which only a conversion to optical technology can solve. It is clear however, that due to lack of integration capacity and relatively large device sizes and switching energies, optics will not replace electronics in compex processing systems. However the use of photonics and optoelectronics technologies in future processing and telecommunications applications should not be underestimated. It is hoped that this thesis will give the reader some understanding of how optics can be judiciously used in conjunction with electonics, to yield much simpler, more efficient and robust systems than was previously possible

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CHAPTER 2

Self Electro-optic Effect Devices

Optical communications systems employing single frequency lasers have already been implemented to huge effect in high capacity, optical fibre, long-haul terrestrial telecommunications networks. Such systems take advantage of the single frequency nature of these light sources so as to avoid the large power penalties that would result if multi-frequency services were used in fibre systems having significant dispersions (≈2ps/km nm). However, even single frequency laser sources are not ideal because upon direct intensity modulation, their wavelengths shift or 'chirp' [1]. If the laser is operated in a continuous mode however, and its light is modulated 'externally', then it is possible to virtually eliminate laser frequency chirp. Improved optical output power may also result as the requirements on the laser source are relaxed. Higher modulation speeds will also be possible because the modulators used may be made very small, with low capacitance and low operating voltages enabling very high speed operation [2]. Further advantages to be gained by using the external modulation of lasers are that the laser source can be located off-chip, reducing the on-chip power consumption and additionally, a single optical source beam can be split and used for multiple signals. It may also be possible for the external modulator to be more easily integrated onto a VLSI chip [3].

External intensity modulators are generally of two types: Phase modulators in a Mach-Zehnder [4] or coupler configuration [5], or through electroabsorption [6]. The phase modulation effect of the first group of modulators can be achieved through either the electro-optical [7] or the stronger electro-refractive effect [8]. The electroabsorption modulator however, is a simpler alternative and is discussed in the following sections. The multiple quantum well (MQW) electroabsorption modulator is discussed and a particular use of MQW modulators, which will be described, is the Self Electro-optic Effect Device (SEED), which under certain conditions can exhibit bistability and perform optical logic functions.

2.1 Electroabsorption modulators

Electroabsorption modulators are devices which can modulate an incident optical beam by absorbing a certain fraction of the optical power incident upon it. The fraction of the incident power absorbed is controlled by a voltage applied across the modulator. Electroabsorption modulators are in general made from semiconductor materials which absorb light by means of optically induced transitions of electrons from the valence to the conduction bands of the material.

The proportion of the incident optical power absorbed, upon passing through the modulator, is known as the 'absorption', A, of the modulator and is dependent on d, the length of the absorbing material through which the light passes. The amount of optical power absorbed also depends on the absorption coefficient, α (cm^{-1}), of the material, which in turn depends on the wavelength of the light used and on the electric field applied. For general consideration, it is assumed that the device absorption coefficient is independent of the optical power incident on the device, however for high powers this assumption is no longer valid as 'saturation' of the material can occur (5.6).

2.1.1 Theory of operation

Electroabsorption modulators utilise changes in the absorption of light, with photon energies close to the band gap of a semiconductor material, upon the application of an electric field. This change in absorption leads to a change in transmission of the light through the modulator. The transmitted optical power through the device can therefore be modulated by varying the electric field and thus the absorption of the device.

Upon application of an electric field, for bulk semiconductors, the valence and conduction bands tilt, allowing less energetic electrons to cross between the bands. There is a field-induced broadening effect and the band-edge is effectively broadened. This is known as the Franz-Keldysh effect [9] and by shining incident light of wavelength corresponding to the band-edge of the material used, this effect can be used to modulate an incident light beam. However, much larger changes in absorption with electric field can be achieved for multiple quantum well material. When the thickness of a semimetal or semiconductor, L_z is reduced to a size of order $\approx$ 500 Å, effects not typical of the bulk material, known as quantum size effects occur. Quantum wells are very thin layers of two different semiconductor materials (figure 2.1a) which have different band energies. For the case of GaAs-AlGaAs quantum wells, the band gaps of GaAs and AlGaAs differ depending on the Aluminium content and there is consequently, a discontinuity in the energy gap at their interface. The periodic nature of the structure (GaAs-AlGaAs-GaAs-AlGaAs-...etc.) results in the formation of potential wells, confining the electrons and holes in the lower gap or well material, in this case GaAs. When the well thickness $L_z <$ $\approx$ 500 Å), size quantization occurs, causing changes to the density of states distribution in the valence and conduction bands and hence to the shape of the absorption spectra of the material. The quantum well layers are so thin that electrons and holes trapped within them can not move freely in the lateral direction (ie. in the growth direction) unless they are energetic enough to surmount one of the barriers [10]. The particle is therefore confined in one-dimension. The behaviour of this 2-dimensional material is very different from the 3-dimensional behaviour which takes place in bulk semiconductors. These differences are as follows:-

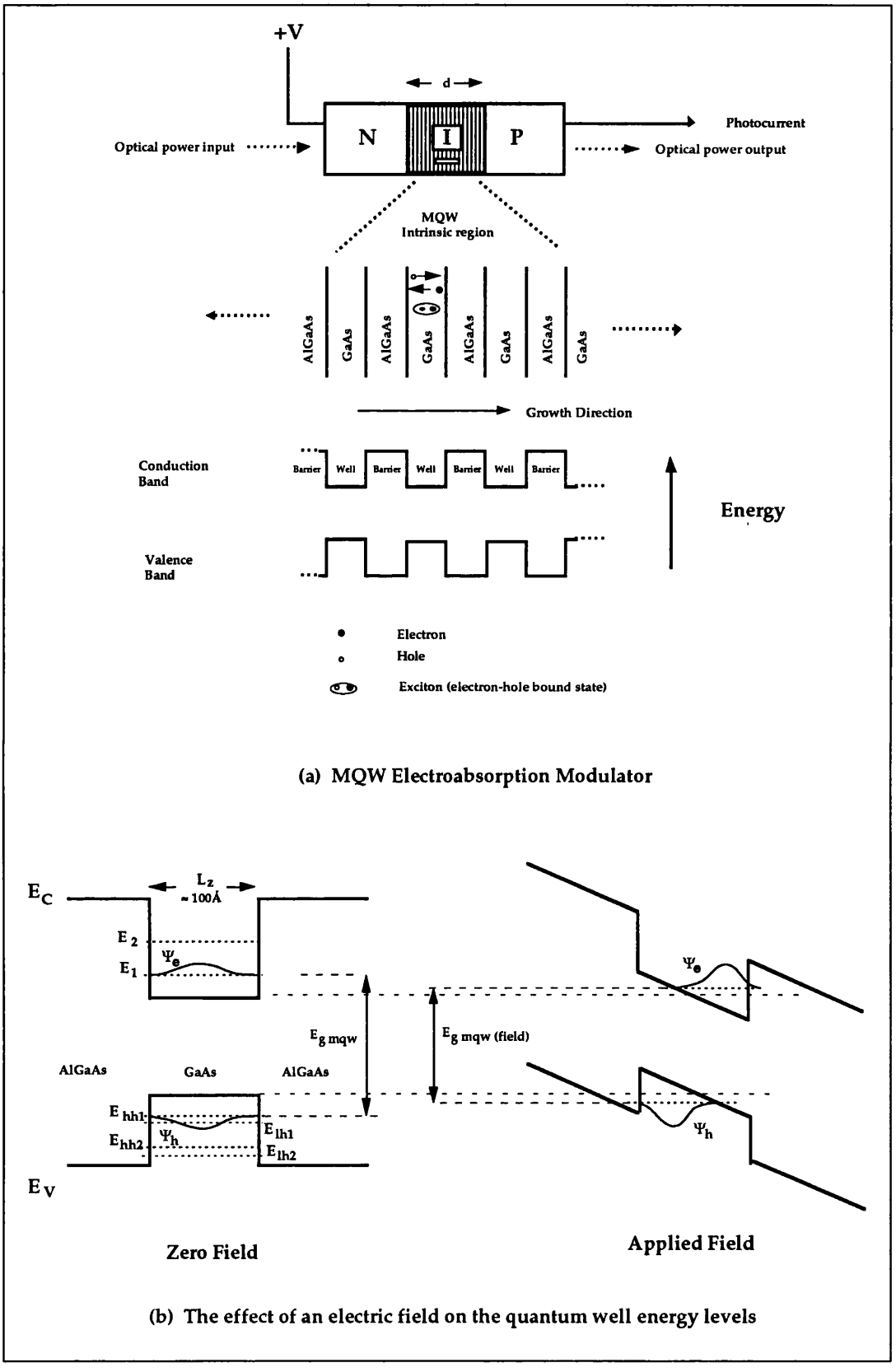

Figure 2.1a MQW modulator structure

Figure 2.1b Band diagram of the effect of an applied field on a quantum well

For bulk or '3-D materials', for photon energies greater than the band gap, the absorption coefficient, α of the material increases with increasing energy. The density of states increases approximately parabolically with increasing photon energies (figure 2.2). For 1-dimensional confinement however (quantum wells), due to quantum size effects, only certain discrete energy levels are available in the direction of the confinement, although many energy levels are still available in the non-confined direction. Quantum confinement also lifts the degeneracy of the valence band and leads to the observation of two sets of subband transitions, namely the heavy and light holes. A potential well exists in the conduction and valence bands giving rise to a series of bound states for the electrons, E_n, and E_{hhn}/E_{lhn} for the heavy and light holes respectively. Below the energy, E_1 there are zero allowed electron states (figure 2.1a). Then as shown in figure 2.2, a sub-band with a constant density of states (per unit area) begins at E_1 ($E_{g\,mqw}$), followed by another block of states appearing at E_2 etc. [11]. The result is that the quantum well material has a 'step-like' density of states. Looking from the outside, it appears that a quantum well has a small number of discrete energy levels available, but each level may accept a large number of particles. The energy levels are said to be 'quantised' in both the valence and conduction bands and the absorption spectrum of the 2-D material consists of a series of steps, with the first step occuring at an energy, E_1 a little greater than the band gap of the material in bulk form, $E_{g\,bulk}$. The probability of absorption at a particular energy is related to the spatial overlap of the wavefunctions ψ_e and ψ_h, in the corresponding conduction and valence band states. A related quantity is the 'oscillator strength' for the optical transition which is proportional to the square of the overlap integral and ultimately determines the absorption coefficient, α of the material [12]. Quantum wells are grown alongside each other in order to increase their total absorption. The resulting multiple quantum well material should have the wells sufficiently separated (ie. the barriers must be sufficiently wide $\approx$ 50Å), so as to avoid coupling between wells. Coupled quantum wells can be used however, to enhance material performance for use in certain systems applications [13, 14, 15], (5.4).

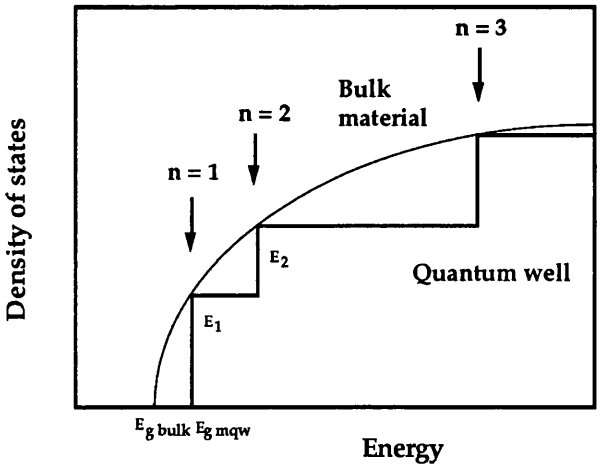

Figure 2.2 Density of states profile for bulk and MQW materials

Extra energy transitions are seen just below the sub-band of each energy transition, E_n. These are exciton states which occur when the electron and hole formed by the absorption of a photon, have insufficient energy to escape from each other and hence form a bound state. This state is confined in three dimensions by the coulomb interaction between the two particles, and as such, has a well defined energy level rather than forming part of the continuum. The energy required to create an exciton is given by:

$$E_{ex} = E_g + E_{e1} + E_{hh1} - B$$

Where E_g is the band-gap of the GaAs well material, E_{e1} and E_{hh1} are the energies of the electron and hole respectively and B is the exciton binding energy.

In a bulk material like GaAs, the exciton binding energy is very small and therefore excitons are visible only at low temperatures. Increased temperature broadening due to increased phonon interactions occurs, so that at room temperature the material does not have a sharpened excitonic absorption peak. In multiple quantum well material however, at room temperature, as a direct result of confinement, the exciton shrinks in size. Its binding energy, B, is thus increased which reduces the probability of phonon ionisation. Although phonon energies are still larger, the exciton has a sufficiently long lifetime so that it can be observed at room temperature. The exciton is therefore stable in multiple quantum well material at room temperature, its strength is increased and sharply enhances absorption at a place where the absorption edge is already sharp [16]. Therefore the absorption curve for a 2-dimensional material follows the density of states function (figure 2.2), with additional absorption due to excitonic absorption at the transition. In the GaAs system there are two excitons at the transition caused by confinement splitting the hole energy into two (the light and heavy holes). For 2-D materials, as for 3-D materials, an applied electric field causes the bands to tilt, thus changing the shape of the wells (figure 2.1b). New quantised energy levels (at energies lower than before) are formed, which implies that the band-edge moves to a lower photon energy. Absorption may also fall, but the band-edge generally shifts as a step, therefore greatly increasing the material absorption for photons with energies just below the band gap under zero electric field. When an electric field is applied, the carrier wavefunction ψ_e and ψ_h are polarised towards the walls of the well: the electrons on one side, the holes on the other. The height of the exciton resonance is proportional to the overlap of the appropriate electron and hole wavefunctions. Thus under an applied electric field, the overlap decreases, as does the height of the exciton peak. Also, the wavefunctions are no longer symmetric about the mid-point of the well. This means that previously forbidden energy transitions, with initially low overlaps, become allowed and new peaks appear in the absorption spectrum. The exciton absorption peak is thus reduced in magnitude and is broadened. The exciton shifts with the band-edge however so that it still enhances absorption at this point. This change in absorption is usually explained as the Quantum Confined Stark Effect (QCSE) [17], the shift in subband energies as the wells are tilted. The exciton binding energy is also proportional to the

quantum well width used [18] and also for narrower wells, the increase in confinement gives increased electron-hole wavefunction overlap, giving increased oscillator strength and a larger exciton to continuum height ratio.

MQW material is therefore useful for electroabsorption modulators because of the large changes possible in its absorption coefficient, due to the sharp band-edge of the material, which moves more or less intact with an applied electric field. Thus absorption of light may change from a very low value to a large value, upon application af an electric field. The presence of excitonic absorption enhances the material peak absorption even further, although it does cause a broadening of the band-edge with applied field. Multiple quantum wells are generally grown alongside each other so as to increase their total absorption. It has been shown [19] that in the limit of infinitely wide wells, bulk behaviour (ie. the Franz-Keldysh effect) is recovered. The 'height' of the well barriers is significant when the speed and saturation performance of these devices are considered, (chapter 5). Also for high barriers, confinement of the particles is enhanced and the wavefunctions for the electrons and holes are stronger within the wells thereby increasing the electron-hole overlap and overall absorption [10].

The idea of using quantum wells is not new. It has only been recently however that semiconductor fabrication technology has allowed the high quality material required to be produced. The growth process used in fabricating all the MQW structures used in this thesis is metal organic vapour-phase epitaxy (MOVPE) [20, 21]. All the material was grown at the SERC central facility for III-V materials at the University of Sheffield. The multiple quantum well modulators referred to in this thesis all use the GaAs/AlGaAs material system. This material has been studied extensively in recent years and exhibits strong absorption changes with applied electric field. However, the principles described in this thesis are equally applicable to other material systems at different operating wavelengths and which may improve device performance for certain systems applications.

2.1.2 Multiple quantum well modulator structures and characteristics

In order to apply an electric field across the quantum well material, and avoiding large currents, the quantum well material is usually encapsulated within the intrinsic or i-region of a pin diode structure (figure 2.1a). The p and n-type materials should ideally be transparent to the wavelength of light at which the modulator is intended to be used. This is achieved by using materials with a larger band-gap than the quantum well material. When this structure is reverse biased, there is only an extremely small 'leakage' current that flows. The intrinsic active region is depleted of carriers and the only way current flows is if carriers are generated within the intrinsic region by photogeneration. Electroabsorption modulators also behave as photodetectors. When a photon is absorbed, an electron-hole pair is generated. In the presence of an electric field, the electron and hole are swept out of the intrinsic region and collected at the device

terminals. The ratio of electrons (holes) collected at the device terminals to the number of photons absorbed, is known as the device quantum collection efficiency, η. η is strongly voltage dependent because in a strong electric field, carriers are swept out of the device intrinsic region more quickly than in a weak field, thus there is less likelyhood of recombination occurring. The physical mechanisms of carrier escape from the MQW region are primarily by either thermionic emmission or a resonant tunelling process or a combination of both. There is some debate as to the exact interaction between the two and which of the two is in fact the dominant mechanism [22]. By increasing the speed of the carrier escape mechanism, these devices can be made to operate more quickly. This and other speed considerations for this class of device will be addressed more fully in Chapter 5 of this thesis. The doping of the intrinsic region should be as low as possible. This is so that all of the quantum wells within the intrinsic region experience the same electric field applied. For high intrinsic doping, each well experiences a different electric field, thus different excitonic shifts etc. take place, thereby effectively broadening the absorption spectrum of the material.

Quantum well modulators can be made into two geometries (figure 2.3): The first with the light travelling parallel to the wells, within a waveguide type structure [23, 24] and secondly with the light propagated perpendicular to the transverse structure [25]. Waveguide modulators are useful as they offer a much longer interaction length between the light and the quantum wells and therefore better depth of modulation can be obtained. The main benefit of the transverse or 'surface-normal' type structure, is the ease with which light can be coupled into and out of the devices using free-space optics. Coupling light into and out of waveguide modulators can incurr significant losses (ie. increased insertion loss to the system) and also optical polarisation considerations have to be taken into account.

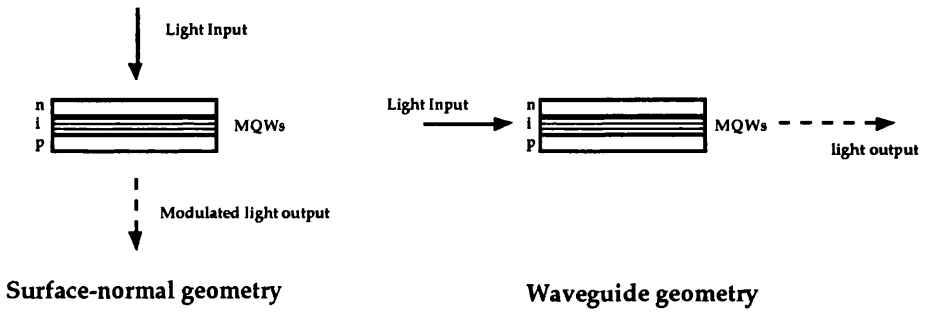

Figure 2.3 Electroabsorption modulator geometries

There are two distinct types of surface-normal modulators: Non-resonant modulators with anti-reflection coatings on one or both surfaces, or resonant modulators with reflections from both surfaces (figure 2.4). The non-resonant modulator is limited in its achievable modulation contrast by the thickness of its absorbing region. A mirror grown on

the back surface changes a transmission modulator to a reflective one, with enhanced absorption due to the doubling of the optical interaction length [26]. The resonant asymmetric Fabry-Perot modulator [27], allows multiple passes of light within a cavity through the absorbing well region. This effectively increases the optical interaction length of the device without altering the number of quantum wells, thereby decreasing the applied voltage required for a given electric field across the wells. It is in fact possible to achieve 100% absorption of light under certain conditions, thereby effectively giving an infinite contrast ratio which proves useful in optical communications systems requiring low cross-talk and high extinction ratios. It is the principle of the asymmetric Fabry-Perot modulator, which has been used in my research and which is described in this thesis, to enhance the performance of a range of optical logic devices, based on the multiple quantum well electroabsorption modulator.

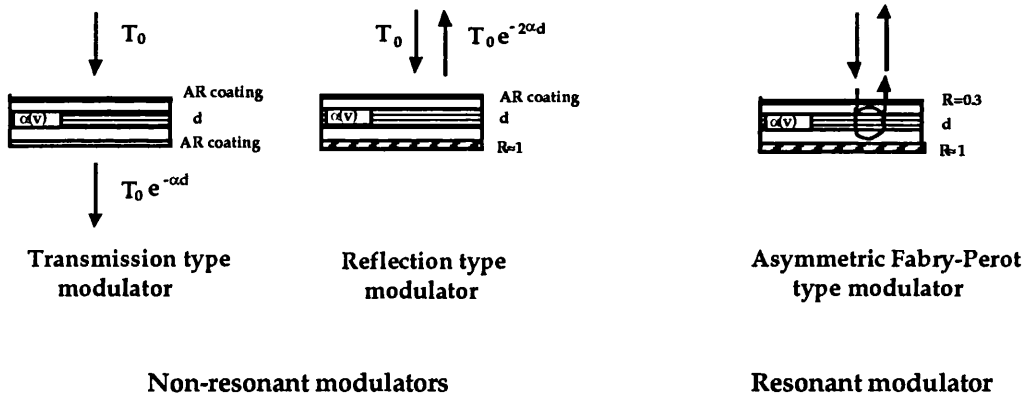

Figure 2.4 Non-resonant and resonant electroabsorption modulators

For the effective modulation of light, modulators need to work at wavelengths where the change in absorption, $\Delta\alpha$ with applied electric field is the largest (figure 2.5). There are two different possible ways of operating the modulator. By using a wavelength corresponding to the zero-field, e1-hh1 exciton, upon increasing device bias, by way of the QCSE, decreasing device absorption occurs due to the red-shifting of the band-edge and the exciton moving to lower photon energies. This is known as the 'bias-transmitting' or the 'normally-off' mode of operation and its associated wavelength of operation is $\lambda_{b\text{-}t}$. The alternative modus operandi is that obtained when operating the modulator at photon energies just below the band-edge of the MQW material used. Upon increasing the electric field, the exciton red-shifts by way of the QCSE, increasing device absorption at this point. This is known as the 'bias-absorbing' or the 'normally-on' mode of operation and its associated wavelength is known as $\lambda_{b\text{-}a}$. The difference in operation between the two wavelengths can be made use of in various device configurations, as will be seen in the following sections.

The overall change in transmission ΔT, through a single-pass, electroabsorption modulator (figure 2.4) is given by the formula:

$$\Delta T(\Delta V,\lambda) = \exp(-\Delta\alpha(\Delta V,\lambda)d)$$

Where ΔT is the change in the fraction of transmitted light through the modulator, $\Delta\alpha$ is the change in the absorption coefficient of the MQWs (dependent on ΔV and λ) and d is the depth of the absorbing region (number of wells x well width). The change in transmission/reflection, ΔR is increased for the double-pass device for the same MQW structure (figure 2.4) and is given by:

$$\Delta R = \exp(-2\Delta\alpha(\Delta V,\lambda)d)$$

For the resonant device, the device characteristic equations are a little more complicated and are shown in Appendix A. The asymmetric Fabry-Perot device structure and behaviour is explained in section 2.5 of this chapter.

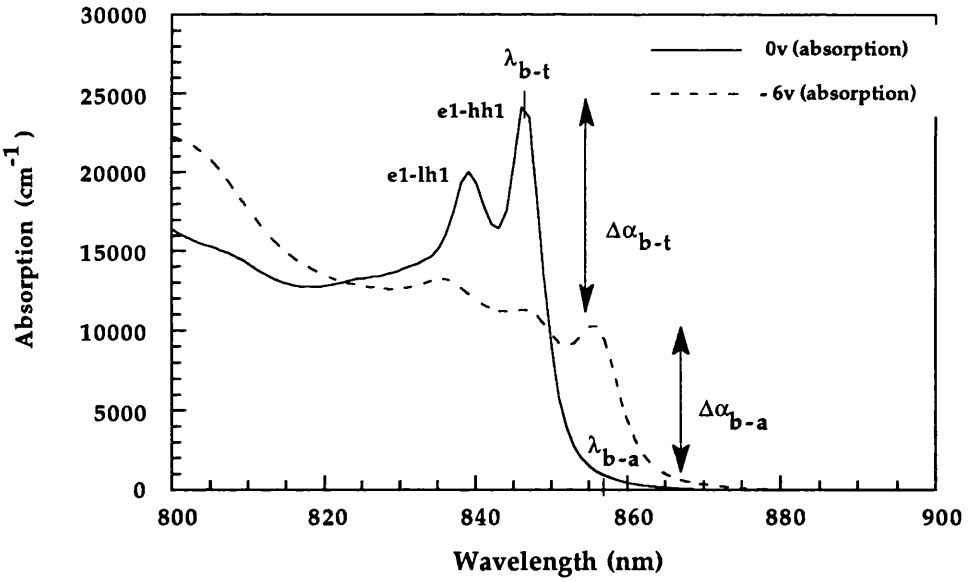

Figure 2.5 Two different modes of operation of an electroabsorption modulator

2.2 SEED theory and principles of operation

The basic principle of a SEED [28-45] is that photocurrent flowing through some electronic circuit influences the voltage across a multiple quantum well electroabsorption modulator (figure 2.6). The voltage across the modulator in turn affects the absorption of light by the modulator, which in turn influences the photocurrent through the external

circuit. A feedback mechanism is thus established. It is the sign of this feedback which determines how the SEED behaves.

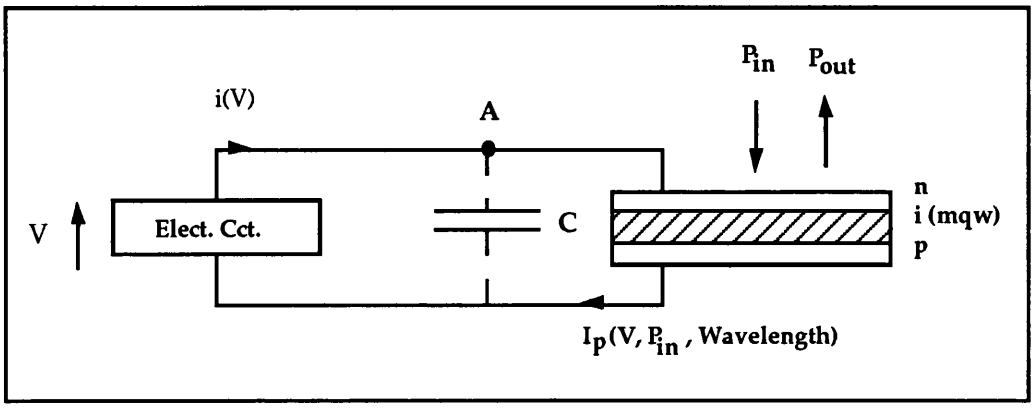

Figure 2.6 Generalised schematic diagram of SEED configuration

When i(v) is not explicitly dependent on time (ie. it doesn't contain capacitors, inductors or time-varying drive voltages), we can deduce the behaviour of the circuit at a given equilibrium state, by performing a linearised stability analysis [30].

Performing a stability analysis on the generalised SEED schematic, figure 2.6: For a small change in voltage, v at node A, the change in current charging the effective device capacitance C, is equal to the change in current flowing through the external circuit subtracted by the change in photocurrent flowing through the modulator. (ie. The electronic circuit acts to charge up the device capacitance, C and the device photocurrent, I_p, acts to discharge C).

$$C\frac{dv}{dt} = \left[\frac{di}{dv} - \frac{dIp}{dv}\right]v$$

$$\Rightarrow C\frac{dv}{dt} = [\,]\,v$$

$$\Rightarrow C\frac{dv}{v} = [\,]dt \quad \Rightarrow \quad \int\frac{dv}{v} = \int\frac{[\,]}{C}dt$$

$$\Rightarrow \text{Ln } v = \frac{[\,]t}{C} \quad \Rightarrow \quad v = e^{[\,]t/c}$$

If [ ] < 0, feedback is negative and v is stable, optical level shifting and self-linearised modulation are possible (see chapter 3). If [ ] > 0, the feedback is positive, v diverges, is unstable and bistability or oscillation are possible.

The magnitude of [ ], determines how quickly v changes. The greater [ ], the faster the

divergence. If [ ] = 0, v takes an infinite time to diverge. This is the characteristic of 'critical slowing down' [46]. Divergence of v, discharge of C, would take longer with a small photocurrent/incident optical power than with a larger photocurrent. If the photocurrent is greater than the external circuit current, then the device discharges. And vice-versa, if the external current is greater than the photocurrent, then the device charges. The greater the difference in currents/incident optical powers, the faster the charging/discharging of C. If the photocurrent is only slightly smaller or larger than the external circuit current, then switching would take very much longer.

In the SEED circuit configurations considered here, electronic circuits exhibiting a positive slope resistance were used:

ie. $\frac{di}{dv}$ is - ve, using the current convention as shown. Thus + ve feedback is only possible

when $\frac{dIp}{dv} < 0$ and then only when $\frac{dIp}{dv} < \frac{di}{dv} < 0$ (equation 2.1)

Therefore positive feedback is only possible when *decreasing* photocurrent through the modulator is observed for *increasing* applied device bias - negative device resistance.

How does one achieve this 'negative resistance' and positive feedback in an actual device? One way of observing this effect is by operating the device at a wavelength corresponding to the unbiased e1-hh1 exciton peak, λ_{b-t} (2.1.2). Upon applying an electric field perpendicular to the thin quantum well layers, by way of the Quantum Confined Stark Effect (QCSE) [17], the band-edge absorption and excitonic features are red-shifted to lower photon energies and the absorption of the multiple quantum well structure falls. Therefore for increasing electric field across the multiple quantum wells, one sees decreasing device absorption and hence decreasing photocurrent, ie. 'negative device resistance'.

2.3 Different SEED configurations

By varying the characteristics of the electrical feedback circuit in series with the MQW modulator, different device functionality can be attained. Some of the many possible variations of SEEDs are explained in the following sections

2.3.1 The R-SEED

The simplest type of SEED is the Resistive or R-SEED [30] in which a MQW PIN modulator is reverse biased in series with a resistive load (figure 2.7). This is a single input, optically bistable device whose operating state is controlled by the power of an incident light beam. Initially, with zero optical power incident on the device all the

supply voltage appears across the photodiode. When light starts falling on the device, photocurrent is generated and a voltage drop can be observed across the resistive load. This voltage acts to reduce the voltage seen across the diode.

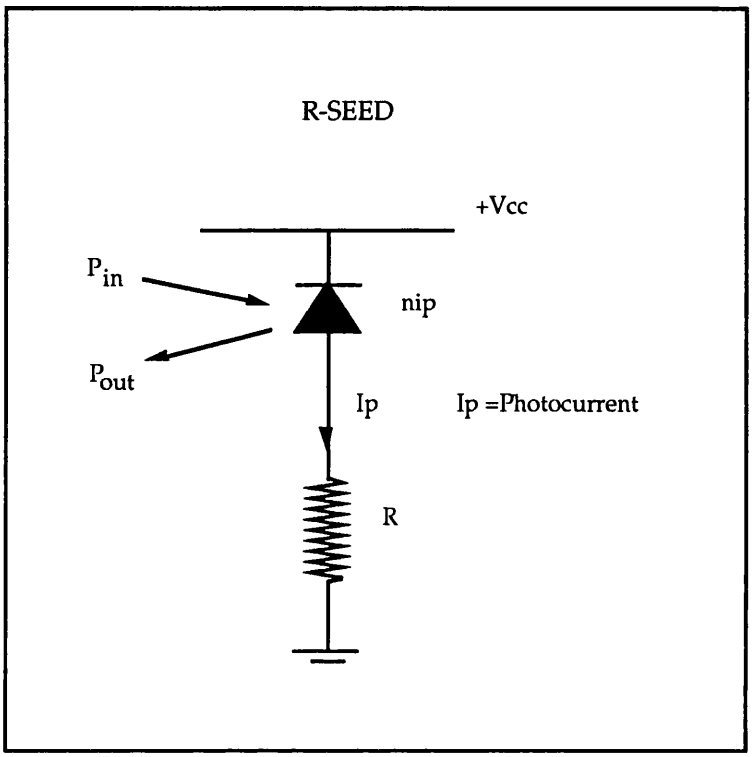

Figure 2.7 Resistive or R-SEED configuration

For light of the correct wavelength, $\lambda_{b\text{-}t}$, at a certain critical incident optical power intensity, P_{crit}, the voltage across the device is such that any further decrease in diode voltage would cause the diode voltage to enter its region of 'negative resistance'. A further drop in diode voltage gives rise to increased photocurrent, leading to increased voltage across the resistive load, giving decreased device voltage which in turn gives increased photocurrent, and so on. This positive feedback causes the SEED to 'switch' its point of operation from a voltage one side of the diode's region of negative resistance to the other. This switch in device voltage gives rise to a corresponding change in the device's absorption of light, by way of the QCSE. The behaviour of the R-SEED is easy to understand through the use of a graphical loadline analysis (figure 2.8).

The three curved lines are schematic photocurrent versus applied reverse bias characteristics for a MQW modulator (operating at $\lambda_{b\text{-}t}$), for three different optical input powers, $P_2 > P_{bistable} > P_1$. The dashed straight line is the loadline imposed on the circuit by the resistive load, R. The intercept of this line with the x-axis is the R-

SEED supply voltage, V_{CC}. Note the voltage range corresponding to decreasing device photocurrent for increasing device bias, ie. negative device resistance.

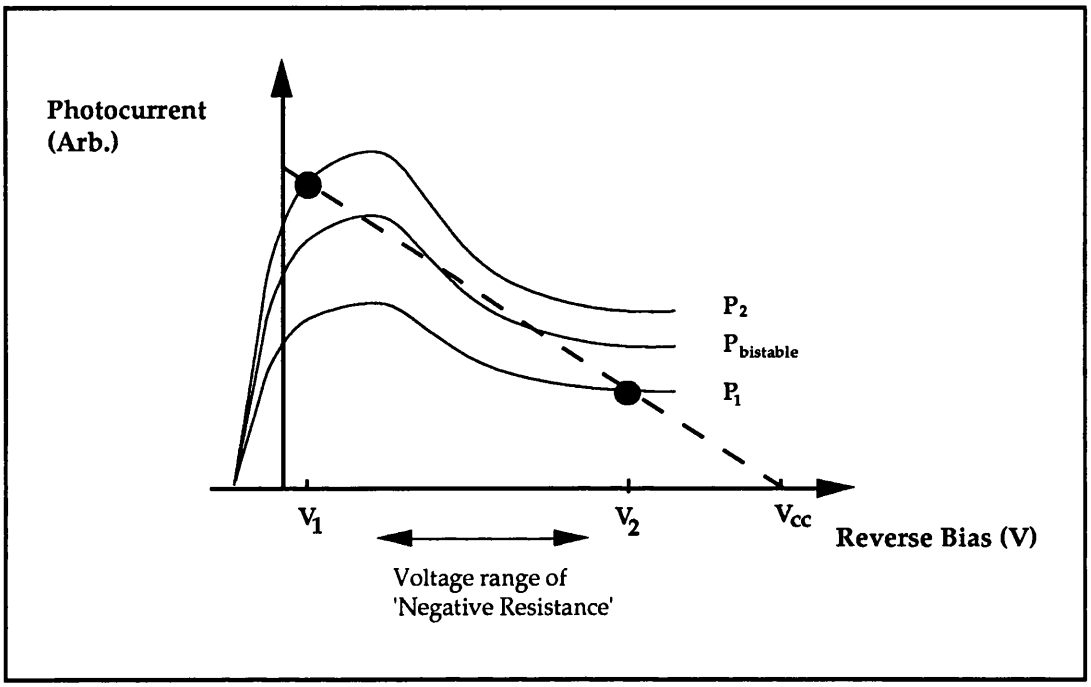

Figure 2.8 R-SEED graphical loadline analysis

The two curves corresponding to incident optical powers, P_2 and P_1, have only one intersection with the resistive loadline at corresponding voltages across the MQW modulator, V_2 and V_1, either side of its region of negative device resistance. At $P_{bistable}$, the loadlines intersect at three points. Two of these possible operating points are stable, the middle one is unstable, since at the midpoint, $\frac{dIp}{dv} < \frac{di}{dv} < 0$ and positive feedback causes the device to change its operating point to a stable one (see equation 2.1). Therefore at this operating power the system is bistable and the device can be in either of the two stable operating states.

In this configuration the resistive load and the power supply act to charge up the characteristic device capacitance and the photocurrent acts to discharge the device capacitance. It can be directly inferred that the dominant time constant for the operation of this device is the resistor-capacitor time constant, RC. The optical powers at which switch-up or switch-down occurs are slightly different. This is due to the resistive loadline being shallower than the device negative resistance and results in a bistable hysteresis width. When one of these currents is larger than the other, the device capacitance charges up/down or 'switches' its operating point.

Increasing the value of the resistive load, R, has the effect of reducing the amount of

photocurrent and thus the incident optical power, required for the device to enter its region of negative resistance and thus cause switching. Increasing R, gives switching at lower optical power levels and conversely, decreasing R, gives switching at higher optical power levels. However, increasing R increases the RC time constant for this device. This implies that high power, high-speed switching is possible for low values of the resistive load. Or alternatively low power, lower speed operation is possible for larger values of the resistive load [43]. Similarly, increasing V_{cc}, means a larger voltage drop across R and thus a larger optical power is required for R-SEED switching. {The interplay between the magnitude of the negative device resistance and the value of the resistive load giving the feedback required for switching, is discussed more fully in Chapter 5 of this thesis Optimisation of negative device resistance is also discussed in relation to a number of material characteristics}.

We could switch this device from the high to the low voltage state by suddenly optically creating a charge $Q = C\Delta V = C(V_2 - V_1)$ in the diode, thereby totally discharging the mqw diode capacitance, C. An absorbed optical energy of $E_{opt} = \frac{hc}{e\lambda} C(V_2 - V_1)$ would be required to do this. Since the absorbed optical switching energy E_{opt}, would normally be a fraction of the incident optical energy, E_{opt} sets the scale of the switching energy [44]. For switching with slowly varying powers, the switching energy can be defined as the incident optical power, P_{in} multiplied by the switching time, Δt: $E_{opt} = P_{in} \times \Delta t$. Where P_{in} is the incident optical power and Δt is the R-SEED switching time.

Increasing the incident optical power to values larger than P_{crit}, (the minimum input power required for switching), reduces the switching time, Δt and vice-versa (2.2) (critical slowing down [46]). For large scale integration, low power dissipation and for high-speed applications, the switching energy of these devices should be made as low as possible. MQW device capacitance scales with its area, hence the optical switching energy also scales with device size [38]. Therefore making these devices smaller is an obvious step towards increased switching and system speeds. However, decreasing device switching energies, by way of smaller area devices and lower operating voltages etc. has the disadvantage that with lower and lower values of optical switching energies, statistical fluctuations in incident photons will be enough to cause the device to change states. Therefore for finite contrast devices, ie. logic zero $\neq$ zero transmitted or reflected photons, there is a limit as to how many optical inputs can be fanned-in and summed onto a single device before severe degradation in system bit error ratio (BER) takes place [47]. Thus very high contrast switching devices are extremely desirable in applications requiring low BERs and high extinction ratios (eg. in telecommunications optical routeing applications).

2.3.2 The D-SEED

In the R-SEED, increasing the supply voltage V_{cc}, causes the resistive loadline to become more shallow, so that the condition for bistability is more easy to achieve, since

there are a wider range of input optical powers with three possible operating points. This bistability occurs at higher input optical powers. However, if the resistive load is increased simultaneously, the optical switching power would remain constant. As V_{cc} and R are increased in proportion, the resistive loadline becomes more horizontal and in the limit of infinite voltage and resistance, di/dv=0, bistability is possible with even the slightest SEED negative resistance. However rather than using high voltages, a constant current source would give the same flat response. Connecting a constant current supply in series with a MQW diode, in the presence of negative feedback, causes self-linearised modulation and optical level shifting [30] and is discussed in Chapter 3 of this thesis. Under conditions of positive feedback however, bistability and switching can be readily achieved.

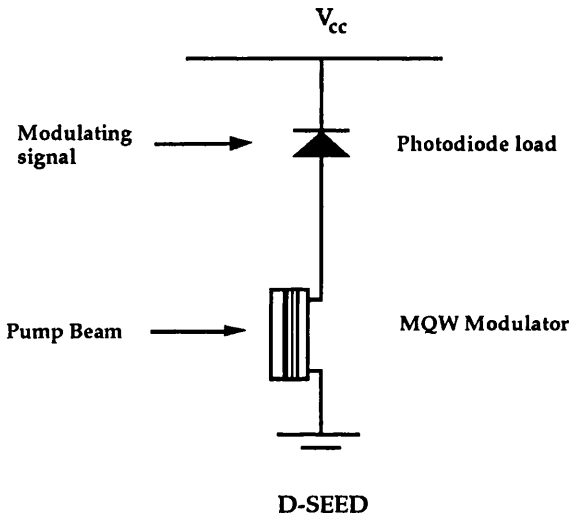

Figure 2.9a The Diode or D-SEED

A good constant current source is a reverse biased photodiode (figure 2.9a). Its photocurrent is directly proportional to its input optical power and its response is flat over voltages greater than about 1 volt. At low voltages, the diode's quantum efficiency falls off and its responsivity characteristic is effectively vertical. The photocurrent versus voltage, loadline characteristic of the diode or D-SEED is shown in figure 2.9b. It can be seen that the reverse supply voltage $V_{cc'}$ required is much less than that for the R-SEED and corresponds to the voltage at the end of the MQW diode's region of negative resistance. It is seen that for the flat responsivity response and the rapid fall-off in photocurrent at low voltages, of the series photodiode, it is very easy to obtain three intersection points and bistability for a range of bias powers, (ie. the bistable loop is wide).

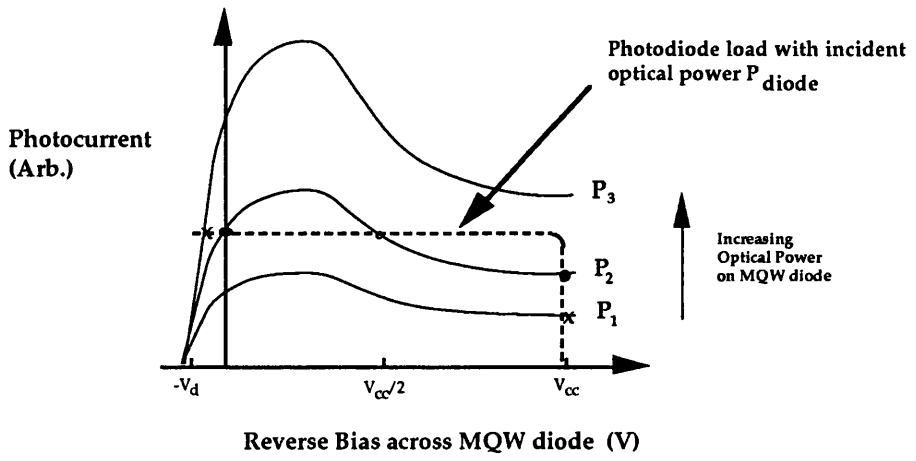

Figure 2.9b D-SEED loadline operation

The required power incident on the MQW modulator to give switching can be set, by adjusting the amount of light incident on the load photodiode, P_{diode} (ie. increasing the light incident on the photodiode, increases the optical power required to be incident on the modulator to cause switching). When the optical power on the MQW modulator is sufficiently greater than that on the photodiode, then all of the supply voltage falls across the photodiode. Conversely, when the optical power incident on the photodiode is sufficiently greater than that on the modulator, then the supply voltage is seen entirely across the MQW modulator. Therefore if the MQW pump beam is held constant, then the signal incident on the photodiode can be used to modulate the pump beam. Device operation is thus possible over a range of input powers set by the magnitude of a control optical signal on the photodiode. This control light beam can be incoherent and broadband so that incoherent-to-coherent, wavelength modulation and conversion can take place [32].

D-SEEDs have been integrated in 2 x 2 [31] and 6 x 6 [33] arrays and the resultant devices can be used as optical dynamic memories. When both beams are removed, it can take up to 30 seconds for the device to discharge due to the diodes' very small leakage currents. If the beams are then simultaneously reinstated, the D-SEED remains in its previous 'memorised' state.

2.3.3 The T-SEED

A variation on the D-SEED is the transistor or T-SEED in which a phototransistor is used as the load of the MQW modulator. Gain in the phototransistor allows a small optical input signal power to generate a large photocurrent which can modulate a large optical pump beam. Under positive feedback, bistability is possible. This device was

proposed in [48, 49] and exhibits a very desirable system device characteristic in that it exhibits 'gain'. The T-SEED is more fully explained in chapter 3 of this thesis as its operation under negative feedback is very similar to that of the self-linearised modulator.

2.3.4 The S-SEED

The Symmetric or S-SEED [34, 36, 37] is configured as two multiple quantum well pin modulators reverse biased in series (figure 2.10a). Each diode sees the other diode as its load. Device operation can be understood by using load lines (figure 2.10b).

The three light solid curves are the photocurrent vs. voltage characteristics for quantum well $diode_1$, operating at $\lambda_{b\text{-}t}$, for three different optical input powers, $P_{in_1} = P_3 > P_2 > P_1$. The dark solid curve is the current characteristic of $diode_2$, for an input optical power $P_{in_2} \approx P_2$, plotted against the voltage across $diode_1$.

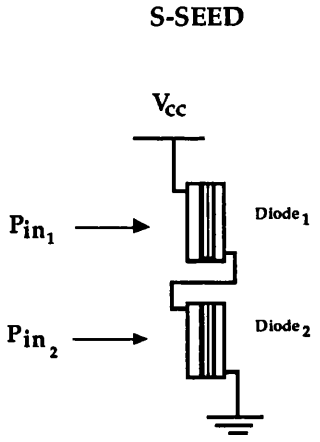

Figure 2.10a Symmetric-SEED configuration

With roughly equal optical input powers on each diode there are three intersections of the load lines. The device is bistable. At intersection point b, $diode_1$ experiences very little voltage across it and $diode_2$ has most of V_{cc} across it. Thus $diode_1$ is in a high-absorbing, low reflecting state and $diode_2$ is in a low absorption state corresponding to high-reflectance. At operating point d, the situation is reversed with $diode_1$ experiencing all of V_{cc} (highly reflecting) and $diode_2$ seeing a very low bias (highly absorbing). The point c corresponds to the unstable case where equal voltages ($V_{cc}/2$) are seen across both diodes.

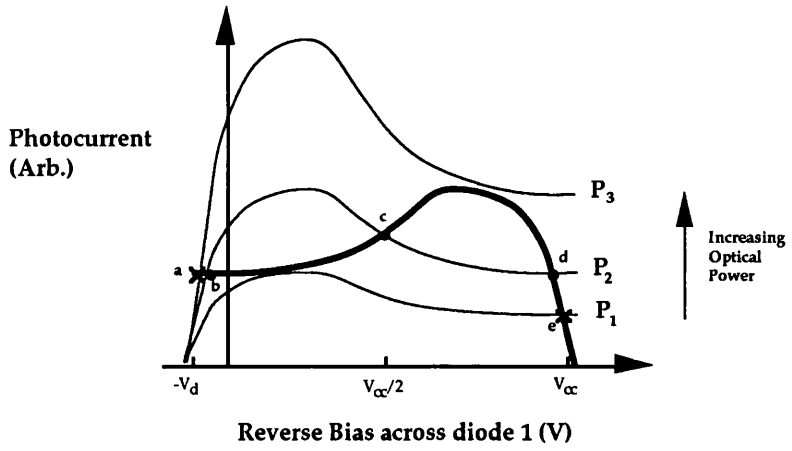

Figure 2.10b S-SEED graphical loadline analysis

For S-SEED operation, two input signal beams are incident on the device. If the difference in power of the two signal beams is sufficiently large, then the device can be forced to operate at either circuit operating point a or at operating point e. The device is bistable in the ratio of its two input beam powers. The S-SEED has a wide hysteresis or bistable loop as can be observed, due to the large power difference between the two input beam powers, P_1 and P_3. From a systems point of view the S-SEED is good because it is quite tolerant to system noise, since a relatively large difference in optical power is required for the device to change its state. (The bistable hysteresis width is dependent on individual mqw modulator absorption characteristics and is discussed in detail in chapter 4 of this thesis).

The optimum bias voltage V_{cc} required for the S-SEED is simply the reverse bias voltage swing required, for the maximum change in absorption of the two single MQW modulators used to make up the S-SEED. For MQW diodes operating as SEEDs ($\lambda_{b\text{-}t}$), maximum absorption occurs at low bias and upon increasing device bias, absorption falls to a minimum. This minima corresponds to the end of the region of decreasing responsivity/photocurrent for increasing reverse bias (negative resistance). For an S-SEED, when the device switches states, $diode_1$ ($diode_2$) sees either a low voltage corresponding to maximum absorption or it sees the supply voltage V_{cc}, corresponding to a minimum absorption. Maximum switching contrast is achieved when the device switches between the two extremes of absorption, therefore V_{cc} is chosen to give a maximum change in absorption, $\Delta\alpha_{max}$, corresponding to a maximum switching contrast for the multiple quantum well structure used.

S-SEED switching time, Δt, is the time it takes to charge the capacitance of each pin diode, by the photocurrent in each diode. Kirchoff's current law can be applied at the

centre node (V_{centre}) of the S-SEED to determine the S-SEED speed characteristic.

$$P_{in_1} S(V_{centre}) - P_{in_2} S(V_{cc} - V_{centre}) + \frac{C dV_{centre}}{dt} - C\frac{d(V_{cc} - V_{centre})}{dt} = 0$$

By assuming constant responsivity S (A/W) for the two diodes [36], a voltage swing V_{cc} in a switching time, Δt. The switching time, Δt can be approximated by:

$$\Delta t \approx C_{tot} V_{cc} / S(P_{in_2} - P_{in_1}).$$

Therefore, maximising the difference between P_{in_1} and P_{in_2}, decreases the switching time, Δt. Also for smaller (lower capacitance) devices and higher optical powers, switching times can be made much faster.

The S-SEED can also be operated as a differential optical modulator, modulating a pair of beams in a complementary fashion, when a single modulating voltage is applied to the centre node between the two S-SEED diodes [36, 40]. This is advantageous because the logic states are now defined by a ratio of beam powers rather than specific power levels. Experimental systems which operate over a range of optical power levels can be designed to take advantage of this mode of operation. A further advantage is that these systems are less sensitive to fluctuations in laser power as well as variations in losses through the system. As the S-SEED also acts as a differential detector, communications links using S-SEEDs as both modulators and detectors can readily be implemented. These differential optical communication links are expected to have improved speed and power characteristics over conventional electrical tracks even for very short interconnection distances [50].

2.3.5 M-SEEDs

The concept of the S-SEED can be extended to include N mqw diodes reverse biased in series. The resulting Multistate or M-SEED [51] has the property that the diode illuminated by the weakest beam becomes the highly reflecting/transmitting one, on powering up the system. An electrically and optically enabled S-SEED or tri-state SEED is possible to implement by using an M-SEED (M = 3). If the beam incident on the enable diode, is larger than the two inputs to the other diodes, then the supply voltage V_{cc}, falls across the two other diodes which effectively make up an S-SEED. If the enable input signal however is smaller than the two other inputs, then the supply voltage is seen entirely across the enable diode and the S-SEED, made up from the other two diodes is effectively disabled, since there is no supply voltage seen across it [52].

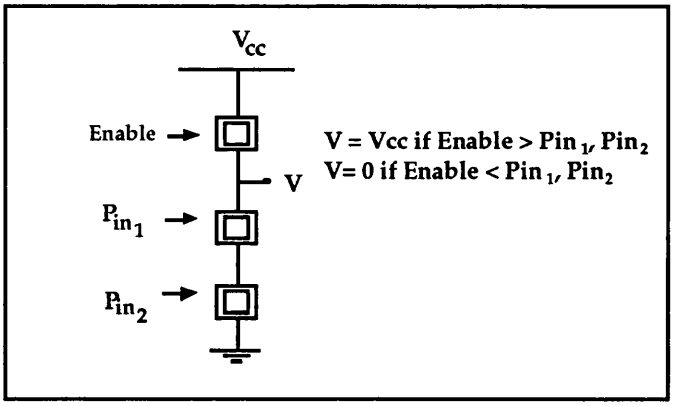

Figure 2.10c Tri-state S-SEED (M-SEED M=3)

2.3.6 SEED Oscillators

When a MQW modulator is electrically biased in series with an L-C circuit, oscillation at the resonant frequency of the L-C circuit, can occur when the SEED is optically pumped so as to produce in it a negative electrical resistance so as to overcome the losses in the rest of the circuit [30, 39]. The SEED capacitance, parasitic capacitance of the inductor and the SEED mount fixture, constitute C, and the oscillation frequency can be electrically or optically tuned through changes in the SEED's depletion layer capacitance. The oscillation is not only seen on the voltage across the MQW modulator but also in the power of the transmitted beam. The pump beam can be quite deeply modulated which could be used for the generation of an optical clock signal. The SEED oscillator can also be injection locked to a small signal, optically modulated beam and used in optical clock-recovery and data retiming applications [35]. The maximum oscillation frequency of the SEED oscillator depends very much on the value of the SEED's negative resistance, dI_p/dV or g_m. Large values of g_m facilitate SEED oscillation at higher frequencies where oscillation is readily damped by electrical losses in the rest of the circuit. (See 5.5 for a further discussion).

2.4 The Evolution of the SEED

The first SEED devices were anti-reflection coated, transmission devices with low contrast (≈2:1) for a 15 volt voltage swing [28-36]. A large intrinsic mqw region was required for significant changes in device absorption, leading to large operating voltages. The first attempts at integration to any degree, were 2 x 2 arrays of D-SEEDs in which the load photodiode was vertically integrated with the MQW modulator [31]. The next generation of SEEDs consisted of 2-pass reflection devices [37, 38]. A dielectric mirror on one side reflects the incident light and allows the double pass of light through the intrinsic region, thus the modulator requires less wells for the same amount of absorption. Also, less voltage is required for a given field across the narrower intrinsic region. The

front surfaces of the modulators were anti-reflection coated for the wavelength of operation so that all the incident light enters the device's intrinsic region. These devices have a finite contrast ratio, ie. non-zero reflectivity in the off-state and contrast ratios were typically 5:1 for a 15 volt supply [37]. Switching energies are low at about 1 - 2.5 pJ for supply voltages of 6 - 15 volts and 10 μm x 10 μm meas sizes [43]. Switching times of 33ps have been demonstrated for these SEEDs with some optimisation of their MQW structures for fast carrier sweep-out [42]. Also, 256 x 128 arrays of optically addressable S-SEEDs have been fabricated with a high degree of device uniformity and additionally, 8 x 16 arrays of electrically addressable S-SEEDs for use as differential modulators/ detectors have been demonstrated [44]. Six stages of arrays of 1024 S-SEEDs each, have also been connected in parallel, using free space optics, to form a photonic switching network demonstration [45].

By using the modulation enhancing characteristics of an asymmetric Fabry-Perot cavity [53] and [54], it will be shown that greatly improved contrast ratios for these SEED type devices can be achieved by allowing multi-passes of light through the absorbing region of these devices. Also, operation at much lower voltages is possible due to the fact that less absorption lengths are required and hence applied voltage, for a given change in device absorption.

2.5 The asymmetric Fabry-Perot SEED device

By aligning the unbiased, e1-hh1 exciton peak wavelength of a MQW intrinsic region with an asymmetric Fabry-Perot cavity resonance, the cavity reflection can be made very low by virtue of matching the top and effective bottom mirror reflectivities. This is achieved by having a suitable amount of absorption in the cavity such that $R_f=R_b e^{-\alpha d}$. The cavity is symmetric, ie. the light reflected from the device cavity is comparable to that reflected at the device's front surface. Upon increasing device bias, by way of the quantum confined Stark effect (QCSE) [17], the exciton red-shifts and decreases in strength. The absorption in the cavity falls, the cavity becomes asymmetric and cavity reflection increases. The front and back cavity mirrors are formed by the air/GaAs interface of the front surface of the device (R=0.3) and an integrated semiconductor multi-layer quarter wave reflector stack of R≥0.95, respectively (Figure 2.11). Where, R_1 is the front surface device reflection and R_2 is the reflection from the device cavity.

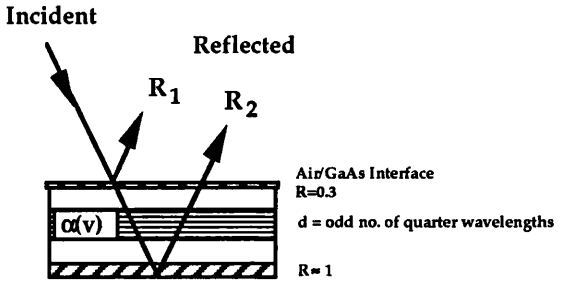

Figure 2.11 Asymmetric Fabry-Perot modulator structure

At low values of absorption α, $R_2 >> R_1$ and the net reflection from the device is high. At a value of absorption α_{crit} such that $R_f = R_b e^{-\alpha_{crit} d}$, $R_2 = R_1$ and R_2 is 180° out of phase with R_1, due to the return trip cavity length being set equal to an odd number of half wavelengths at the wavelength of SEED operation. Destructive interference of the reflected light beams takes place and cancellation reduces the reflected light from the cavity to zero. Therefore effectively infinite device contrast ratios may be obtained for an applied voltage swing.

Wide multiple quantum wells of 150Å GaAs (Barriers 60Å $Al_{0.3}Ga_{0.7}As$) are used because of the wider well's greater sensitivity to applied field. This gives a greater change in absorption $\Delta\alpha$, at the wavelength of operation, λ_{b-t}, for a given electric field [55]. Modelling shows the effect of the number of wells used, on the contrast ratio, insertion loss and operating voltages of these devices.

Number of wells	C_{max}(dB)	Insertion loss	Bias (V)
40	9.8	8.4	7.1
35	16.5	7.4	6.2
30	40	6.3	5.3
25	15.8	5.4	4.4
20	10.2	4.4	3.5
15	6.7	3.5	2.6
10	4.2	2.6	1.7
5	2.0	1.65	0.85

Table 2.1 *Modelled modulator characteristics (Whitehead [53])*

{C_{max}, the maximum contrast ratio is calculated as: $C_{max}(dB) = 10Log[R_{max}/R_{min}]$, where R_{max} and R_{min} are the maximum and minimum reflectivities from the device. Insertion Loss, corresponds to the minimum power loss to the system, by using the device, (Insertion loss = $10Log[1-R_{max}]$). These calculations make use of the standard Fabry-Perot type equations (see Appendix A) and the absorption changes with applied field for these type 150Å multiple quantum wells (see Appendix B). Values used for the front and back surface reflectivities were R_f=0.3 (air/GaAs interface) and R_b=0.95 (multilayer reflector stack) respectively.

It is seen that upon increasing the number of wells used, there is a trade-off between contrast and insertion loss. Contrast is a maximum with 30 wells (figure 2.12) and corresponds to the case when cavity absorption, at low field, is such that the front and effective back mirror reflectivities of the cavity are equal. Increasing the number of wells also increases the voltage required to apply a given field across the intrinsic (mqw) region. Low intrinsic doping is required in these structures so that all the wells in the intrinsic region see approximately the same electric field. If doping is high then

different wells would experience different fields, excitons would shift to a greater or lesser extent and an effective broadening (or diluting) of excitonic features summed over the whole of the device would be observed.

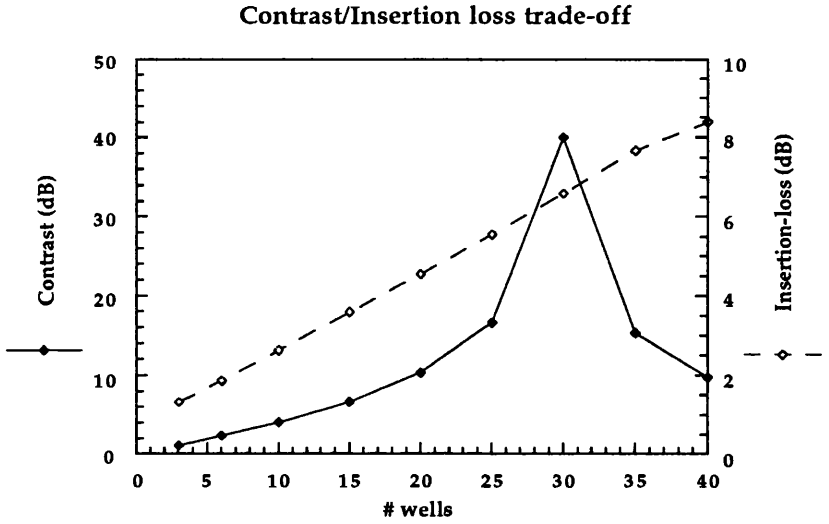

Figure 2.12 Theoretical reflection contrast ratio versus number of wells (Table 2.1)

2.5.1 Low operating voltage, 5:1 contrast, asymmetric Fabry-Perot SEED

The modelling shown in Table 2.1 shows that much improved contrasts for SEED switching at low operating voltages can be attained by using the modulation enhancing characteristics of the asymmetric Fabry-Perot cavity. The first Asymmetric Fabry-Perot SEED type structure to be grown was that of 15 x 150Å GaAs wells and 60Å $Al_{0.3}Ga_{0.7}As$ barriers (QT74 - [53]). The structure of this quantum well SEED/modulator was grown by MOVPE and is shown in figure 2.13 below.

The n+ type and intrinsic i MQW regions make-up the Fabry-Perot cavity and their total thickness is such that a resonance occurs at 862nm (the wavelength of the unbiased exciton, for 150Å wells). Total cavity length is an an odd multiple of quarter wavelengths in order to achieve cancellation and low cavity reflection. The mean weighted refractive index of the quantum well material used was $n_m \approx 3.37$. Ordinarily the multilayer reflector stack gives reflectivities ≥ 0.95 [27]. The upper layer of the stack is left undoped to guard against possible dopant diffusion into the multiple quantum wells. The GaAs capping layer is for electrical contacting purposes since it is much easier to form an ohmic contact to GaAs than to AlGaAs, in the absence of Aluminium oxides. The capping layer is thin enough so as to have negligible effect on the light passing through it. Due to non-uniformities during growth, the wafer was optically scanned at normal incidence, using an

optical multichannel analyser, in order to determine areas of correct reflection characteristics at 862nm. Simple mesa diodes (540 μm x 540 μm) with windowed top contacts (400μm x 400μm) were fabricated from selected areas using standard photolithographic, metallisation and wet chemical etching techniques.

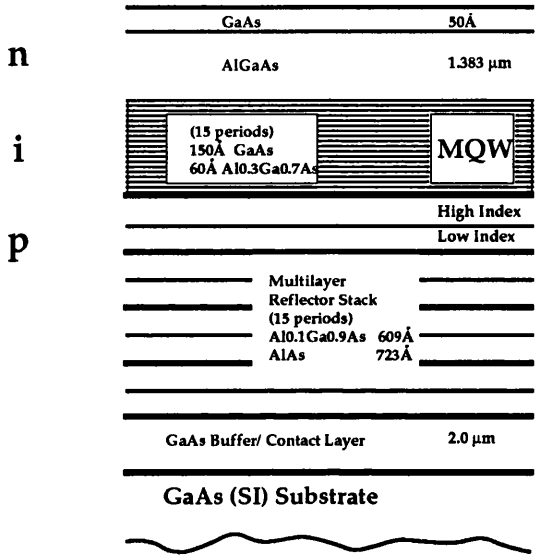

Figure 2.13 low voltage SEED structure (QT74)

These devices were characterised at low optical incident power using an automated halogen lamp monochromator system (approximately 100nW of power and 0.6nm linewidth). Reflection and photocurrent measurements were taken over a range of wavelengths. It was observed at 862 nm, that this device operated as a bias-reflecting or normally-off reflection modulator of Contrast 6.7 dB (4.7:1) with insertion loss of 3.2 dB for a voltage swing of 3.5 volts (0.9v forward bias to 2.6 volts reverse bias, figure 2.14). It was necessary to slightly forward bias the device in order to counteract the significant built in field of this relatively thin structure, in order to see a minimum reflection corresponding to maximum device absorption [53].

Keeping the device operating wavelength fixed at 862nm ($\lambda_{b\text{-}t}$) for constant optical power, and measuring photocurrent for varying bias voltages, it was also seen that this device exhibited negative resistance over effectively the same voltage swing as for the maximum change in device reflectivity (figure 2.15), therefore SEED operation, positive feedback, bistability and switching should prove possible.

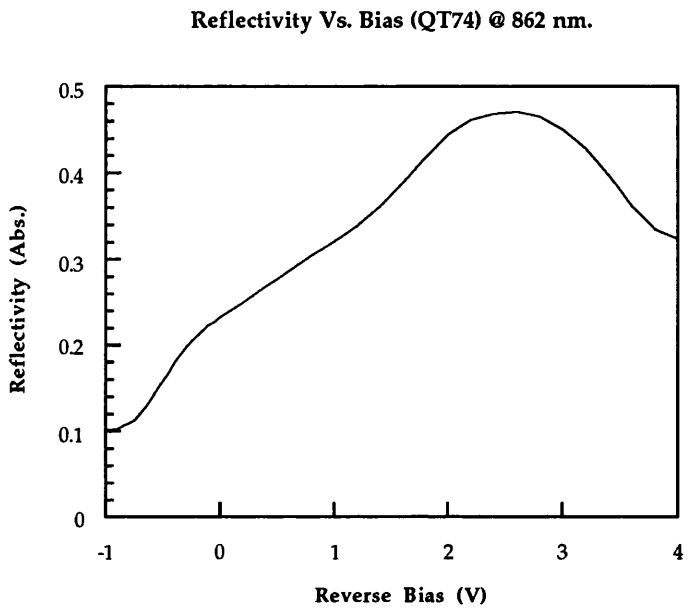

Figure 2.14 Reflectivity versus Reverse bias for SEED structure (QT74)

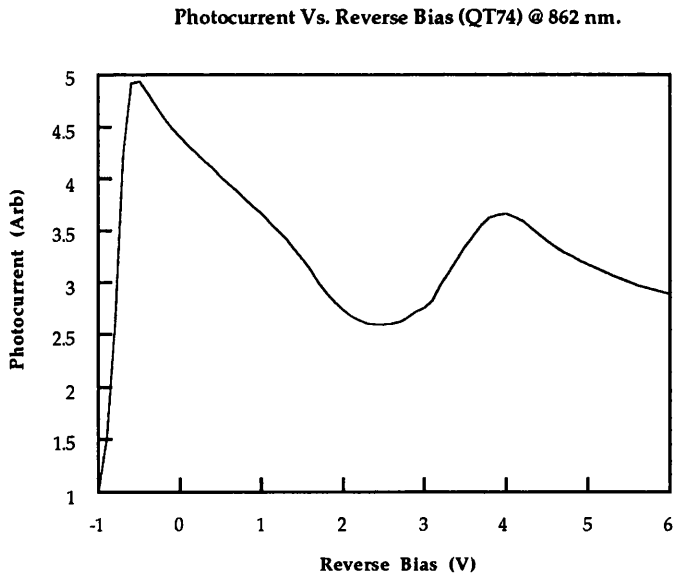

Figure 2.15 Photocurrent vs Reverse bias for SEED MQW modulator (QT74)

Note that increasing the reverse bias across the device, initially produces a rapid increase in device photocurrent. This is due to an electric field being set up within the

mqw intrinsic region which allows electron-hole pairs generated by incident photons to be swept across the depletion region and out into the external electrical circuit. When the field is such that a further increase in applied field does not give rise to any further increase in photocurrent (at a given optical incident power) then we say that the device quantum efficiency η, has reached its maximum value $\eta \approx 1$, (in this case at approx 0.5 volts forward bias). Quantum efficiency, η is the ratio of photons absorbed by the device to electrons released to the external circuit. With increasing bias, photocurrent decreases (negative resistance) due to the e1-hh1 exciton decreasing in strength and moving away from the wavelength of operation. After this region, the photocurrent successively rises and falls with voltage. This rise is due to previously forbidden energy transitions now entering the operating wavelength at high electric field. It should be noted how device reflectivity inversely follows the device photocurrent/ absorption characteristic.

In one respect SEED devices made using wide wells are slightly different to narrower well reflection SEEDs, in that with the narrower well versions, absorption continues to fall up until very high fields, whereas for wider wells, where the exciton characteristics are very close together, ie. the heavy hole and light hole can be indistinguishable and forbidden transitions shift much more quickly with field. A definite minimum absorption at a relatively low field is achieved for wider wells before forbidden transitions enter the operating wavelength, causing a subsequent rise in device absorption and photocurrent. Optimum V_{cc} corresponds to lower fields for the wider wells used in this structure, rather than the narrower wells used in previous devices. At higher fields, forbidden transitions increase device absorption above this minimum. The size of the electric field required is significant when it comes to optimising the switching speeds of these devices. Lower electric fields give rise to lower switching energies giving faster switching speeds (5.2).

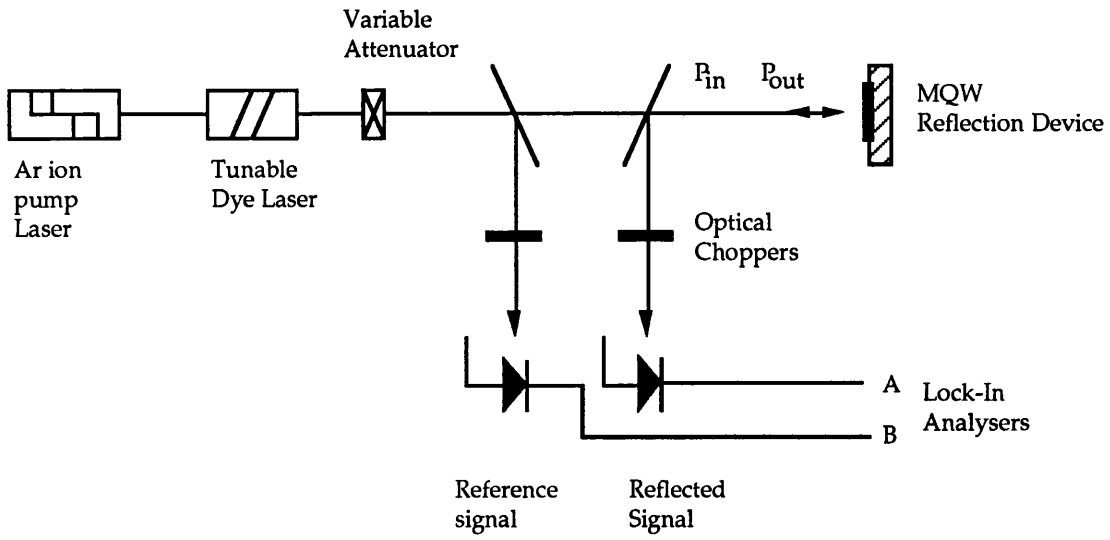

Figure 2.16 Dye laser experimental set-up

Using an argon ion pumped tunable styrylene-9 dye laser set-up (figure 2.16) and the MQW diode in the R-SEED configuration (figure 2.17), bistability and R-SEED type switching behaviour were observed with this device structure (figure 2.18).

The MQW modulator was reverse biased with a voltage V_{cc}, in series with a resistive load, R. Optical power incident on the device (P_{in}), was ramped up and down and the reflected power off the device (P_{out}) was measured.

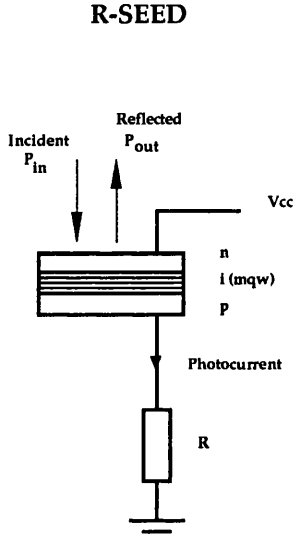

Figure 2.17 R-SEED schematic diagram

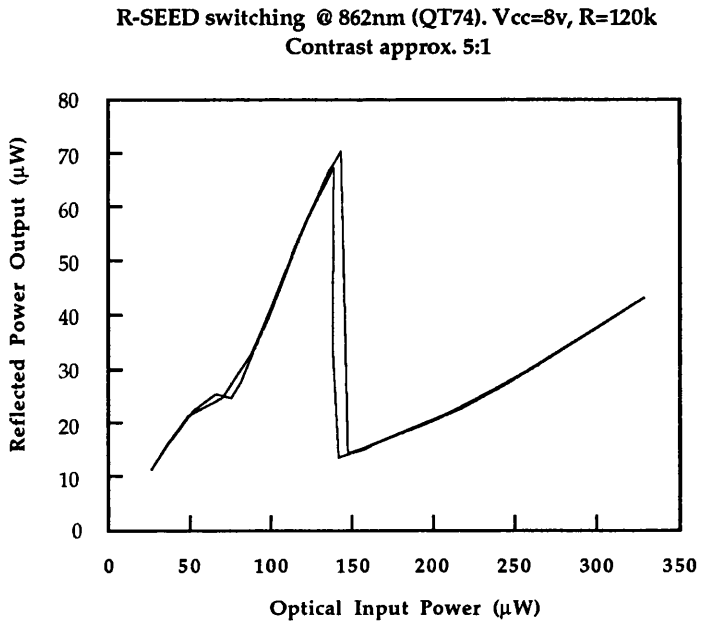

Figure 2.18 R-SEED optical bistability and switching

In figure 2.18 above, it can be seen that upon increasing optical power, the device switches and changes states at a certain critical power. Switching contrast ratio is approximately 5:1 for a supply voltage V_{cc}=8v @ 862nm. The initial kink in the curve at low power, high voltage across device, is due to the forbidden energy transitions entering the operating wavelength creating a separate region of negative resistance. At higher voltages and powers this can develop into its own separate bistable region.

The amount of power required to switch the device (P_{crit}) is dependent on the supply voltage V_{cc} and the magnitude of the feedback resistor, R. Higher V_{cc} necessitates a larger photocurrent and hence optical power, in order to give a sufficient drop across the resistive load so that the device enters its region of negative resistance and its bistable region of operation. Increasing the resistive load gives a larger voltage drop across the load for a given current and therefore less optical power is required for the device to enter its region of negative resistance. For example, increasing the value of the load resistor by a factor of 10, reduces the optical power required for switching by a factor of 10. Increasing V_{cc}, increases the width of the bistable switching region (figure 2.19). This effect is due to the resistive load-line intersecting the MQW device load-line more obliquely and subsequently a greater change in the R-SEED's input power is necessary for the device to switch its operating point from one side of the region of negative resistance to the other. The bistable region is consequently widened.

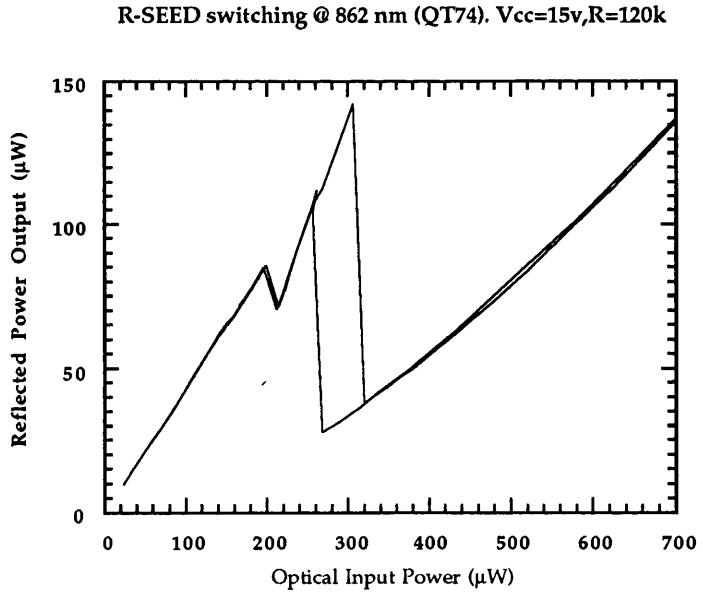

Figure 2.19 R-SEED optical bistability and switching

Increasing the width of the hysteretic region is desirable in systems applications where one needs a degree of noise immunity. A very narrow bistable region is relatively sensitive to signal noise and a small fluctuation in optical power could cause the device to erroneously change state. Large hysteretic width is therefore desirable and in fact is readily achieved when these SEED devices are operated in a Symmetric or S-SEED configuration (figure 2.10). There is an optimum R-SEED bias voltage V_{cc}=8v for maximum contrast switching (figure 2.20), R=120kΩ. This corresponds to the diode switching between values of its maximum and minimum absorption/reflectivity and vice-versa. The minimum value of V_{cc} required for R-SEED operation is proportional to the fall off in device responsivity with applied reverse bias (or negative resistance) and is discussed further in chapter 5. The effect of the actual magnitude of the negative resistance of a MQW modulator with respect to a number of systems applications using SEEDs, is also discussed.

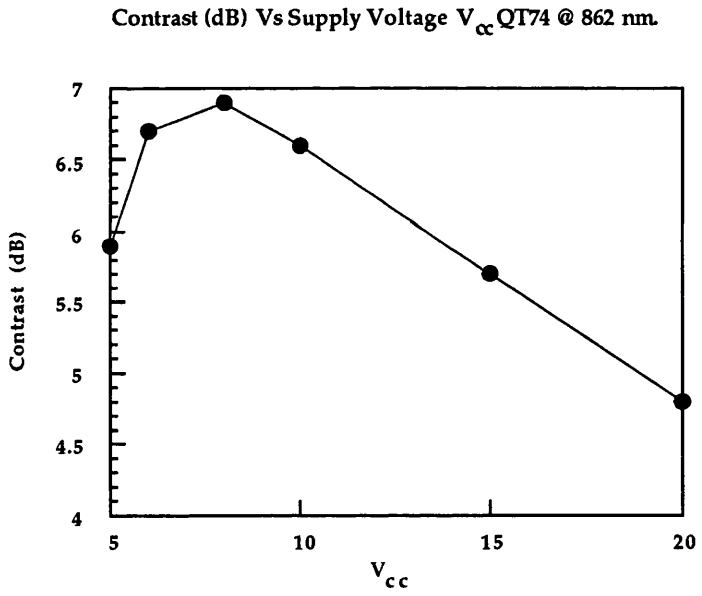

Figure 2.20 Switching contrast ratio for varying supply voltages V_{cc}

Negative device resistance and bistability were observed over a range of wavelengths. Clearly 862nm (λ_{b-t}) is the optimum wavelength of operation giving the maximum change in absorption and hence reflection, on switching. Either side of 862nm, switching contrast decreases (Figure 2.21).

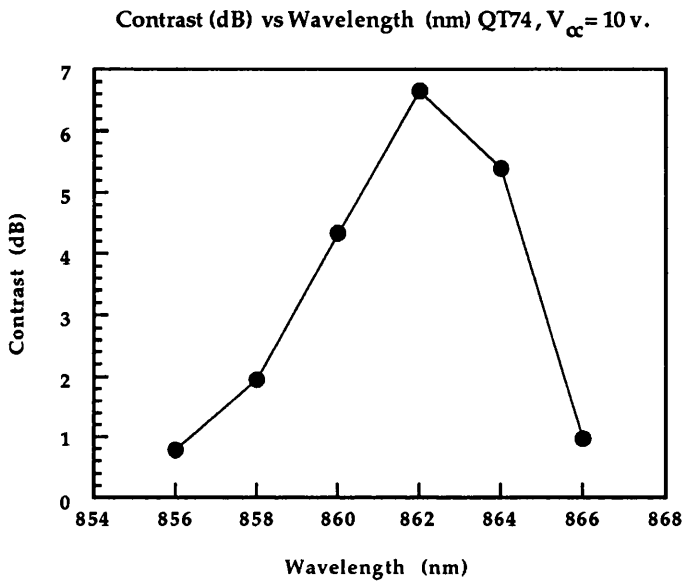

Figure 2.21 Switching contrast ratio for different wavelengths

2.5.2 The very high contrast asymmetric Fabry-Perot SEED.

The next MQW SEED structure grown was the 30 well sample of Table 2.1, QT104 (figure 2.22). The 30 well structure at zero field was designed so that the front and effective back mirror reflectivities were matched, thus giving zero reflected light at low field. Upon applying a reverse bias, absorption in the cavity falls, the cavity becomes asymmetric and reflectivity increases. The effective contrast ratio of this device is designed to be very high since reflectivity in the absorbing state is very close to zero. Due to non-uniformity during wafer growth, only a very small piece of the wafer exhibited the correct cavity length for designed operation. Unfortunately, because of a processing error this piece of usable material was rendered useless and another wafer growth was requested.

A regrowth of QT104 was requested and with QT154 a more sizable piece of wafer was deemed usable by scanning using an optical multichannel analyser, taking into account the effect of the built in field on the unbiased wafer reflectivity. Standard mesa diodes (as with QT74) with optical window size (400μm x 400μm) were fabricated from this material and then characterised. Measuring photocurrent and reflection against reverse bias @ 862nm for low constant optical power using the monochromator set-up showed all the characteristics expected and desired of the SEED device - ie. negative device resistance (figure 2.23) and very high contrast (figures 2.24 and 2.25), for the expected voltage swing of approximately 5 volts.

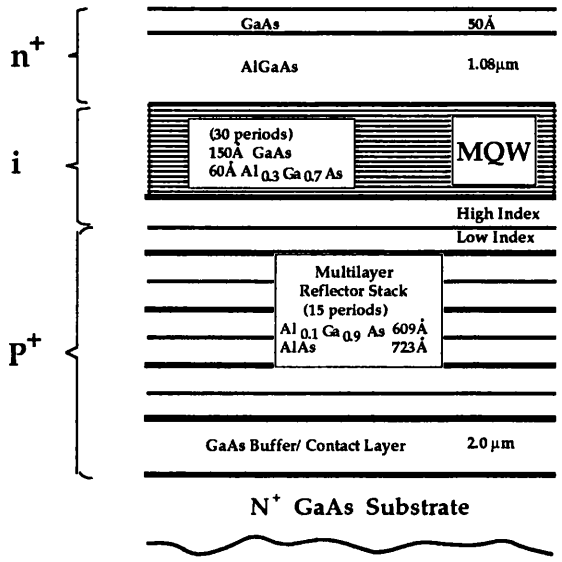

Figure 2.22 QT104/154/225 High-Contrast SEED

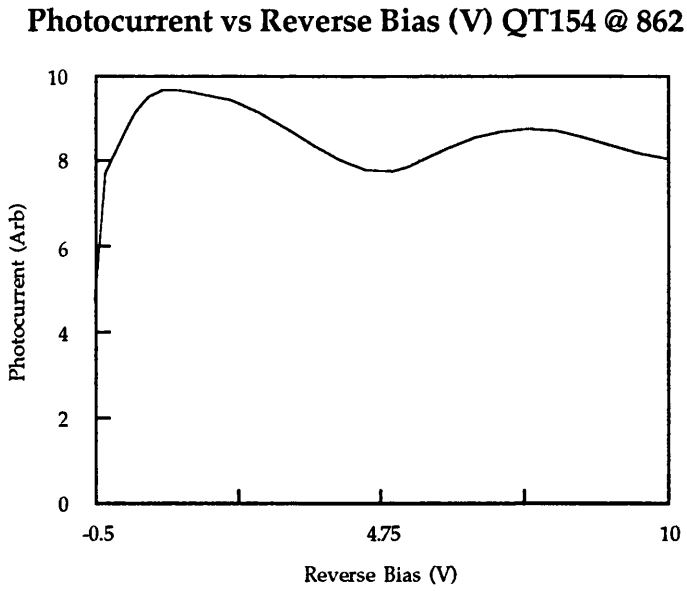

Figure 2.23 Photocurrent versus Reverse bias voltage showing negative resistance for the high contrast SEED (QT225)

Due to the lower maximum reflection, ie. higher insertion loss >6dB of this structure, the 'DC' or minimum absorption is much higher than for the previous device (QT74). 70% as opposed to approximately 44%, therefore a relatively smaller change in

absorption/photocurrent with bias takes place for a given optical power. A smaller change in photocurrent implies a narrower bistable hysteresis width since a smaller difference in S-SEED input powers is required for switching from one state to the other. With maximum absorption (100%) and minimum absorption quite high, responsivity (A/W) is high. More photocurrent is generated for a given optical power, therefore faster switching should be possible (See S-SEED speed considerations, 5.2).

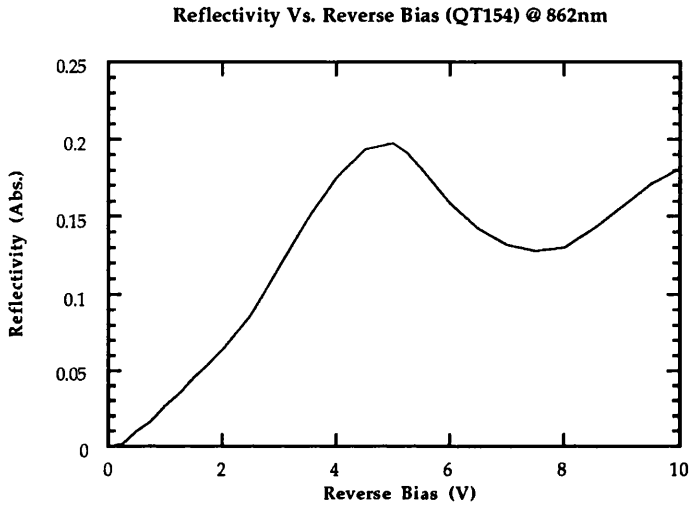

Figure 2.24 Reflectivity versus Reverse bias for high contrast SEED

The maximum change in reflectivity occurs for a voltage swing of 0 to 5 volts. Insertion loss is quite high at 7dB, due to a slightly non-optimum cavity length, due to variations in the material thickness caused by wafer growth non-uniformities.

This device exhibited very high maximum contrast (>100:1), within the noise limits of the monochromator measurement system, and a contrast of more than 10dB for a linewidth of over 3 nm, for a voltage swing of 0 to 5 volts. The advantages of high contrast are many: lower crosstalk, ease in cascading logic devices, fanout etc. [47]. However, when these devices were tested for SEED switching at higher powers, using the dye laser set-up, it was found that they behaved very differently from that expected and already observed at low power. It was observed that for optical powers of order 1μW, no excitonic changes in device absorption took place with bias, thus no region of negative resistance was observed. Increasing the electric field simply gave increasing photocurrent, yielding negative, rather than positive feedback and therefore no SEED switching or bistability was possible. Operating the device at lower wavelengths, away from all excitonic features showed decreasing device quantum efficiency for increasing optical power. For higher incident powers, a larger and larger applied voltage was required to generate sufficient field to sweep electron-hole pairs out of the intrinsic region. The device exhibited a variable collection efficiency.

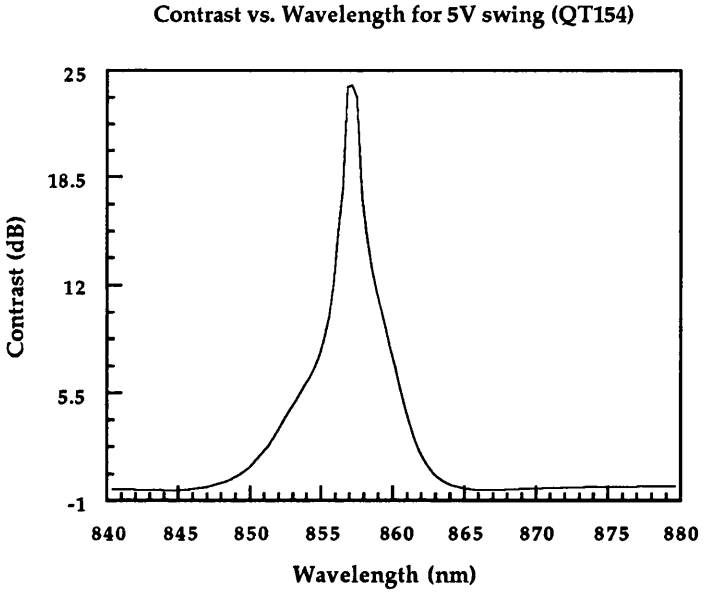

Figure 2.25 Reflection contrast ratio versus wavelength for high contrast SEED for a 5 volt voltage swing

Figure 2.26(a) below shows an ideal PIN diode photocurrent versus voltage characteristic for increasing incident optical powers. Ideally collection efficiency should be high and the I-V response flat, even into small forward bias voltages.

Figure 2.26(b) shows a schematic diagram of the observed I-V characteristic for these devices. Upon increasing the incident optical power ($P_3>P_2>P_1$) on the device, more and more bias voltage ($V_1>V_2>V_3$) was required in order to sweep photon generated electron-hole pairs out of the device intrinsic region (fig. 2.21(b). Increasing device bias simply gave increased photocurrent due to increased quantum collection efficiency. This effect was apparently greater than any electric field induced changes in device absorption. Therefore the expected excitonic features ie. negative device resistance etc., were effectively 'invisible' to the external electrical feedback circuit and therefore no positive feedback or switching was possible.

(Excitonic features and field induced changes in device absorption could only be observed at extremely low levels of optical power (~nW's) on a monochromator set-up, figures 2.23, 2.24 and 2.25).

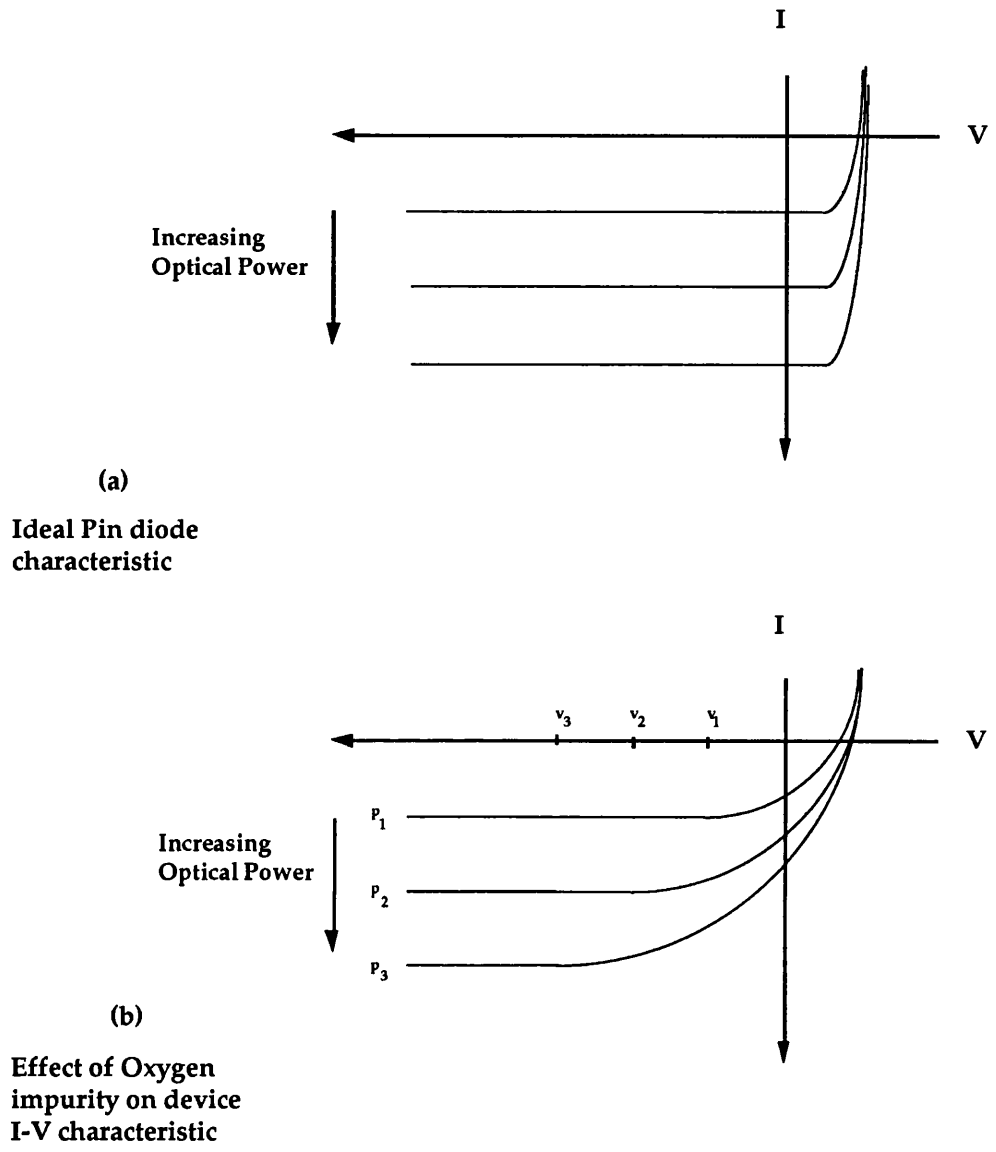

Figure 2.26 Schematic diagram showing ideal and observed pin diode characteristics

Initially, it was thought that this problem could be due to a very high contact resistance in series with the device so that the MQWs were not experiencing the full applied electric field changes, due to a large voltage drop across the device contacts. However contact resistance was measured and found to be too low (<1kΩ) to have any significant effect (for the levels of photocurrent involved). It transpired, however, that the reason the exciton becomes so readily bleached was an O_2 contamination in the Aluminium source during wafer growth. The Oxygen acts as a trap and reduces the strength of the exciton. For increasing optical powers, the intrinsic region effectively

becomes less intrinsic and its resistance increases. The exciton becomes saturated even at relatively low powers and at powers above nW's is almost invisible to applied Electric field changes. Photoluminescence measurements showed very weak exciton luminescence.

Aluminium source contamination in the material growth process having been traced to TMA (Tri-Methyl Aluminium), the source of Aluminium in the MOVPE growth process, with high Oxygen impurities, a third wafer regrowth was requested of the 30 well SEED structure. The Aluminium source was replaced and photoluminescence measurements on the regrowth material QT225, showed much stronger and improved exciton strength. The wafer was analysed using an optical multichannel analyser and standard mesa diodes were fabricated from selected areas. Devices were characterised at low power using the monochromator set-up and then at higher powers using a tunable Ti:Sapphire laser source. Negative device resistance was observed for a range of wavelengths for a reverse voltage swing from approximately 0.5 to 5 volts (figure 2.27).

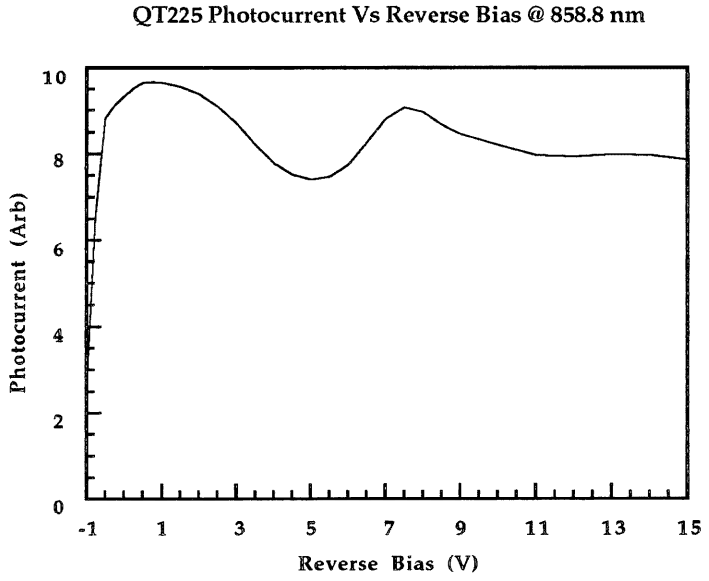

Figure 2.27 Photocurrent versus Reverse Bias voltage for high contrast SEED

High contrast switching and bistable hysteresis were observed for devices in an R-SEED configuration @ 858.8 nm, R=1.5MΩ (Figure 2.28). A contrast ratio of >100:1 was observed for an insertion loss of 6.6dB (R_{max}=22%). Increasing R-SEED bias voltage increases the power at which switching occurs (figure 2.29) as expected.

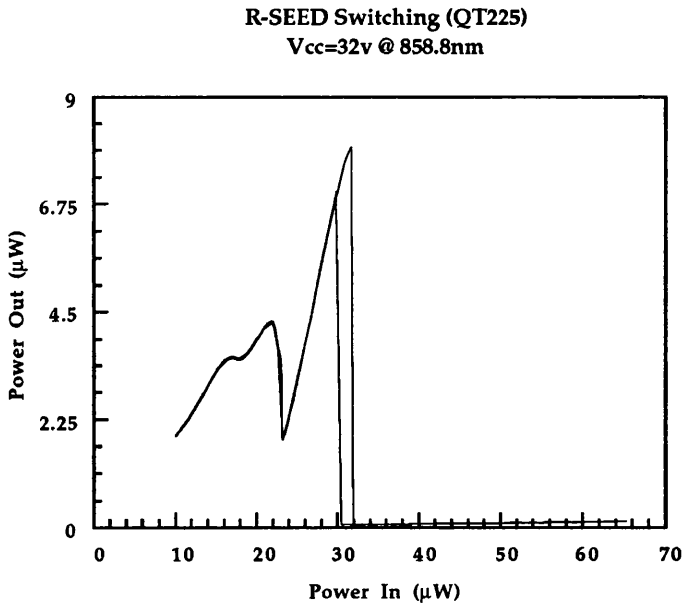

Figure 2.28 Very high contrast R-SEED switching (QT225)

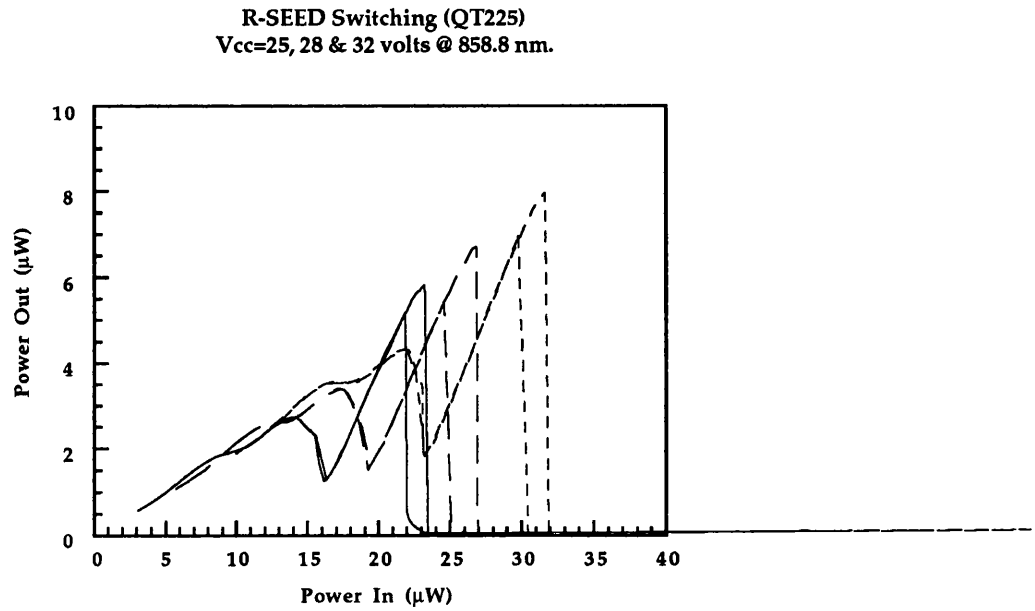

Figure 2.29 Very high contrast R-SEED switching for three different operating voltages

2.6 The high contrast S-SEED

Two high contrast asymmetric Fabry-Perot MQW modulators were connected in a discrete S-SEED configuration as is shown in figure 2.30 below.

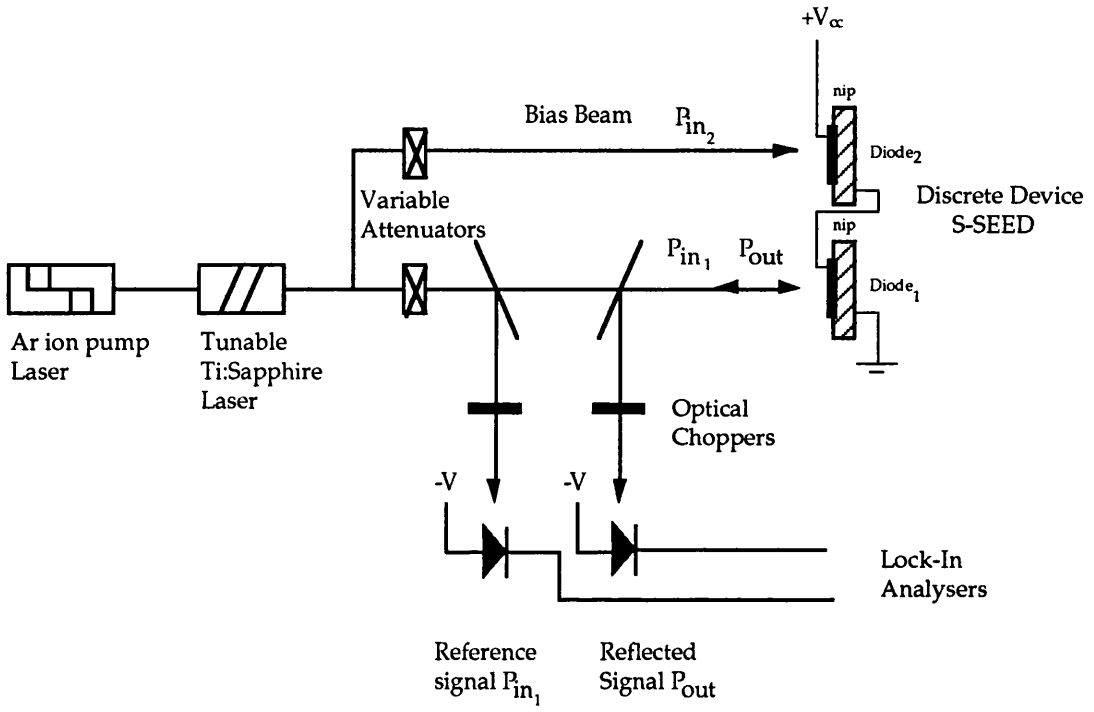

Figure 2.30 S-SEED Experimental Set-Up

For a supply voltage, V_{cc}=4.2V, a constant bias beam P_{in_2} was applied to $diode_2$. Optical power P_{in_1}, incident on $diode_1$ was ramped up and down and the reflected optical output power P_{out_2} was measured

Optical bistability and hysteresis was observed in the ratio of the two input beams [56]. High contrast switching (> 60:1) was observed for a range of bias beam powers: figures 2.31, 2.32 and 2.33. Increasing the constant bias power (P_{in_2}) increases the input optical power (P_{in_1}) at which switching occurs and also increases the width of the hysteretic curve. The width of the bistable loop is proportional to the absolute change in device photocurrent for the switching voltage swing. Chapter 4 discusses in detail, the effect of the device's absorption characteristics on the S-SEED hysteresis curve. For higher optical powers, the difference in magnitude of the two photocurrents to induce switching is greater, therefore the optical power hysteresis curve is wider at higher optical powers.

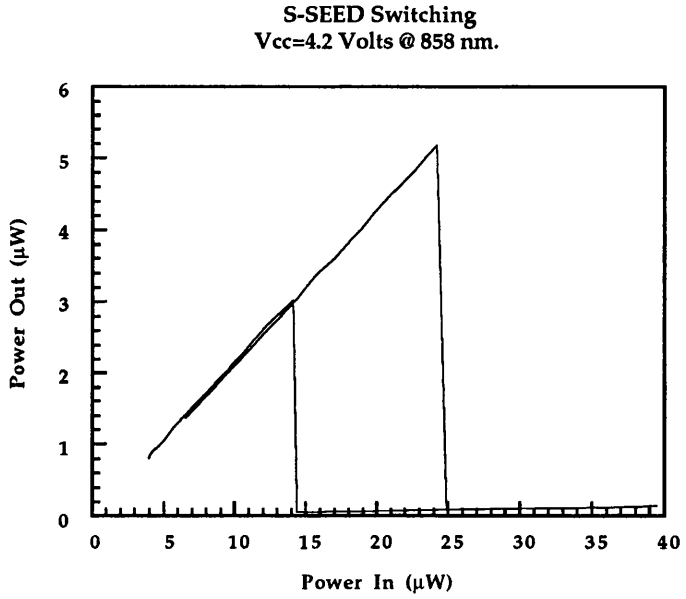

Figure 2.31 Very high contrast S-SEED switching hysteresis at low power

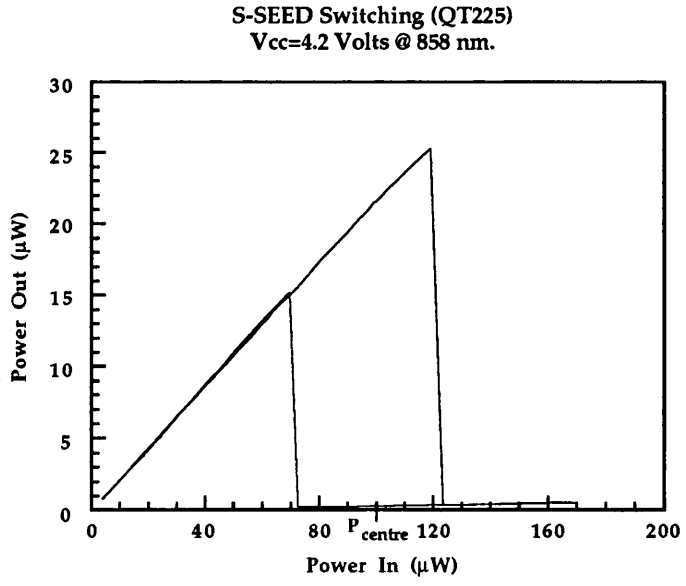

Figure 2.32 Very high contrast S-SEED switching hysteresis at a higher power

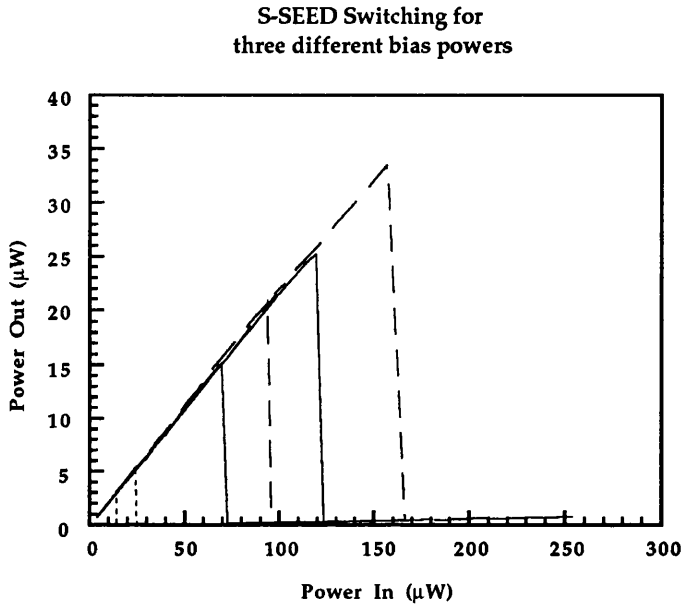

Figure 2.33 Very high contrast S-SEED switching for three different bias beam powers

2.7 Conclusions

It has been shown in this chapter that the use of the asymmetric Fabry-Perot type modulator structure and its optimisation for use as a SEED gives a much improved SEED device that has a very high switching contrast ratio for low operating voltages, at the expense of a very small increase in fabrication complexity. These higher contrast SEEDs may be used in systems applications requiring a high degree of contrast between signal channels. Due to operating the S-SEED at the e1-hh1 exciton peak, insertion loss can be quite large due to the high background absorption at this wavelength. These devices may be improved however, by using techniques which apply to normally-on or bias-absorbing modulators [57]. By increasing the front surface reflectivity of the Fabry-Perot cavity, devices with smaller absorbing regions operating at lower voltages can be obtained [58]. Increasing the front surface reflection of these devices entails the growth of a mirror on the front surface. This adds considerably to the tolerance in material growth parameters which is allowed. A front surface reflectivity of $R_f = 0.3$ is much easier to achieve since it is formed by the air/GaAs interface. High contrast modulation (20dB) has been obtained without the use of a resonant cavity in the GaAs/AlGaAs system [59]. This requires however very long absorbing regions requiring very high operating voltages (30 volts) and very low intrinsic doping. Other work has also been carried out which applies Fabry-Perot techniques to superlattice electroabsorption modulator structures [60, 61]. These structures exhibit Wannier-Stark localisation which gives rise to a 'blue shift' in the band edge absorption upon application of an electric field.

There now exists a very significant body of knowledge in this field and devices with very finely tuned characteristics can be fabricated. Post-growth techniques such as impurity free vacancy diffusion (IFVD) [62] can be used to precisely 'engineer' the band-gap of these mqw structures. By the selective application of anti-reflection coating to Fabry-Perot modulators after fabrication it is possible to integrate both bias-absorbing and bias-reflecting (normally-on and normally-off) modulators on the same integrated circuit [63]. This can be used to give increased logical functionality for use in optical processing systems. The following chapters address some of the design issues of using SEEDs in actual systems applications and how these devices, which can be made with widely varying operating characteristics, can be optimised and used to maximum effect.

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CHAPTER 3

The SEED optical tap / High-contrast self-linearised modulator

Linear optical modulators are modulators whose optical output signal is in some way linearly proportional to a control input signal. This class of modulator can be useful in low-noise subcarrier multiplex systems [1] and also for example in electro-optical neural networks [2], where the device transmission is required to correspond linearly to the magnitude of some input or 'weighting' factor. For the case of linear amplitude modulation of an optical signal, ideal linear modulator characteristics are similar to ordinary electroabsorption modulators and include high contrast ratios, large reflection changes and low operating voltages. For these types of application, the modulation enhancement obtained through the use of an asymmetric Fabry-Perot (AFP) type multiple quantum well (MQW) reflection modulator can be used to advantage. This chapter describes such device utilisation and then goes on to describe device optimisation issues and systems applications for this type of device functionality.

Being able to extract a small part of, or 'tapping' an optical signal without destroying the entire signal is a very desirable system feature for use in communications network architectures. The D-fibre backplane of BTRL [3] uses this principle for interconnecting electronic circuit cards to a shared backplane bus, within a computer rack system. Connecting integrated circuits over even shorter distances is also advantageous. Reference [4] describes an optical rail-tap system used for interconnecting integrated circuits on the same printed circuit board. In this chapter SEED operation for this type of systems application is also discussed.

3.1 Theory of operation

As discussed earlier in (2.2), if the feedback in a SEED [5-9] system is positive, bistability or oscillation is possible. If the feedback is negative, then the SEED exhibits a different behaviour. The negative feedback acts to stabilise the system and self-linearised modulation or optical level shifting is obtained [5]. Operating a MQW modulator/detector at a wavelength giving increased photocurrent (responsivity) for increasing applied bias (ie. bias-absorbing, $\lambda_{b\text{-}a}$, 2.1.2), establishes a negative feedback which acts to stabilise the system, provided the series electronic circuit has positive slope resistance [5, 6]. If the MQW diode is biased by a constant current I_c, then in the equilibrium state, photocurrent through the diode, I_p, equals the current sourced by the external electrical circuit (Kirchoff's current law), figure 3.1. For a device with unity quantum efficiency η, (ie. for every photon absorbed, one electron is collected at the device terminals, η=1), the optical power absorbed, P_{abs} is the Absorption, A multiplied by the Incident optical Power, P_{in}: $P_{abs} = AP_{in}$. Absorbed power is converted into photocurrent with responsivity $\frac{e\lambda}{hc}$ (A/W):

$$I_p = \frac{e\lambda}{hc} P_{abs} = \frac{e\lambda}{hc} A P_{in}$$

For circuit equilibrium, the absorbed optical power is directly proportional to the external current flowing through the circuit. If the circuit bias current is varied, device absorption varies proportionally in order to equalise I_p and I_c. I_c acts to charge up the characteristic device capacitance of the MQW modulator, whilst I_p acts to discharge it. When they are imbalanced, for example when $I_c > I_p$, current flowing into the MQW device exceeds the current leaving the device. The voltage across the device therefore increases, causing increased device absorption/photocurrent, (due to device operation with negative feedback), and equalises I_c and I_p. When $I_c < I_p$, the voltage across the device decreases, causing decreasing device absorption, again equalising I_c and I_p. The Absorption, A is given by $\left(\frac{hc}{e\lambda}\right)$ times the Responsivity, (I_p/P_{in} [AW^{-1}]). If the external biasing current is varied linearly, then these devices can be used as linear modulators, with the magnitude of the absorbed (and hence reflected) optical power directly proportional to the magnitude of the constant current supply bias. Conversely, if the supply current is held fixed and the optical power incident on the device is changed, then a constant optical power, which is proportional to the magnitude of the biasing current, is subtracted from the incident optical signal: 'optical level shifting' or 'tapping'. Hence we have the result that by biasing a MQW PIN Detector with a (mean) current corresponding to a desired photocurrent signal level, the device self-adjusts its absorption to produce just that signal, leaving the remaining incident optical signal power to be reflected.

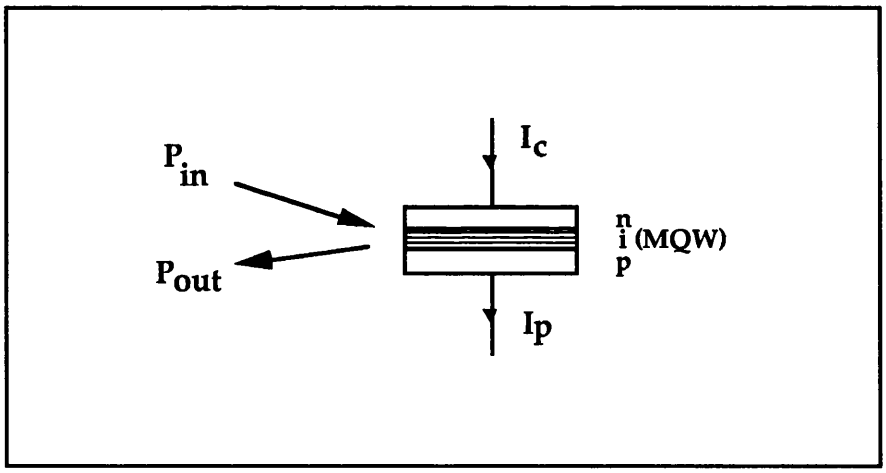

Figure 3.1 Self-linearised modulator schematic

3.2 The asymmetric Fabry-Perot SEED optical 'tap'

The performance of the SEED with negative feedback, ie. the self-linearised

modulator, can be dramatically improved by using the modulation enhancing characteristics of an asymmetric Fabry-Perot cavity [10], yielding a device configuration with very useful operating characteristics. Additionally, due to very high values of device absorption, very high responsivity (A/W) is obtainable. This device therefore also acts as a very efficient photodetector. The following sections describe the application of this type of device structure for use as a linear modulator or an optical 'tap' with substantially improved performance over conventional designs.

3.2.1 Device design used

The device used in this experiment is a p-i(intrinsic)-n, high contrast, asymmetric Fabry-Perot, GaAs/AlGaAs, multiple quantum well reflection modulator [10]. The intrinsic region consists of 75 x (95Å GaAs well and 60Å $Al_{0.3}Ga_{0.7}As$ barriers) contained by a cavity formed by an integrated dielectric back reflector stack (R≥0.95) and a front surface Air/GaAs interface (R=0.3). Device operation is the same as that explained in (2.5) and is such that the high contrast modulation of light at 860nm can be achieved by shifting the excitonic absorption into and out of a resonant cavity upon application of an electric field, by way of the quantum confined Stark effect [11]. Operating the device at a wavelength greater than the band-edge of the material, when an electric field is applied perpendicular to the multiple quantum wells, the band-edge and exciton red-shift, therefore increasing absorption at this point (λ_{b-a}). The device therefore exhibits increasing device absorption with increasing device bias (the condition for negative feedback). Reflectivity falls to very near to zero (figure 3.2) as absorption approaches 100%, for about 9 volts reverse bias, giving a responsivity very close to the theoretical maximum, $\frac{e\lambda}{hc}$ = 0.69 A/W at 860nm (figure 3.3).

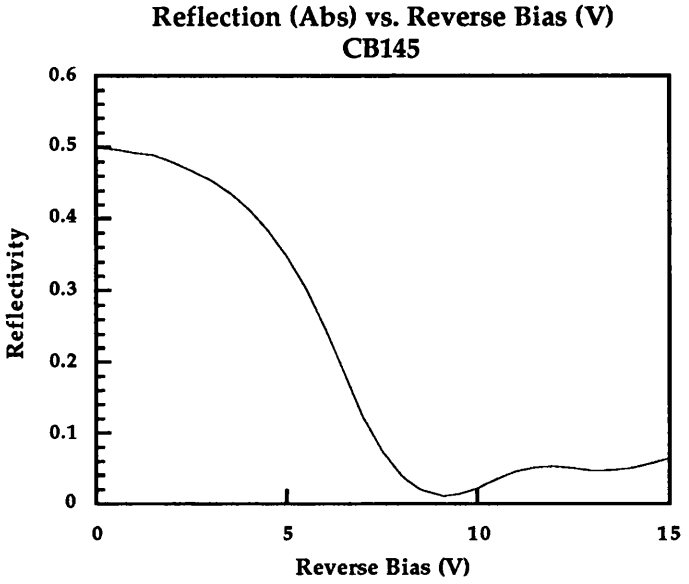

Figure 3.2 Reflection versus voltage characteristic of the MQW modulator used.

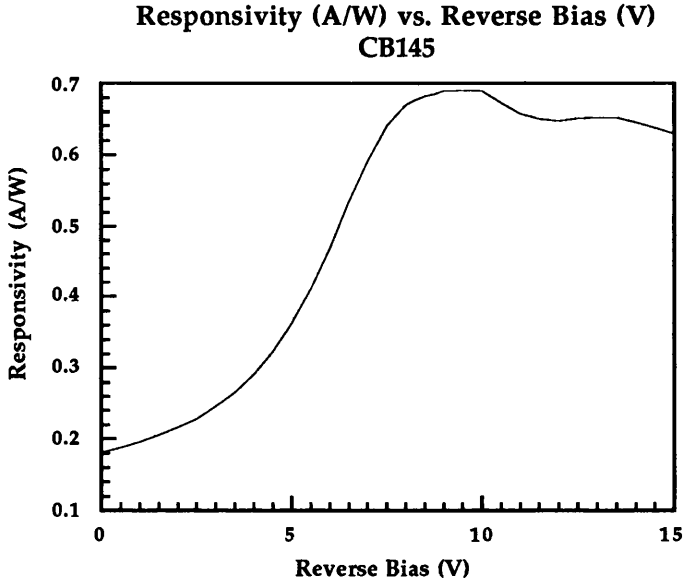

Figure 3.3 Responsivity versus voltage characteristic of the MQW modulator used

3.2.2 Experimental set-up and procedure

The MQW modulator PIN diode was placed electrically in series with a simple operational amplifier as a constant current source (shown in figure 3.4). The constant current supply sources a fixed current, $I_c=V_{z_1}/R_1$. At low levels of device photocurrent (ie. low incident optical power), I_c charges up the device capacitance since the net flow of charge into the diode is positive. The zener diode, Z_2 protects the pin diode modulator from going too far into reverse bias and breaking down at high voltages. This zener diode, also limits the maximum possible voltage across the MQW modulator to V_{z_2} ($\approx$ 9 volts), corresponding to the voltage of maximum device responsivity. Therefore at low optical powers, the device is anchored to its most responsive operating point and any incident optical power will be converted to photocurrent with maximum conversion efficiency. If the voltage across the device becomes greater than V_{z_2}, the zener diode conducts the constant bias current, I_c away to ground, thereby fixing the device voltage to V_{z_2}. A chopped optical signal of 860nm, obtained from an Argon ion laser pumped, tunable Ti:Sapphire laser was focussed onto the MQW detector. For various constant current values I_c, the optical beam (of power P_{in}), incident on the MQW modulator, was ramped and, using lock-in amplifiers, the reflected optical output power P_{out}, and the photocurrent I_p, were measured (figures 3.5 and 3.6). A parallel coupling capacitor, C_c was also used, to ensure a fast enough speed response to the system in reaction to using a chopped optical signal beam of a few kHz.

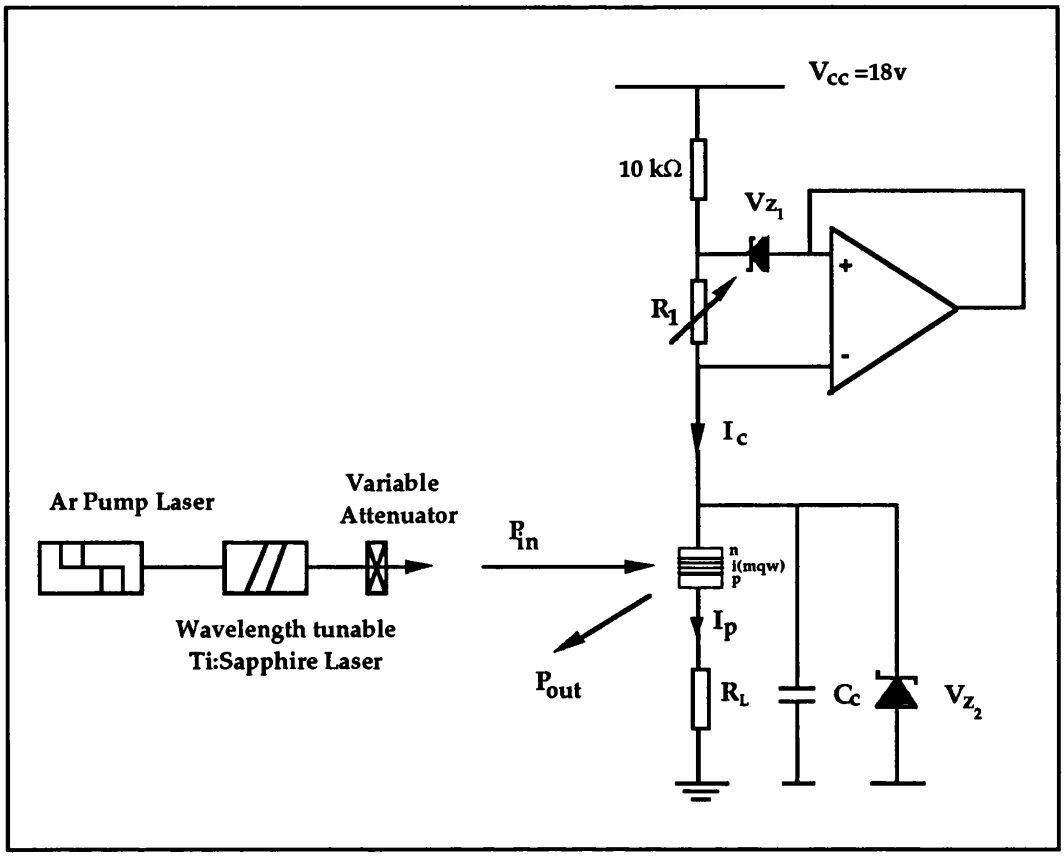

Figure 3.4 Experimental set-up showing the constant current biasing of the SEED

3.2.3 Results

With low optical power incident on the MQW diode, $I_c > I_p$, the modulator charges up to the breakdown voltage of the parallel zener diode, V_{z_2} corresponding to the voltage (9 volts) at which the device operates at 100% absorption, A_{max}. At this voltage, photons incident on the device are converted to electrons with very near to maximum conversion efficiency, $I_p = P_{in}\frac{e\lambda}{hc}$ and very little of the light incident is reflected from the modulator ($P_{out} \approx 0$). The slope of the photocurrent-input power characteristic for this range of operating powers is therefore the same as the responsivity, $A\frac{e\lambda}{hc} \approx 0.69$ A/W (where A=1). At an input power P_1, sufficient light is absorbed within the device to generate photocurrent equal to the constant source current I_c, $I_c = I_p$. P_1 corresponds to the power, $P_1 = P_{abs} = \frac{hc}{e\lambda} I_c$ (for $I_p = I_c$). As the incident optical power P_{in} is further increased, I_p becomes greater than I_c, the voltage across the MQW device reduces as does device absorption (negative feedback) in order to maintain circuit stability and $I_c = I_p$ (figures 3.5 and 3.6a).

As P_{in} increases to powers greater than P_1, device absorption decreases with P_{in}^{-1} in order to keep $P_{abs}=P_1$ constant and $I_p=I_c$, (figure 3.5). I_p can be seen to increase slightly with power, due to the constant current I_c being non ideal and its output current being slightly dependent on its load voltage. With increasing optical input power, the voltage across the diode drops, cavity absorption decreases and cavity reflection increases. Therefore for increasing optical power, a decreasing fraction of the incident light is required to be absorbed so as to satisfy $I_p=I_c$. Therefore for increasing optical power, an increasing fraction of the incident optical power is reflected. As P_{abs} and I_p remain constant beyond a certain critical input power P_1 (at which $I_p=I_c$), any further light incident is reflected. As the voltage across the diode reduces and tends towards 0 volts and minimum absorption, any further decrease in device responsivity is achieved by a decrease in internal device quantum efficiency, photons are lost to recombination and at higher powers the device does in fact forward bias. For an input power P_2, the voltage across the modulator drops to 0 volts and the device operates at the point of its minimum absorption, A_{min} (and maximum reflectivity of 50%). The P_{out}/P_{in} slope then becomes equal to the maximum device reflectivity, R_{max} (figure 3.6b).

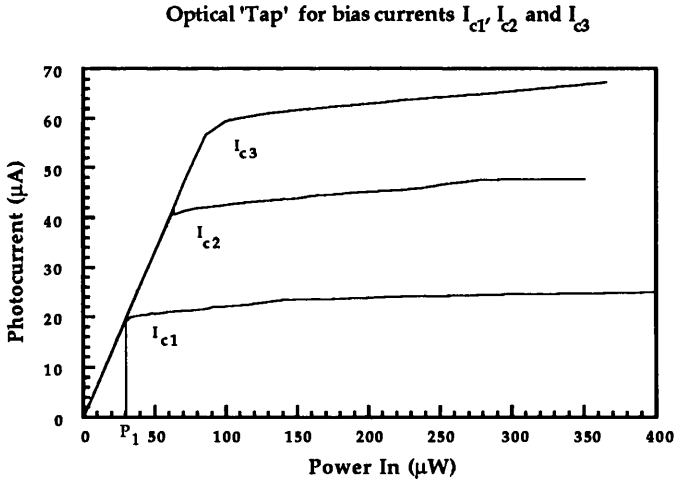

Figure 3.5 Photocurrent versus input optical power characteristics for three different constant bias currents I_{C1}, I_{C2} and I_{C3}= 20, 42 and 60μA respectively.

It is therefore seen that for a constant bias current I_c, there is a threshold power $P_1=I_c\left(\frac{hc}{e\lambda}\right)$ below which all light incident on the detector is absorbed at near maximum responsivity ≈0.69 A/W.

The device is reflective for all powers greater than P_1. For an ideal device, $P_{out}=P_{in}-P_{abs}(=P_{in}-P_1)$ therefore the slope, $P_{out}/P_{in}=1$. However the device used has non-zero insertion loss (3dB or 50% maximum reflectivity) and also transmits some of the incident light into the device substrate. As absorption falls with P_{in}^{-1}, reflection tends towards

the fixed value $R_{max}<1$. Absolute reflectivity cannot increase indefinitely as the responsivity falls. The deficit is therefore lost to recombination and transmission. The slope of the P_{out}/P_{in} curve, for optical input signals greater than P_1 is $R_{max}/(1-A_{min}/A_{max})$. In this case the slope $P_{in}/P_{out} = 0.65$ (figure 3.6a).

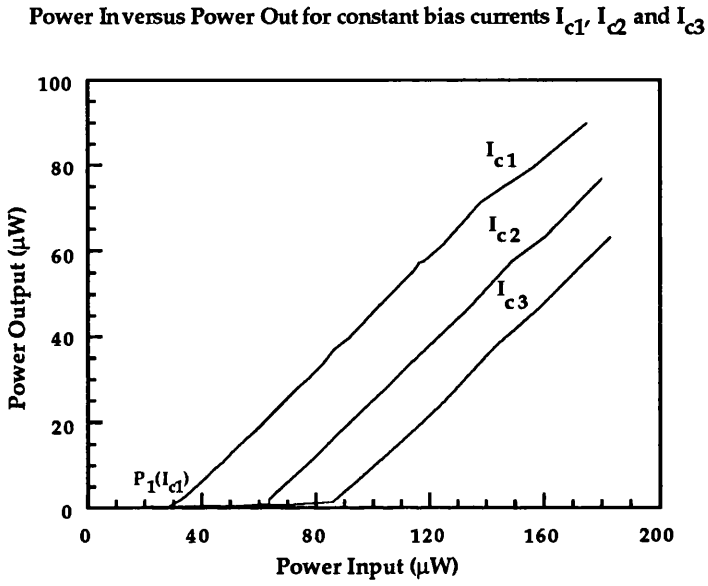

Figure 3.6a Reflected optical output power (P_{out}) versus input optical power (P_{in}) for constant current biases Ic1, Ic2 and Ic3

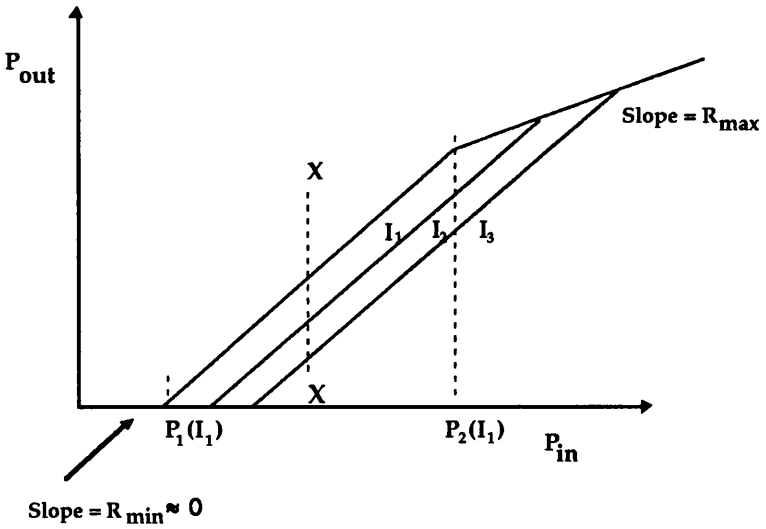

Figure 3.6b At higher powers than P_1, device reflectivity tend to its maximum, R_{max}

3.3 Significance of the optical tap

We have demonstrated using the device design available that a constant current electrical output signal level can be maintained for changes in input optical power of 6.6 dB ($\approx A_{max}/A_{min}$) whilst the surplus optical power is reflected, for a 0 to 9 volt swing [12]. By reoptimising the device design for lower 0 volt insertion loss and lower minimum absorption A_{min}, we believe this could be extended to a much larger input power range. Modulation contrast ratios have also been dramatically improved for this device making it more suitable for high bit-rate communication systems with high signal to noise ratios and applications requiring a high degree of fan-in or fan-out [13]. The device exhibits very high responsivity for optical input powers $P_{in} \leq I_c \frac{hc}{e\lambda}$ and can therefore be used as a very efficient photodetector.

Using this device configuration as the node interface in a 'daisy-chain' waveguide bus would allow nodes along the chain to efficiently extract a signal of no more than sufficient optical power from the waveguide (say to satisfy a given Signal-to-Noise Ratio). The magnitude of the power 'tapped' in 'receive mode' being controlled by an external current level. This can be seen schematically in figure 3.6b: The line X-X corresponds to the current bias I_c being varied, thus varying the magnitude of the optical power 'tapped'. The same device could also be used in 'talk mode' since it acts as a very high contrast modulator with modulation depth directly proportional to the size of the modulating current [5, 6]. However, to obtain optimum performance, over the widest possible voltage range, the existing device needs to be reoptimised to give lower minimum insertion loss and consequently lower A_{min}. A very high contrast F-P modulator structure has recently been reported [14] showing a maximum reflectivity change of >68% with an insertion loss of less than 1.65dB. These devices will also need to have their MQW structure modified to ensure rapid carrier sweep-out of the MQW material at low bias voltages [15].

Ideal device characteristics would include zero insertion loss and zero transmission. This may be partially achieved by optimising the Fabry-Perot cavity, increasing the zero-bias wavelength separation between the e1-hh1 exciton and F-P resonance. This would however increase the required device operating voltage which might prove restrictive. Marginal gains may also be achieved by increasing the reflectivity of the integrated back mirror [16]

3.4 An application of the SEED optical 'tap'
(A serial to parallel, optical to electronic, convertor)

Using the device configuration as described in sections 3.1-3.3 of this chapter, a simultaneous single stage, serial to parallel, optical to electronic conversion system can be implemented.

By cascading n optical taps (figure 3.7), a serial optical signal (M bits/s) input at one end of the chain propagates down the link through each successive optical 'tap'. Each element or 'tap' in the cascade would consist of a MQW modulator in series with a resistive load and in parallel with a zener diode and a coupling capacitor for high speed operation (figure 3.8). Each tap would be biased by a Clock current (CLK) which is normally equal to Zero. When the biasing current is zero, the voltage across each modulator is low, the devices are in a state of their highest reflectivity and the optical signal travels down the chain with minimum attenuation. (A small negative voltage may appear across each stage's resistive load, R_L due to the photovoltaic effect of the incident light).

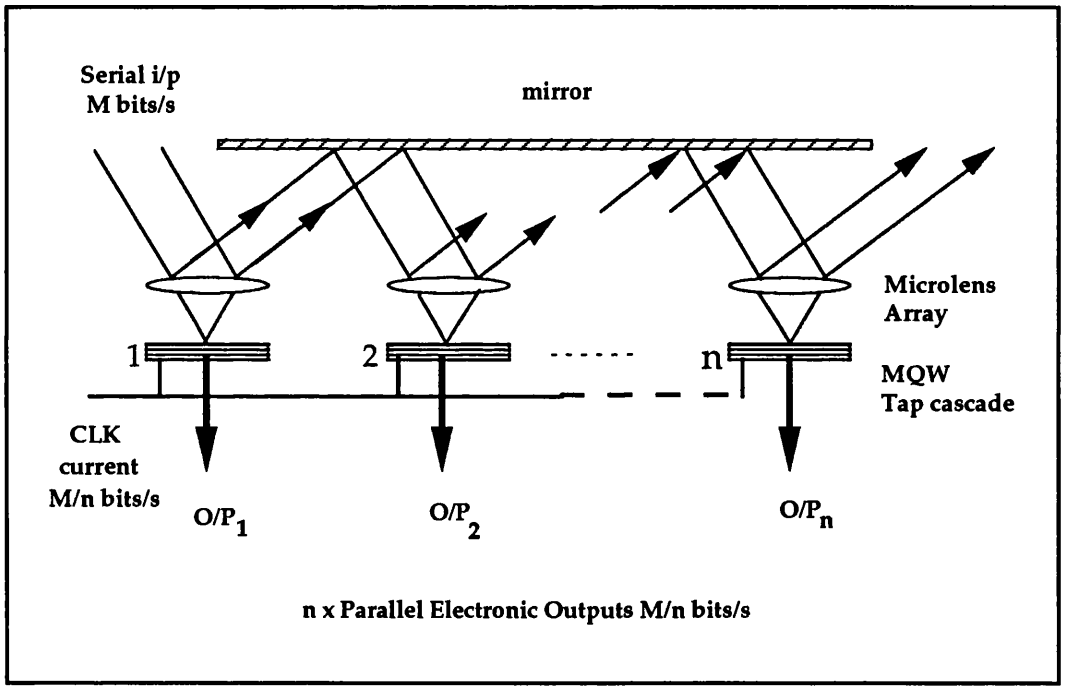

Figure 3.7 Schematic of n-element cascade, serial-to-parallel, optical to electronic convertor

The optical signal seen by each tap is delayed from that of the previous tap by a time proportional to the optical path length between each device. The n-element chain may be cascaded using free-space optics or a waveguide/fibre delay line. If the time required for the optical signal to traverse the path length between two successive stages of the cascade is made equal to 1 bit period (1/M seconds), (achieved by choosing the path length between successive elements), then at any one time, the last n bits of the serial input signal are present at the detectors of the n-element cascade.

The n-element cascade can be clocked or strobed by a fixed bias CLK current at a rate

of M/n bits/s for a time equal to one bit period. On a CLK high current strobe, the voltage across the MQW devices rapidly increases and the taps absorb power in proportion to the size of the biasing CLK current. The advantage of using the same current drive for all the devices in the cascade, is that the photocurrent output levels of each stage are equalised and compensation for optical signal attenuation down the line is accomplished. At each successive stage of the cascade, each tap absorbs proportionally more of the incident light so that the effect of signal attenuation down the chain is counterbalanced. If the incident signal level on a tap is high (logic level '1') upon CLK high, then a large photocurrent flows creating a large increase in voltage across R_L (logical '1'). If the incident optical signal is low (logic level '0'), then so is the photocurrent, device voltage is high and the bias current flows through the external zener diode and the voltage across the resistive load is low (logical '0'). Thus by using the voltages across the n resistive loads, as parallel electronic outputs, the last n serial optical bits input can be read out in parallel electrical format. With CLK returning low, subsequent sets of n bits cascade through the system, with minimum attenuation, before the next strobe and n-bit parallel electronic output. The electronic parallel output is clocked at a rate 1/n th that of the original serial optical input. This allows use to be made of the high bit-rate capacity of optical interconnection techniques, whilst the electronic processing part of the system is kept to a speed within the constraints of current electronic technology.

Device optimisation is again required for low minimum insertion loss and cascadability to larger n. Also fast carrier sweepout and low device capacitance are necessary for operation at high bit-rates [15].

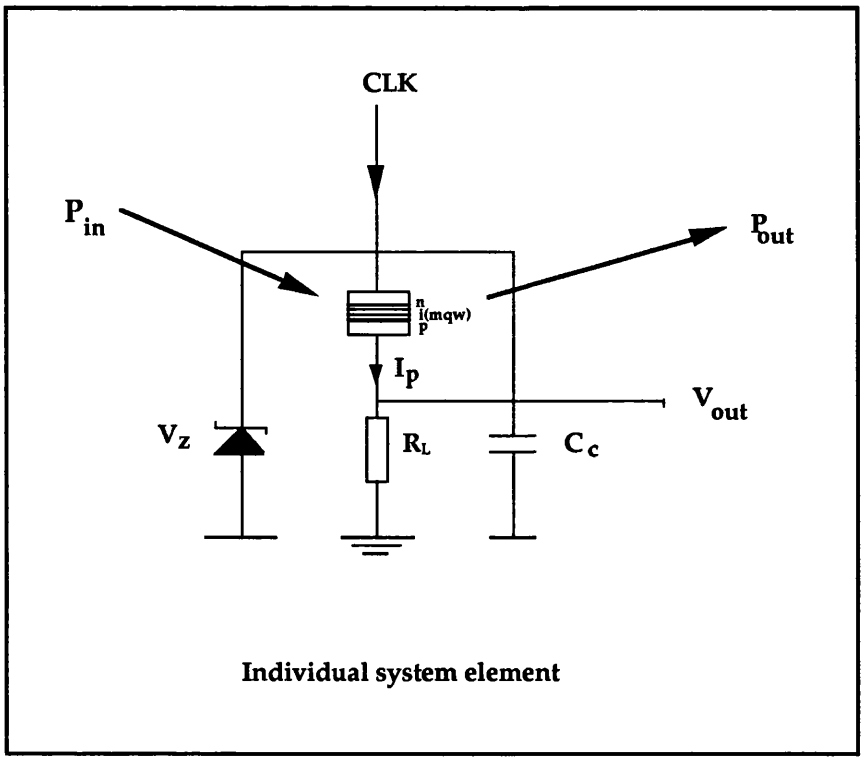

Figure 3.8 system element at each stage in the cascade

The functionality obtained from this serial to parallel, optical to electronic convertor is very similar to that required in a real telecommunications network node (figure 3.9) [17]. Optical data, generally of high-bit rate and in a serial format, needs to be received and converted to a parallel electronic signal for processing at lower data rates. After processing, a parallel electronic output needs to be converted back into a serial optical signal, for transmission to the next node in the network. A bypass mechanism is also required so that the optical signal can be directed straight through the node.

The initial serial to parallel conversion can be performed by the cascaded tap structure previously described in detail. For the reverse parallel to serial conversion to take place, the n-element 'tap' cascade may be operated in reverse. Unmodulated light could be made incident on the cascade and the parallel electronic outputs could be used to directly modulate the corresponding elements in the cascade, thereby converting the parallel electronic output to a serial optical signal. This method of modulating a serial optical signal with parallel electronic data is however rather wasteful of optical power when compared to the alternative of direct modulation of a laser source. However, the electronics required need only operate at 1/n th of the optical bit-rate and the same system can be used for both E-O and O-E conversion. This system configuration is a very simple and robust implementation of what would normally require a large amount of sophisticated, high-speed electronics to give this type of functionality. The bypass operation can be achieved by simply allowing the optical signal pass through the cascade, without clocking.

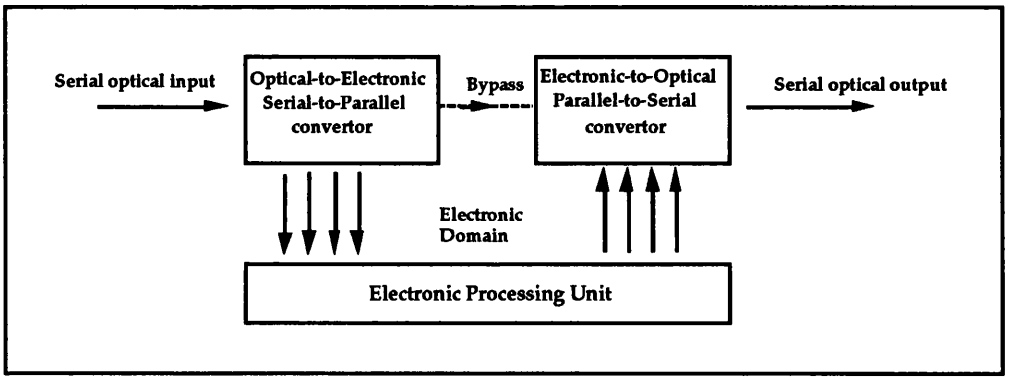

Figure 3.9 Telecommunications network node functionality

3.5 Design issues for this type of system configuration

The practicalities of optically cascading an n-element tap are non-trivial. The optical path-length between each element in the cascade should be made equal to 1 bit period. Light travels approximately 30cm in 1ns in a vacuum. For an optical signal of 1 Gbit/s, 1 bit period is 1 ns. Therefore, the optical path length between successive elements

in the cascade should equal 30cm. If the interconnect medium is glass (n=1.5) then the interconnection path length is reduced to 20cm. This implies a rather lengthy and bulky imaging system for an n-element cascade. At bit rates of 10 Gbit/s the problem reduces to a more reasonable 2cm connection delay line. Thus reasonable integration of the serial to parallel, optical to electronic, single stage convertor would only be possible at quite high bit-rates. The interconnection length between successive 'taps' should all be the same distance. However, some margins for alignment error should be defined. For example a timing tolerance of ± 5% of a bit period @ 10Gbit/s gives a necessary alignment accuracy of ± 1.5mm for each interconnection between elements. This represents a reasonable tolerance in the manufacture of an integrated optical imaging system. The interconnection of elements in the cascade could also be achieved by fibre delay lines between each stage. However, at higher bit-rates and for relatively short lengths of fibre, this would represent a considerable manufacturing problem. Additionally the losses incurred coupling light into and out of the fibre would probably give rise to a very severe power budget penalty. An extra dimension could be added to this system by having multiple optical input channels and a planar imaging system interconnecting parallel cascades.

3.6 Other applications: Wavelength conversion, T-SEEDs etc.

In this chapter, the bias current I_c driving the MQW modulator was obtained from a variable electronic constant current source. However, an ordinary photodiode with light shining on it also acts as a very good current source. Therefore, if a silicon photodiode is reverse biased in series with the MQW modulator, then the constant photocurrent generated, I_c, is directly proportional to the light incident on the photodiode [5] (figure 3.10). Therefore, increasing the light incident on the photodiode increases the biasing photocurrent which causes the absorption of the pump beam incident on the MQW modulator to increase accordingly. Conversely, decreasing the incident power on the photodiode, causes the MQW modulator to decrease its absorption of the pump beam. The light shining on the photodiode can of course be incoherent, therefore an incoherent input signal incident on the photodiode can be used to modulate a constant, coherent light beam incident on the MQW modulator. The system is behaving as a 'linearized, inverting, light-by-light modulator and incoherent-to-coherent convertor'. Under the presence of positive rather than negative feedback, this circuit operation is the same as the Diode or D-SEED, as discussed in 2.3.2.

Instead of using a photodiode as the current source, a phototransistor can be used to bias the MQW modulator [18]. A small incident optical signal on the phototransistor is therefore amplified giving rise to a large bias current (due to the gain of the transistor). The quantum efficiency η of this optical to electrical conversion is effectively greater than unity, because of the gain of the phototransistor. The small input signal can therefore be used to modulate a larger pump signal power. This device configuration proposed by Wheatley et al. [11] is known as the transistor or T-SEED (figure 3.11). It has been suggested that this device with 'gain' and its limited response outside its self-linearised region, can be very usefully used in optical logic systems.

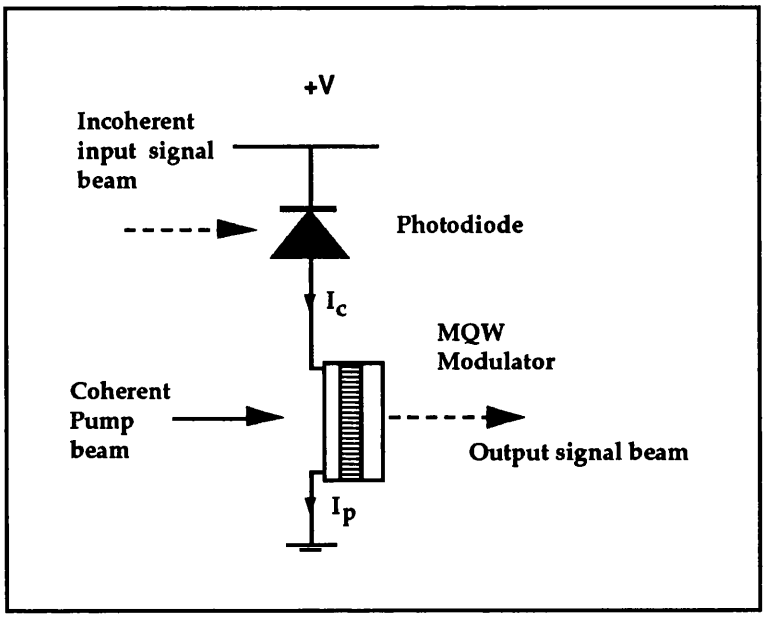

Figure 3.10 Incoherent to coherent convertor

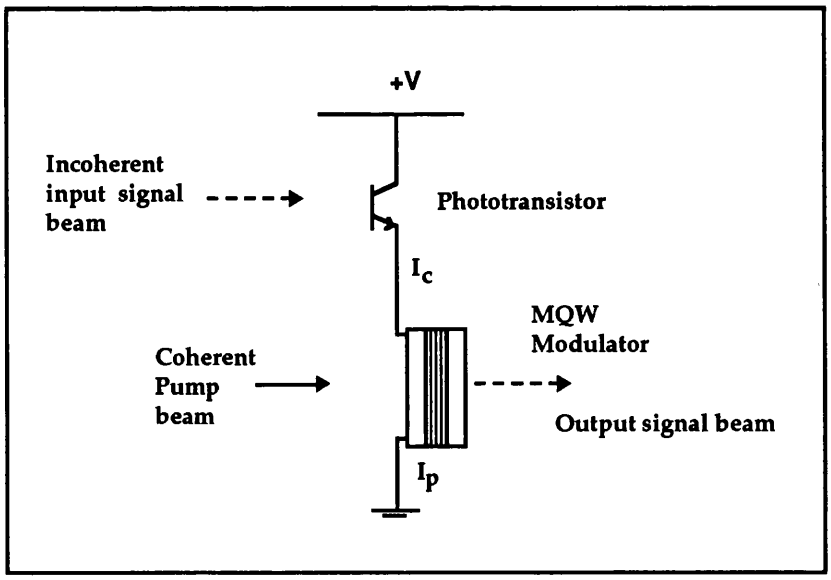

Figure 3.11 Transistor or T-SEED

A further sophistication proposed is to integrate field-effect transistors (FETs) with photodiodes and MQW modulators to make Field-Effect Transitor SEEDs (F-SEEDs) [19]. This allows the possibility of electronic circuits with many optical inputs and outputs. The resulting optical pin-ins and pin-outs can be very small and can be accessed with 2-

dimensional arrays of light beams. Additional functionality can be obtained between inputs and outputs by using electronic techniques. Such a technique allows optics and electronics to be used to their best advantage - Optics provides the interconnect and electronics the processing functionality. This is a manifestation of the 'Electronic Islands' or 'Smart Pixels' architecture [20] where small islands consisting of very high speed electronics are interconnected by high speed optical channels. This type of architecture alleviates the pin-out problem of electronic circuits by taking advantage of the 3-D, parallel interconnect that optics brings to systems design. Also, because interconnection over distance is carried out optically, electronic track lengths are small and very high speed operation can be achieved.

3.7 Conclusions

This chapter has demonstrated how the asymmetric Fabry-Perot design can significantly improve the device characteristics of SEED self-linearised modulators. A way of using these devices in the context of an optical 'tap' was also discussed. A highly functional and compact serial-parallel, optical-electronic convertor configuration was proposed and is a very useful demonstration of how simple optical techniques can be used in conjunction with electronics to yield a highly functional and yet more simple and efficient data processing system than would previously been possible with just conventional electronic technology.

3.8 References

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CHAPTER 4

Enhanced functionality of the S-SEED for use in optical switching systems

4.1 Limitations of current optical switching devices

Optics offers many attractive features for use in telecommunications, computing and the high capacity interconnection of electronics [1]. Optical fibre has now, due to its low cost and huge capacity, almost entirely displaced co-axial cable in long-distance terrestrial communications links [2]. Recently, the advent of the optical fibre amplifier [3], has enabled optical signals to be amplified without first having to convert the signal into an electrical one. As transmission becomes less of an issue in telecommunications networks, more attention is being directed towards switching and how it can benefit overall network performance. With the all-optical transmission of telecommunication signals over larger and larger distances it becomes more and more desirable to be able to perform switching and logical processing operations on optical signals without first having recourse to the speed limiting, electronic domain.

Asynchronous Transfer Mode (ATM) is a packet based transmission format in which data is grouped in 48 byte bundles contained within a packet or cell of 53 bytes. The cell also consists of a 5 byte header in which the cell's destination address is contained. Individual cells are 'posted' over the network to their respective destinations with each ATM cell being treated exactly the same on their routing through the network, regardless of their service origin. Higher bit-rate services such as TV simply send out more ATM cells to satisfy their increased bandwidth requirements. ATM allows different bit-rate services to make efficient use of available network bandwidth by the statistical multiplexing of many cells on high capacity broadband channels [4]. For this reason the CCITT has chosen ATM as the target transfer mode for B-ISDN (broadband integrated services digital network) However, ATM switching requires very much more computing and processing than circuit switched ISDN telephony channels at 64 Kbits/s which have relatively long holding times. An evolutionary approach from the proposed synchronous network (SDH or SONET [5]) to full scale ATM would include the asynchronous multiplexing of many ATM cells (going towards the same destination) onto the payload envelope of a much larger synchronous packet or timeframe [5]. This would require switching at a far lower rate than necessary for individual ATM cells. Given the dramatic increase in processing overhead by switching individual ATM cells rather than using current circuit switched techniques, it may be very desirable for individual ATM cells to be able to self-route through a switch to their network destinations. One such switch type is the Batcher-Banyan routing network of which the 'Starlite' switch is an example [6]. At each stage in this switch, a simple logical operation is performed on the cell header which determines whether the cell is exchanged or bypassed. This is a non-blocking switch architecture whose size scales very favourably with switch size. It would of course be very convenient to be able to perform this logical operation and self-

routeing, optically and 'on-the-fly', thereby distributing control of the switch and the routeing of cells over the entire switch fabric. To implement in electronics, this normally requires a small processor with order of 100 gates per exchange-bypass stage.

A number of technologies exist that can switch or route optical signals. These can be divided into two main categories based on their device characteristics in photonic switching architectures [7]. Firstly, 'Relational' or 'Passive' devices are optical switches that perform a mapping function between given inputs and outputs depending on the state of some control signal (figure 4.1). These devices are transparent to the service bit-rate passing through them and therefore their bandwidth can be very large, however, they have no ability to extract information from the bits throughput. Optical switches of this kind would include mechanical fibre switches [8] and planar waveguide switches, for example in $LiNbO_3$ [9]. The second category of optical switches are 'logic' devices in which an optical signal interacts with the device in such a way that controls the state of the switching device (ie. ON or OFF). These devices sense individual bits and can perform various boolean logic operations. However, because of their strong interaction with individual bits the maximum transmitted bit-rate that may be conveyed is limited because of the need that some of the devices in a system must be able to change states or switch as fast or faster than the signal bit-rate. An optical logic device of this type is the bistable Self-Electro-optic Effect Device (SEED) [chapter 2, 10, 11], which uses the Quantum Confined Stark Effect [12] in semiconductor multiple quantum wells to alter its absorption of light.

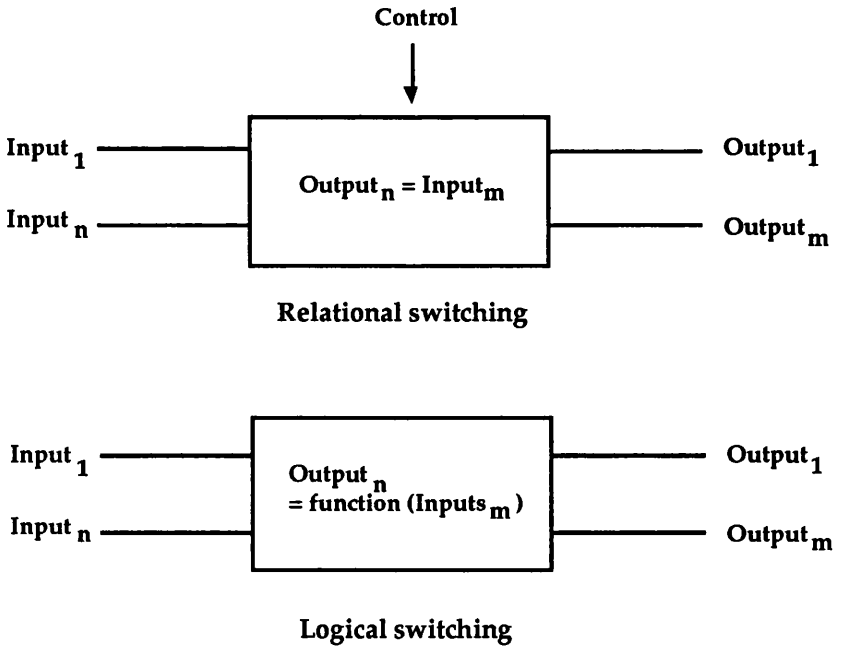


Figure 4.1 The two main categories of optical switching devices: Relational and Logical

Because of the relative characteristics of the various logic devices available, ie. relational devices (high bandwidth and data transparency, but no logical operation) and logical devices (optical processing functionality but much lower bandwidth), perhaps the advantages of both can be used in some 'hybrid' network switching fabric. Up until quite recently however, it has been difficult to consider the usage of current optical logic devices in real systems applications. High power, critical biasing and accurate temperature control device requirements have meant the slow evolution of these devices from the laboratory into practical systems. However, the SEED and in particular the symmetric or S-SEED, overcome many of these difficulties [13]. Its dual-rail differential logic operation, low switching energies and wide bistable hysteresis width lend it to some very interesting systems applications. The S-SEED has already been proven useful in optical computing applications such as optical clock extraction [14] and wavelength modulation/conversion [15]. It can also be used as a self-linearised modulator [16] or an optical 'tap' [17]. A whole range of SEED devices can now be fabricated in large arrays [18] and with varying operating characteristics, such as very high contrast [19] and low voltage [20].

Current S-SEED computing architectures however, are operated in a rigidly clocked synchronous mode. Logical functionality is obtained in return for the penalty of increased system complexity arising from a number of optical beams being incident on individual devices and the requirement for strict clocking techniques [21]. It will be shown in this chapter, how the S-SEED can be used in a more flexible manner, combining the properties of both relational and logic devices, enabling quite sophisticated functionality and a degree of transparency to be achieved for a number of very simple control algorithms, in the context of a self-routeing, optical packet switch [22, 23].

4.2 Added functionality of the S-SEED

4.2.1 Theory - Two modes of operation

An S-SEED consists of two PIN, Multiple Quantum Well (MQW) modulators reverse biased in series [13], figure 4.2.1a. The MQW modulators are operated at a wavelength corresponding to the unbiased e1-hh1 exciton peak and exhibit decreasing absorption and photocurrent for increasing applied voltage. They therefore have negative differential resistance, (ie. increasing device absorption/photocurrent for decreasing applied bias and vice-versa), the condition required for positive feedback and bistability [10]. If the optical power incident on one of the diodes is sufficiently greater than the optical power incident on the other diode, positive feedback causes the entire supply voltage to be seen across the diode with the least light incident upon it; the other diode experiencing a very low voltage. One diode is operating in a low voltage, high absorbing state and the other is experiencing an high electric field, and operates in a low absorbing state. The S-SEED is bistable in the ratio of its two optical input signals. (See chapter 2 for a more detailed explanation).

S-SEED operation can be easily understood by the use of current loadlines (figure 4.2.1b). The two light solid curves are the photocurrent versus voltage characteristics of $diode_1$ of the S-SEED, for two optical input powers, P_1 and P_2. The heavy solid curve is the photocurrent of $diode_2$ ($diode_1$'s load) for an incident optical signal power, $P_{in_2}= P_{bias}$. Optical power incident on $diode_2$ is held constant at P_{bias} and the optical power, P_{in_1} incident on $diode_1$ is ramped up and down. If P_{in_1} is sufficiently greater than P_{bias} (ie. $P_{in_1}>P_2$), then the only S-SEED loadline intersection point is at a, with all the supply voltage seen across $diode_2$. If P_{in_1} is decreased to a value sufficiently less than P_{bias} (ie. $P_{in_1}<P_1$), then the only possible operating solution is reversed to that at b, the entire supply voltage now being seen across $diode_1$. For optical powers P_{in_1}, with $P_1<P_{in_1}<P_2$, the S-SEED is bistable, with a total of three possible operating points, two of which are stable [10]. For optical powers between these limits, the S-SEED remains in either of the states a or b because the difference between the two input powers is not sufficient to cause the S-SEED to alter its state. For reflective SEEDs there is a corresponding change in device reflectivity as the S-SEED switches states. In either stable state, one of the MQW diodes is more reflecting than the other, due to the change in device absorption with voltage (Quantum Confined Stark Effect [12]).

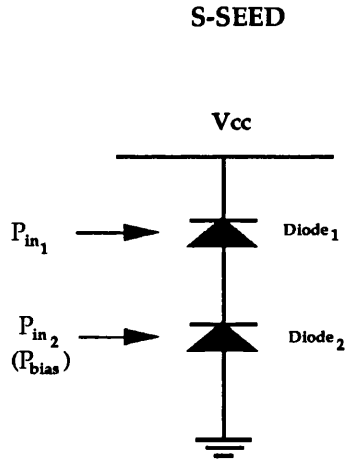


Figure 4.2.1a Schematic diagram of the Symmetric-SEED configuration

It can be seen from figure 4.2.1b, that when P_{in_1} is increased to a power P_2, such that the two curves intersect at points **d** and **a**, a further increase in P_{in_1} will cause the device to switch its operating point from **d** to **a**. Just at the point **d**, the *minimum* photocurrent generated by $diode_1$ for an incident optical power P_2 is equal to the *maximum* photocurrent generated by $diode_2$ for an incident power P_{bias}; ie. $A_{min}\frac{e\lambda}{hc}P_2 = A_{max}\frac{e\lambda}{hc}P_{bias}$. If P_{in_1} is increased beyond P_2, the photocurrent from $diode_1$ acts to charge up $diode_2$ and the S-SEED changes its operating point to that at **a**. Conversely, at operating point **c**, the minimum photocurrent generated by $diode_2$ for P_{bias} is equal to the maximum photocurrent through $diode_1$ for an optical power P_1, (ie. $A_{min}P_{bias} = A_{max}P_1$). If P_{in_1} is made smaller than P_1, $diode_1$ charges up, $diode_2$ discharges and the device switches its stable operating point to **b**.

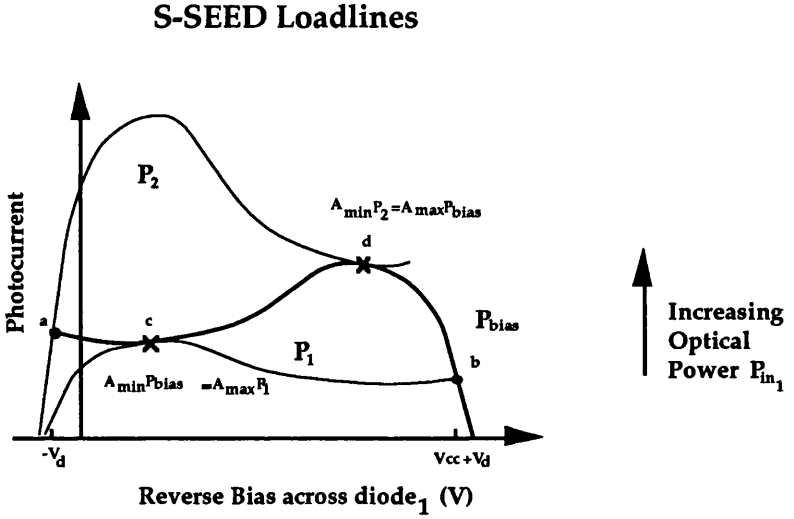


Figure 4.2.1b S-SEED loadlines and device operation

It is thus seen that $P_2=\left(\frac{A_{max}}{A_{min}}\right)P_{bias}$ and $P_1=\left(\frac{A_{min}}{A_{max}}\right)P_{bias}$. The required input contrast ratio (RICR) of the two input signals is therefore 1:C, where $C=\left(\frac{A_{max}}{A_{min}}\right)$, in order to cause S-SEED switching. The width of the bistable S-SEED region, $\Delta P=(P_2-P_1)$ for a given bias beam P_{bias} is $\Delta P = P_{bias}\left(\frac{A^2_{max} - A^2_{min}}{A_{max}A_{min}}\right)$. A_{max} and A_{min} can be varied by device design therefore S-SEEDs may be fabricated with specific hysteresis widths to suit the intended systems application.

A schematic S-SEED bistable, hysteresis plot is shown in figure 4.2.2. Optical power incident on diode$_2$ of the S-SEED is held constant at P_{bias} and power on the other input, P_{in_1} is ramped up and down. P_{out} reflected from diode$_1$ is shown on the y-axis. By driving the S-SEED with input powers $P_{in_1}=P_2$ and $P_{in_2}=P_{bias}$, a further increase in P_{in_1} causes the photocurrent from diode$_1$ (charging diode$_2$) to exceed the photocurrent discharging diode$_2$. Upon switching with $P_{in_1}>P_2$, device reflectivity changes from a maximum, R_{max} (corresponding to low absorption at operating point d), to a minimum reflectivity R_{min}, corresponding to maximum absorption for low electric field (operating point a). For $P_{in_1} < P_1$, the device switches from a minimum reflectivity (maximum absorption) at operating point a, to a minimum absorption and maximum reflectivity at operating point d. The greater the difference in the input powers and photocurrents, the faster the charge transfer and the more quickly switching occurs. Switching time from one state to the other is $\Delta t \approx C_{tot}V_{cc}/S(P_{in_2}-P_{in_1})$, where S is the average MQW device responsivity (A/W) [13]. The optical switching energy E_{opt} required to switch the S-SEED is constant and can be approximated by $E_{opt} \approx \Delta t\, \Delta P'$, where $\Delta P'$ is the difference in the optical input powers $(P_{in_2}-P_{in_1})$. If P_{in_1} is only infinitesimally greater than P_2 or infinitesimally less than P_1, then the S-SEED will take a long time to switch. This is the characteristic of critical slowing down [24]. Therefore to quickly change the state of the S-SEED, P_{in_1} should be much greater than P_2 or much less than P_1, for a given bias power $P_{in_2}=P_{bias}$.

It is important to note that the constant biasing power $P_{in_2}= P_{bias}$ on diode$_2$ does not correspond to the power at the exact centre of the bistable hysteresis curve. This is because the magnitude change in device photocurrent with voltage depends on the absolute power incident on the device. For $\left(\frac{A_{max}}{A_{min}}\right)=2$ and $P_{bias}=100\mu W$, $P_2 = 200\mu W$ and $P_1 = 50\mu W$. A different real change in power on one of the S-SEED inputs is required depending on the direction of switching, ie. V_{centre} (the centre voltage of the S-SEED) going from high to low, or vice-versa. The relative position of P_{bias} in the hysteresis plot is given by:

$$P_{bias\,(rel)} = \frac{P_{bias}-P_1}{P_2-P_1} = \left(\frac{A_{max}A_{min}-A^2_{min}}{A^2_{max}-A^2_{min}}\right)$$

(Where $P_{bias\,(rel)}= 0.5$ when P_{bias} coincides with the exact centre of the hysteresis plot, for the non-bistable case when $A_{max}=A_{min}$. For all values of $A_{min} < A_{max}$, $P_{bias(rel)} < 0.5$, the position of P_{bias} moves to the left of the centre of the hysteresis plot).

For 'AC' optical input signals, ie. when logic 0 corresponds to zero power incident at an S-SEED input, signal combinations 10 and 01 will always be sufficient to cause the S-SEED to switch, (because when $P_{bias}=0$, P_{in_1}=logic 1 is always greater than P_2). The greater the power level corresponding to logic level 1, the faster the S-SEED changes states. The S-SEED switching time Δt, should be sufficiently smaller than the incident signal bit-rate t_b ($\Delta t << t_b$), so that the S-SEED can fully latch on each successive input bit pair. When both inputs are high however (ie. 11), the S-SEED remains latched in its previous state because the difference between its two input signals should not be sufficient to cause the S-SEED to change its state - the S-SEED is operating in its bistable region. If a constant optical bias control signal is added to the two AC digital signal inputs, the control signal power effectively degrades the input contrast ratio of the two input signals. If a large enough control bias is simultaneously applied to both S-SEED inputs, the input contrast ratio falls below that required to induce switching, and the S-SEED remains latched in the same state it was in, prior to the application of the control bias. The S-SEED operates within the confines of its own bistable hysteresis loop, remaining latched in either of its two stable states, regardless of the AC component of the two input data streams (figure 4.2.2).

The condition for non-switching is that the maximum power difference between the two input channels does not exceed the S-SEED required input contrast ratio, $C=\left(\frac{A_{max}}{A_{min}}\right)$. This implies that when a 0 and 1 are present at the S-SEED inputs, that the AC+Control bias signal power (corresponding to logic 1) is not sufficiently greater than the control signal power on its own (corresponding to logic 0), so as to cause the S-SEED to change states.

ie. AC+Control must be less than $\left(\frac{A_{max}}{A_{min}}\right)$Control

$$\Rightarrow \quad AC < \left(\frac{A_{max}}{A_{min}} - 1\right)\text{Control} \qquad \text{(S-SEED non-switching signal format)}$$

Conversely the condition for the S-SEED to change states, ie. S-SEED switching, is that the ratio of the two input intensities is greater than $\left(\frac{A_{max}}{A_{min}}\right)$.

$$\Rightarrow \quad AC > \left(\frac{A_{max}}{A_{min}} - 1\right)\text{Control} \qquad \text{(S-SEED switching signal format)}$$

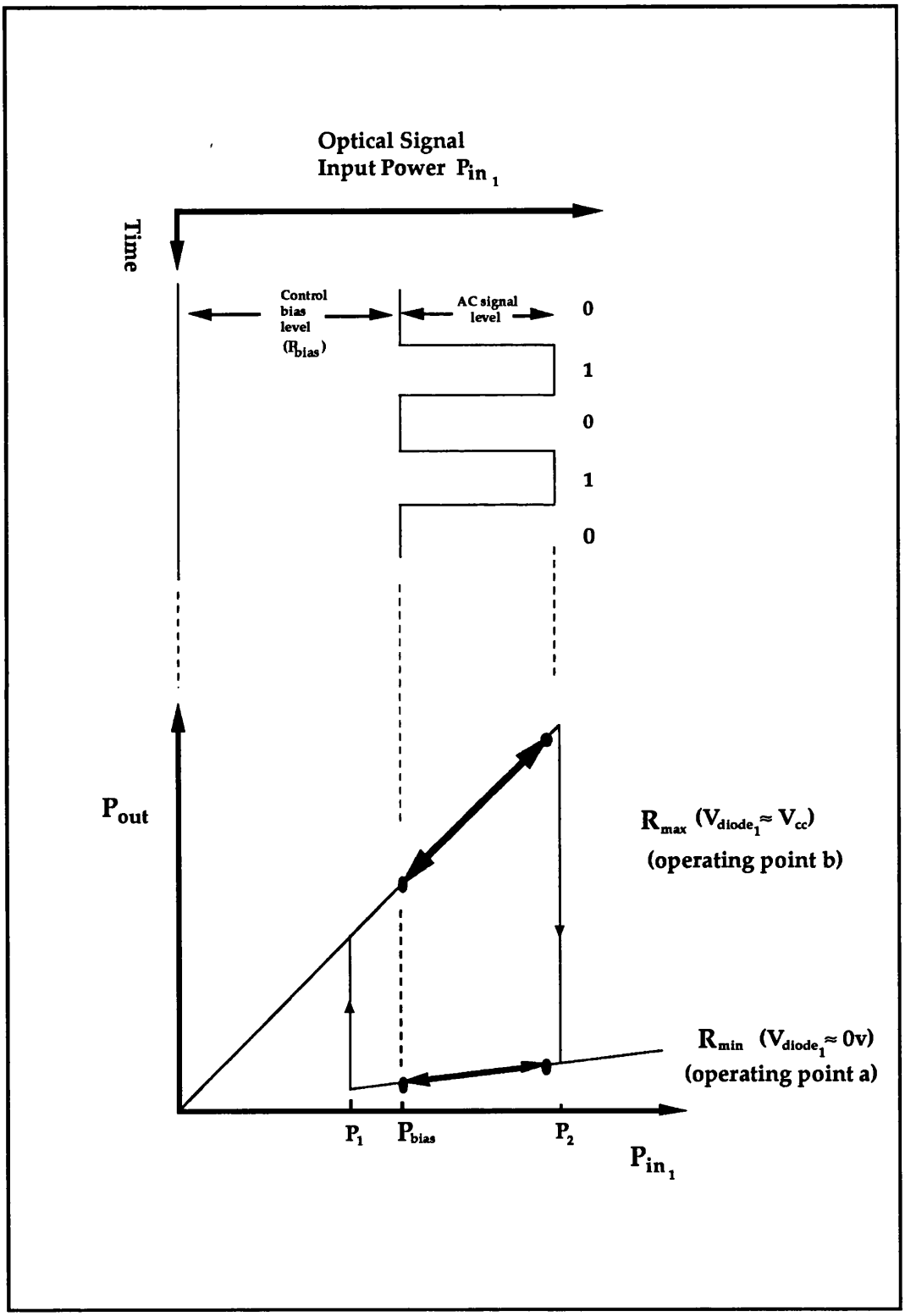


Figure 4.2.2 S-SEED bistable hysteresis schematic

Another variation on this way of using S-SEEDs is due to the fact that when no optical power is incident on the S-SEED, once the S-SEED has stabilised through its leakage currents, each diode of the S-SEED experiences the same voltage across it, $V_{centre} \approx V_{cc}/2$. If two equal input power beams are applied, the device operates in this unstable state [25]. A small difference in optical powers will push the S-SEED in one direction or the other, to one of its stable states. This mode of operation is known as 'optical sense amplification' and in this case not all the switching energy is derived from the signal beams, some of it is obtained from the bias beams so that a small difference in input powers is enough to cause the S-SEED to latch [26]. If an optical signal incident on the S-SEED is in non-switching format and the S-SEED is operating at $V_{centre} \approx V_{cc}/2$, then if the first bit of each of the input signals are different, ie. 01 or 10, then this difference is enough to cause the S-SEED to latch to whichever state. Once the S-SEED has latched on the first bit difference of the two inputs, then it remains latched for the remainder of the optical signal input, since the signal inputs are in S-SEED non-switching format. For this technique to be successful, the power difference between 1 and 0 signals (ie. the amplitude of the AC information signal) must be sufficiently greater than the control bias level so as to latch the S-SEED within one bit interval, for a given signal power, ie. $\Delta t(01, 10) << t_b$. If the first input bits are 00 or 11, then the two input signal powers should be sufficiently similar so as not to latch the S-SEED in one bit interval, $\Delta t(11, 00) >> t_b$. The S-SEED should remain unlatched until the first bit *difference* of the two data signals.

4.2.2 Applications for this way of using the S-SEED

There are therefore two possible modes of operation of the S-SEED. The first of these is the conventional 'logic' or 'bit-sensitive' mode, in which when the signal inputs to the S-SEED are AC, the S-SEED changes its state depending on whether its inputs are 01 or 10. The S-SEED is acting as an optical logic device whose present state depends on its current inputs. The second mode of operation is the 'relational' or 'bit-insensitive' mode, which when control optical bias beams are applied to the two S-SEED inputs, the S-SEED remains latched in its state prior to the application of the control bias. The S-SEED is now acting as a passive or relational device which suppresses one of its input signals with respect to the other, (due to the difference in the two diode reflectivities), depending on which of the two stable states the S-SEED has latched. The S-SEED now passes or suppresses one of each of its inputs (to varying degrees, depending on the S-SEED component device parameters of absorption, A_{max} and A_{min} and reflection, R_{max} and R_{min}) and passively relates the inputs to their outputs in a bit-transparent mode of operation. These control optical beams can be generated locally to the switch, to obviate the necessity to transmit control signals alongside of the data signals. It is shown schematically in figure 4.2.3, that in 'logic' mode the S-SEED changes its state with the inputs 10 and 01, remaining in that state for the inputs 00 and 11. When the optical control bias is applied the S-SEED remains latched regardless of the combination of bits

at its inputs (relational mode) with one diode highly absorbing and the other reflecting. Operating the S-SEED in this simple manner, (ie. the adding or removing of a control optical bias signal which controls whether the device can switch its state or not), combines the advantages of both optical logic and relational devices. Using S-SEEDs in these two modes of operation can, with a few very simple control algorithms, provide for relatively complex optical processing functionality in photonic switching fabrics.

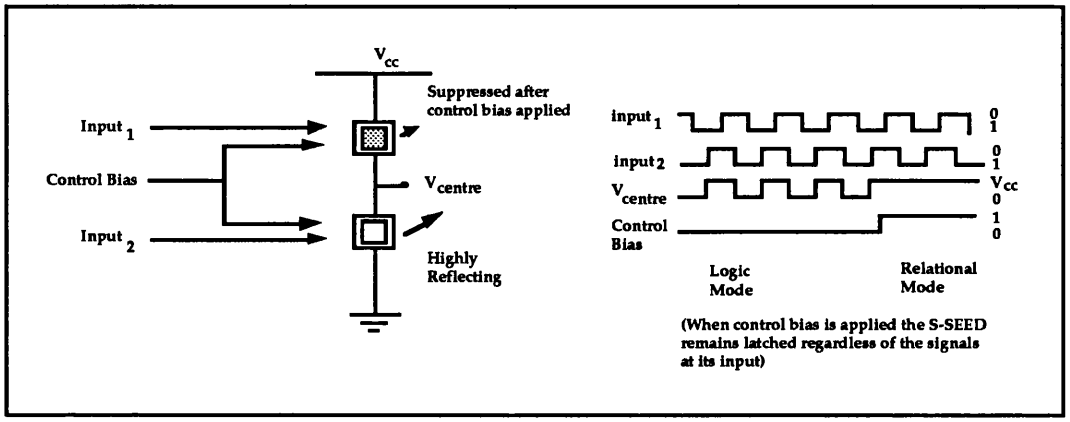


Figure 4.2.3 The two modes of S-SEED operation

If the signals arriving at the inputs to an S-SEED are in the form of two, bit-synchronised optical data streams in Least Significant Bit (LSB) first format, then the S-SEED changes its state as the inputs vary from 01 to 10. If these data signals are followed by a control bias signal in non-switching format, then the S-SEED remains latched in a state corresponding to the Most Significant Bit (MSB) difference of the two data streams. If the serial binary number at $input_1$ is greater than that at $input_2$, then the S-SEED latches in the state $V_{centre} \approx V_{cc}$; If the reverse is true the S-SEED remains latched with $V_{centre} \approx 0$. A magnitude comparison between two binary optical signals has therefore taken place. This represents a very simple task for an S-SEED operating in this fashion but would be a significant feat for conventional electronics, requiring a significant number of logic gates. This type of functionality combined with switching on the first bit difference of two data streams as described above, can lend itself to some interesting system applications. This type of functionality is similar to that required in a Batcher-Banyan or 'Starlite' type switching fabric (figure 4.2.4), where optical packets or cells need to be routed according to the magnitude of their header destination addresses. A 2x2 switch is the basic building block for this type of multistage interconnection network (MIN). Columns of switches are interconnected by interconnect patterns which allow rearrangability and non-blocking of the switch. This type of switching fabric scales well with increasing switch size and offers non-blocking paths between any input and any output. Two cells are input into a switch and are exchanged or bypassed depending on which header address is the greater, (eg. Batcher sort: at each 2x2 stage, the cell with the largest header gets routed in the direction of the arrow) or whether a particular bit in a header is either 1 or 0, (eg. Banyan routeing stage). Once the S-SEED has latched on

an incident header, the ensuing data, in S-SEED non-switching format, is passively reflected and related independently of its bit-rate. The advantages of both logic and relational devices, (ie. bit sensitivity and transparency), are thus utilised by this way of using S-SEEDs.

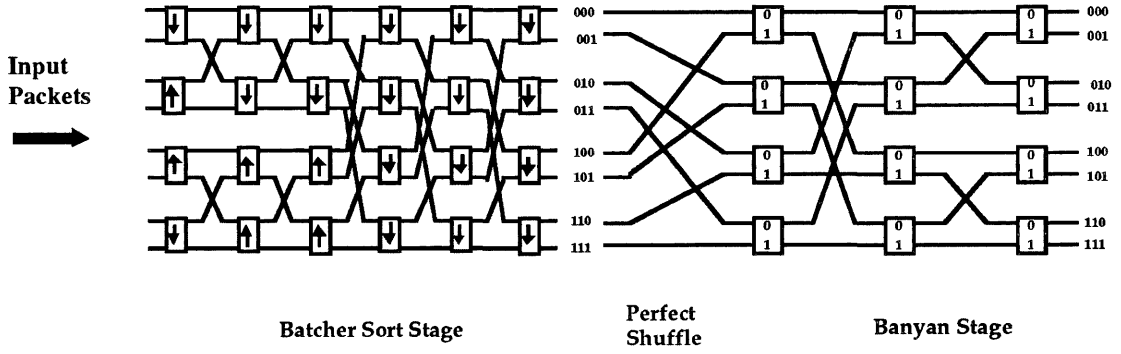


Figure 4.2.4 Batcher-Banyan routing network

4.2.3 Experimental set-up, procedure and device structure used

The SEED devices used in this experiment were of an asymmetric Fabry-Perot, Multiple Quantum well (MQW), type structure as reported in [27] and whose device characteristics are described in (2.5). The MQW device structure was grown by MOVPE and is a normally-off (Bias-reflecting) asymmetric Fabry-Perot modulator [28] consisting of a 15 x (150Å GaAs well / 60Å $Al_{0.3}Ga_{0.7}As$ barrier) intrinsic region sandwiched between p-type and n-type layers (figure 4.2.5). The unbiased e1-hh1 exciton peak wavelength was aligned with an asymmetric Fabry-Perot cavity resonance, and cavity reflection at zero field is made low by virtue of matching the top and effective bottom mirror reflectivities. Upon increasing the applied electric field across the device intrinsic region, by way of the Quantum Confined Stark Effect (QCSE) [12], the e1-hh1 exciton red-shifts and loses oscillator strength. As cavity absorption falls the cavity becomes asymmetric and device reflection increases. The front and back mirrors are formed by the air/GaAs interface (R=0.3) and an integrated p-type semiconductor multiple quarter wave stack of R≥0.95 respectively. Maximum absorption for these MQW devices is $A_{max}\approx 0.80$ for a forward bias voltage of about 1 volt (to counteract the diode's built-in field) and minimum device absorption, $A_{min}\approx 0.44$ for a reverse bias voltage of 2.5 volts. A corresponding device reflection change from 10% to approximately 50% occurs for the same voltage swing, ie. a 5:1 reflection contrast ratio.

(For the devices used, $\left(\frac{A_{max}}{A_{min}}\right)$ was measured from photocurrent spectra to be ≈1.8)

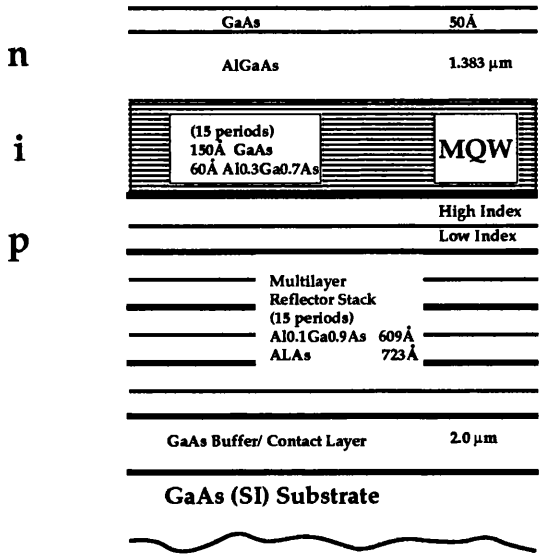


Figure 4.2.5 Device structure used (QT74)

The experimental set-up was as shown in figure 4.2.6. An Argon-ion laser pumped tunable Ti:Sapphire laser was used as a source of continuous light at 860 nm, from which four separate beams were obtained. Two of these beams were 'AC' modulated by simultaneously passing them through an optical chopper. The chopper was arranged so as to modulate the two signals with each of the possible combinations of 1 and 0 in a repeating series, (ie. 00, 01, 11, 10 etc.). (The effective bit-rate of these AC header and data signals could be varied by slowing down or speeding up the optical chopper). Each of the AC signal beams was directed onto the corresponding input diode of a discrete device S-SEED which was configured so that it could easily be changed into two R-SEEDs (2.3.1) and vice-versa. Two constant power or control beams were also made incident on each S-SEED input. The magnitudes of the AC and control optical signals incident on the two S-SEED inputs were measured by reverse biasing the two SEED devices, separately, in series with a resistive load (R-SEED configuration [10]). Photocurrent flowing through the SEED devices was measured as a voltage drop across the R-SEEDs' 33kΩ resistive loads. A direct comparison of the relative magnitudes of the incident AC and control powers incident on the two inputs could therefore be made on the oscilloscope screen. The magnitudes of the signal and control optical signals incident on the two S-SEED inputs were controlled using variable attenuators and neutral density filters. Because discrete devices were used to make up the S-SEED, devices manufactured from slightly different parts of the wafer exhibited slightly different behavior, with the consequence that, as with electronic devices, it was difficult to match up the devices exactly. By examining the magnitude of the photocurrents flowing through the separate devices configured as

R-SEEDs, rather than the optical power incident, it was easier to allow for any differences in their maximum and minimum absorptions ensuring their respective values of (A_{max}/A_{min}) were similar. Measuring photocurrents flowing through the resistive loads of the R-SEEDs, rather than the incident optical power, allowed accurate matching of the photocurrents by defocussing the light incident on the individual devices.

{The frequency shift, $\Delta\omega$ of a light wave of frequency ω_l, as it passes through an acousto-optic modulator and diffracted by a sound wave is given by: $\Delta\omega=\omega_s$ [29], (where ω_s is the frequency of the acoustic wave, measured in this case to be $\omega_s \approx 7x10^8$ rads/s). The shift in frequency, $\Delta\omega$ of the light wave was therefore negligible compared to its frequency ($\omega_l \approx 2x10^{15}$ at 860nm). The frequency shift translates to a wavelength shift of less than $1x10^{-3}$ nm and can therefore be discounted}.

Two photodetectors D_1 and D_2 were used to monitor the two optical input signals (P_{in_1} and P_{in_2}) incident on the S-SEED. The two optical input channels and the voltage between the two devices, V_{centre} (showing the present state of the S-SEED), were observed on an oscilloscope screen. The 1st order diffracted beam of an acousto-optic modulator located at (A), was used to generate the control signal beams incident on the S-SEED. The control signal beams could therefore be easily turned on and off at a variable frequency and duty cycle, controlled by a variable function generator via the blanking input to the acousto-optic modulator supply. The blanking input to the acousto-optic modulator was used to trigger the oscilloscope so that the effect of adding and removing the optical control bias to the information signal, on the S-SEED could be observed. By removing or allowing the optical control bias, the difference between header and data signals of an ATM cell or packet was simulated. This was used to demonstrate the S-SEED latching on the MSB difference of two input packet headers. The acousto-optic modulator was subsequently moved to position (B), so that all light incident on the S-SEED could be either totally transmitted or suppressed. The transmission of light through the acousto-optic modulator on to the S-SEED was used to simulate the arrival of an optical packet signal after a period of switch inactivity. This was used to demonstrate S-SEED latching on the first bit difference of two input signals in non-switching format as used in the Banyan routeing stage of the 'Starlite' type switch (figure 4.2.4).

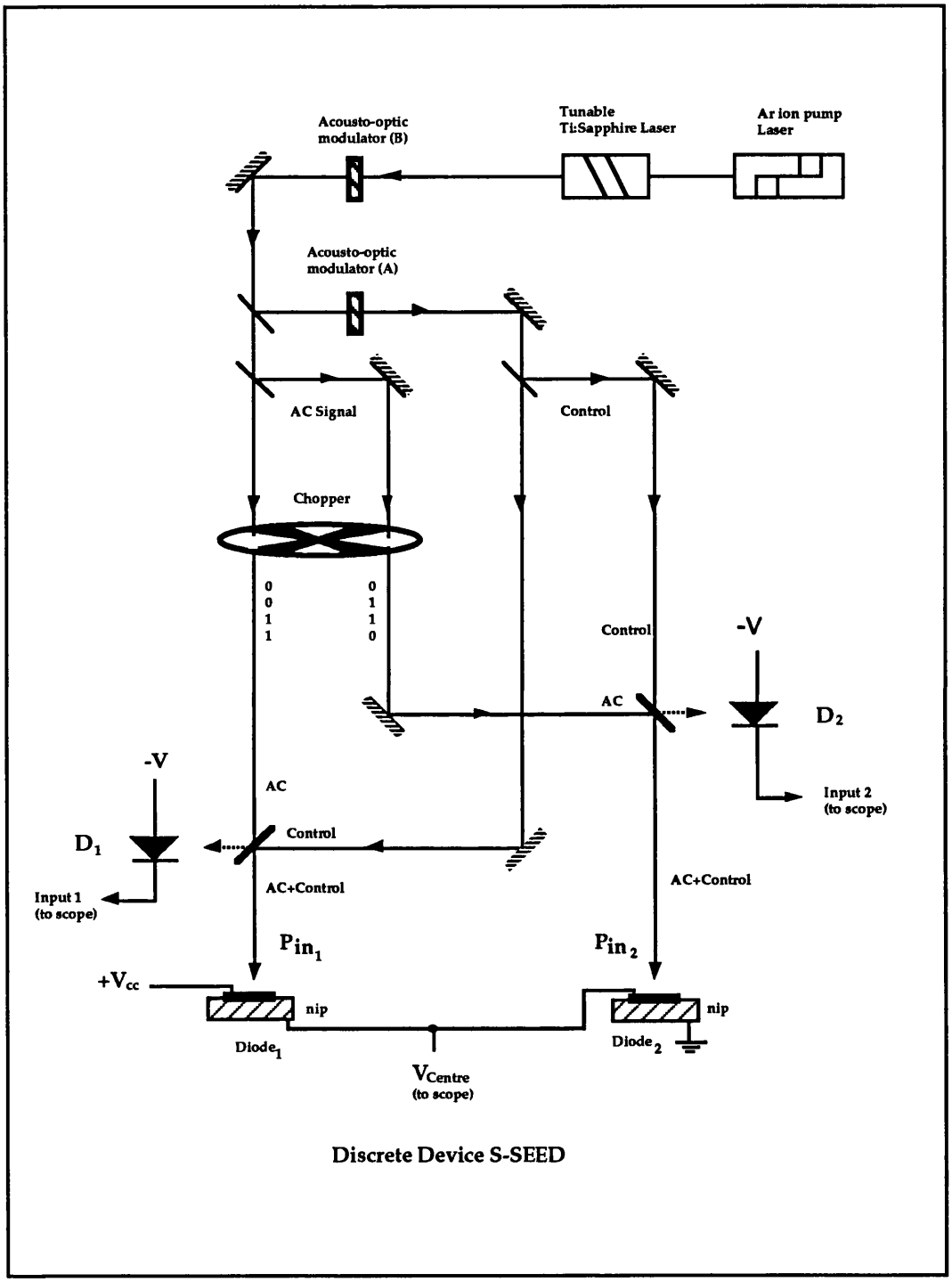


Figure 4.2.6 Experimental set-up

4.2.4 Results and validation of theory

The S-SEED was supplied with a reverse bias of V_{cc}=2.0 volts. Upon application of two constant power input beams, the S-SEED remained in either of two states, V_{centre}= 2.5 volts or - 0.8 volts. The S-SEED exhibited the expected bistable behaviour and it was observed that if either of the two beams were momentarily removed or broken, then the S-SEED would switch its point of operation to the corresponding stable state and remain in that state when both input beams were reinstated. The S-SEED was bistable for a wide range of supply voltages greater than 0 volts. However, the value of V_{cc} was chosen such that upon switching, the MQW diodes making up the S-SEED would experience the voltage swing which yielded the largest possible change in their respective absorption of incident light. V_{centre} can be greater than V_{cc}, because in the latched state, the PIN diodes' built in voltages, V_d, act to reinforce V_{cc}. Upon switching to either of the stable states, one of the diodes experiences a reverse bias of approximately $V_{cc}+V_d$, whilst the other experiences a small forward bias, $-V_d$. Intersection of the S-SEED operating curves occurs at a voltage greater than V_{cc} and less then zero because the photocurrent/internal quantum efficiency of the individual MQW diodes only falls off after the very significant built-in field, for these relatively thin devices, is counteracted: Operating points a and b in figure 4.2.1b. The magnitude of the constant power inputs was varied and it was verified that the required input contrast ratio C, was the same as expected from the previous theory (4.2.1), (ie. it was noted that $C \approx A_{max}/A_{min} \approx 1.8$, $P_2=CP_{bias}$ and $P_1 = C^{-1}P_{bias}$). The difference in optical powers required to switch the S-SEED was measured directly by observing the difference in magnitudes of the two photocurrents flowing through the two R-SEEDs, converted from the S-SEED, just after switching had taken place.

The two AC digital signal beams were used as inputs to the S-SEED. The AC signals were designed to input to the S-SEED a repeating sequence of all the possible combinations of 1 and 0; ie. 00, 01, 11 and 10 etc. For the input combination $diode_1$=1 and $diode_2$=0 (ie. 10), the S-SEED switched to stable state $V_{centre}\approx$2.5 volts (point **a**, figure 4.2.1b). For input combination 01, the S-SEED switched to the stable state, V_{centre}= -0.8 volts (point **d**, figure 4.2.1b). For the 11 input combinations, the S-SEED remained latched in its previous state at a voltage slightly less than 2.5 volts for the high state and slightly greater than -0.8 volts in the low state. This was because the S-SEED is now operating in its bistable region and the operating points a and b are quite high on the operating curves (figure 4.2.1b). For optimum performance the voltage difference between points a and b should be the same as the desired voltage swing for the maximum change in device absorption upon switching, thereby maximising the extent to which one input is suppressed (or reflected) with respect to the other. Therefore, for the repeating sequence of 01 and 10 input combinations, the S-SEED switched its operating point correspondingly, remaining latched for the intervals 00 and 11. It was noticed that for AC input

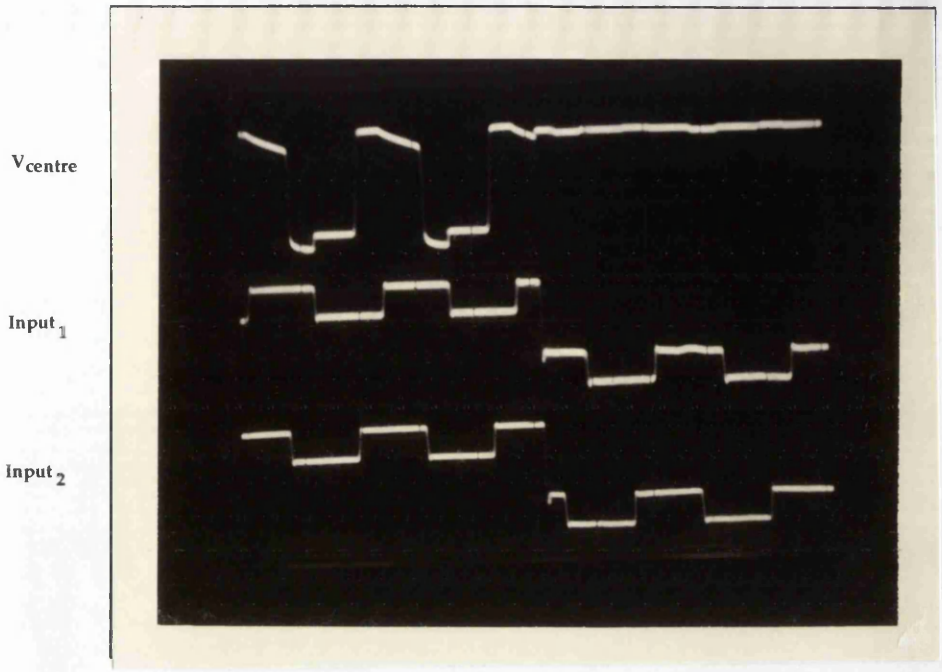
combination 00, when no light is incident on either input of the S-SEED, the S-SEED diodes slowly discharges because of their dioide's respective leakage currents. The time taken for this discharging however, was large compared to the input signal data rate and so had little effect on the expected device behaviour.

As expected, upon application of the control bias signals, the S-SEED remained latched in the state prior to the application of the control bias powers. This was observed by taking a photograph of the oscilloscope screen showing the two input signal channels and V_{centre} (indicating the current state of the S-SEED). The oscilloscope was single-shot triggered by the blanking input to the acousto-optic modulator. When the control signals are applied to the S-SEED, the oscilloscope triggered once, exposing a photographic film which allows the interdependence of the inputs and control signals on device behaviour to be assessed. Figure 4.2.7 shows the two AC modulated input signals, $input_1$ and $input_2$, detected by D_1 and D_2, and their effect on V_{centre}, which shows the state of the S-SEED at a given time. It is seen that for input combination 01, the S-SEED switches to the stable state, V_{centre}= -0.8 volts and for the input combination 10, V_{centre}= 2.5 volts. For the state 00, the centre voltage decays slightly due to the dark currents of the two diodes. However because this decay is slow, it has little effect on the S-SEED's performance. Just prior to the application of the control bias signals to the S-SEED inputs, the input state is 00, the S-SEED thus remains in its previous state for 10, $V_{centre}\approx$2.5 volts. It can be seen that when the control bias offset is applied to the two inputs, the S-SEED remains latched in its present state ($V_{centre}\approx$2.5 volts), regardless of the combination of the AC signals present, xx (where x=don't care) at its input. The S-SEED then remains latched for the remainder of the following data signal, in S-SEED non-switching format, passively relating (to varying degrees) its inputs to its outputs. This effectively demonstrates S-SEED latching on the MSB difference of two optical packet headers.

With no light incident on the S-SEED, V_{centre} was found to be equal to zero volts, presumably because of unequal leakage currents in the two devices. Two 470kΩ resistors in series, were placed in parallel with the S-SEED, with the centre voltage between the two resistances tied to the centre voltage, V_{centre} of the S-SEED. The resistive values were chosen to be low compared to the reverse bias impedance of the S-SEED under zero illumination and high relative to the impedance of the illuminated S-SEED. This anchored V_{centre} to $V_{cc}/2$ when no light was incident on the S-SEED. Under illuminated conditions, the resistors in parallel had no discernible effect on device behavior. When the acousto-optic modulator transmitted, optical signals in S-SEED non-switching format were made incident on the S-SEED. Depending on the time at which the signals are applied to the S-SEED, relative to the input data signals, ie. whether the first bits input are 01 or 10, the S-SEED latches to either of its stable states and remains latched in that state. When the incident light is removed, ie. once the optical packet has been transmitted, the S-SEED returns to its 'middle' state, $V_{centre}\approx V_{cc}/2$. This can be

observed in figure 4.2.8. Initially the S-SEED is latched in the state $V_{centre} \approx 0$ and continues to remain so regardless of the combination of 1's and 0's at its inputs. When the optical power is removed, the centre voltage of the S-SEED returns to $V_{cc}/2$, as the respective leakage currents of the two diodes act to equalise the voltages across themselves, (aided by the series resistances in parallel). When the optical signals in S-SEED non-switching format are restored, the first signal inputs can be seen to be 10, therefore the S-SEED latches to $V_{centre} \approx V_{cc}$. When the optical power is subsequently removed and restored, the S-SEED can be seen to latch to $V_{centre} \approx 0$, due to the fact that the first bit difference input was 01, as can be observed in the photograph. This demonstrates the principle of routeing the optical cell according to the first bit difference of the two cell headers, as required by the Banyan routeing algorithm. It should be noted again that when the first incident bits are different, 10 or 01, the S-SEED must latch more quickly than one bit interval. However when the first incident bits are either 00 or 11, the incident signals must be sufficiently similar so as not to cause latching *until* their first bit difference. The tolerance in the degree of similarity of the 00 and 11 signals is relaxed at high data speeds, however for the relatively low data rates (~1 kbit/s) used in this experiment, any difference in optical powers was very significant, since the S-SEED latching time was fast, compared to the bit-interval of the signal data. Figure 4.2.9 shows that upon restoration of the two optical input signals to the S-SEED, the centre voltage V_{centre} starts to switch to low. This is because even though the first bits incident are both 1's, their difference is sufficient at these low bit-rates to start to cause latching. It is for this reason that the power levels of the 00 and 11 input signal combinations should be similar enough so as not to cause switching in one bit interval and for input combinations 01 and 10 to be sufficiently disimilar so as to latch more quickly than one bit interval. When the input signals change to 10, the S-SEED switches to V_{centre}=high within the bit interval and subsequently remains latched. Latching on the first *bit difference* of the two signals is therefore demonstrated.

Using the S-SEED in this way, ie. latching on the most significant bit or the first significant bit difference of two input signals, the behavior of the S-SEED is both stable and repeatable. By adjusting the frequency of the acousto-optic modulator's blanking input, the phase of the control bias signal to the S-SEED inputs could be selected so that it was possible to select regular and repeating latching of the S-SEED in either direction. For example, it was possible to simulate optical packet switching for cells latching the S-SEED in either direction either continuosly, or pseudo-randomly. Due to the relatively wide hysteresis width of the S-SEED for a given optical power intensity, the system was very stable and noise in the optical signals used was insufficient to cause any deviation from the expected system behaviour.



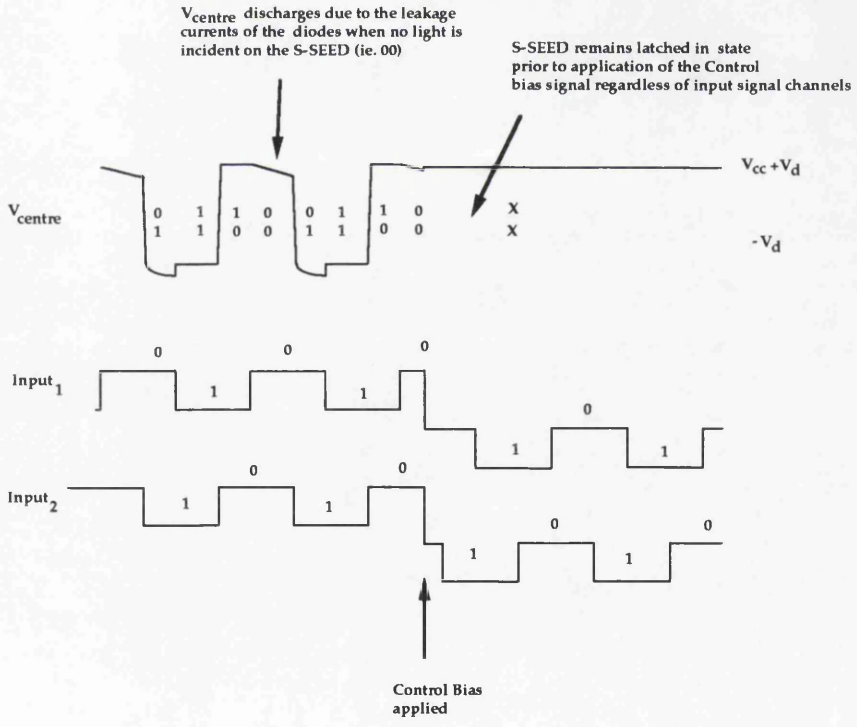
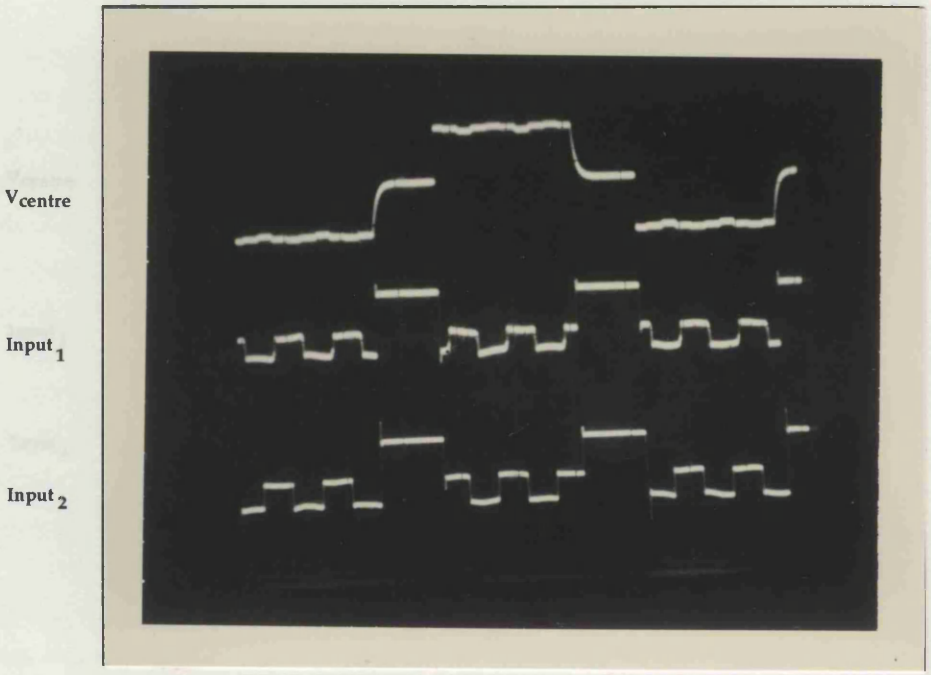


Figure 4.2.7 S-SEED: Switching on the Most significant bit difference of two data streams



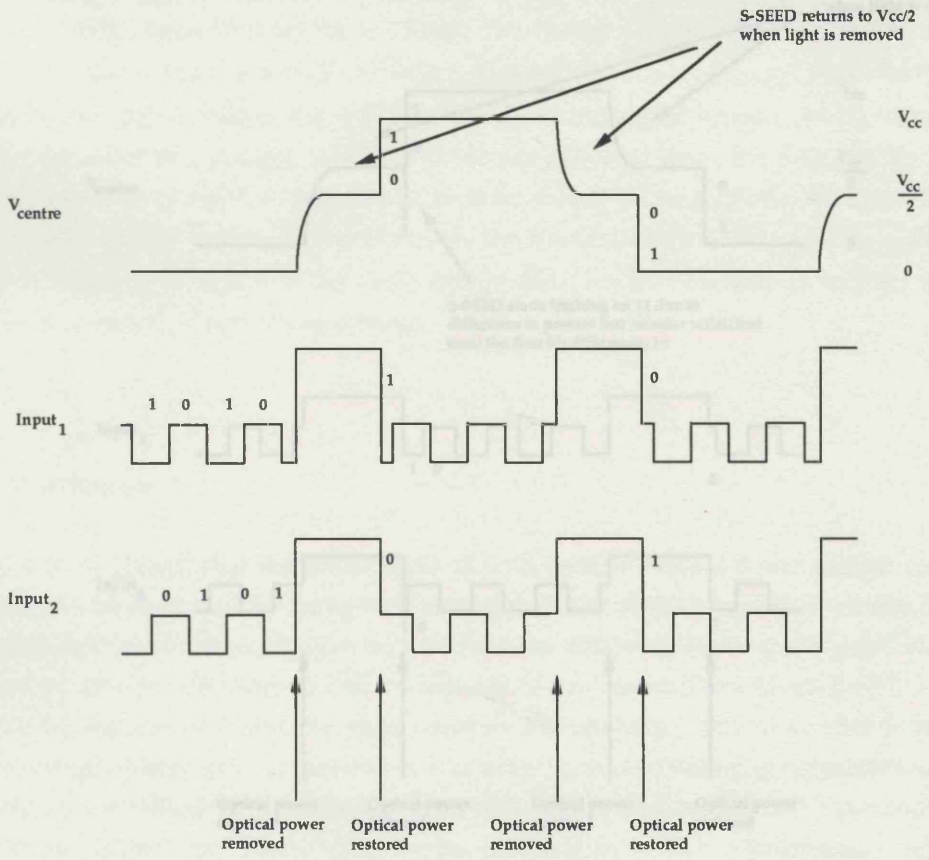


Figure 4.2.8 S-SEED: Switching on first bit difference of two data streams

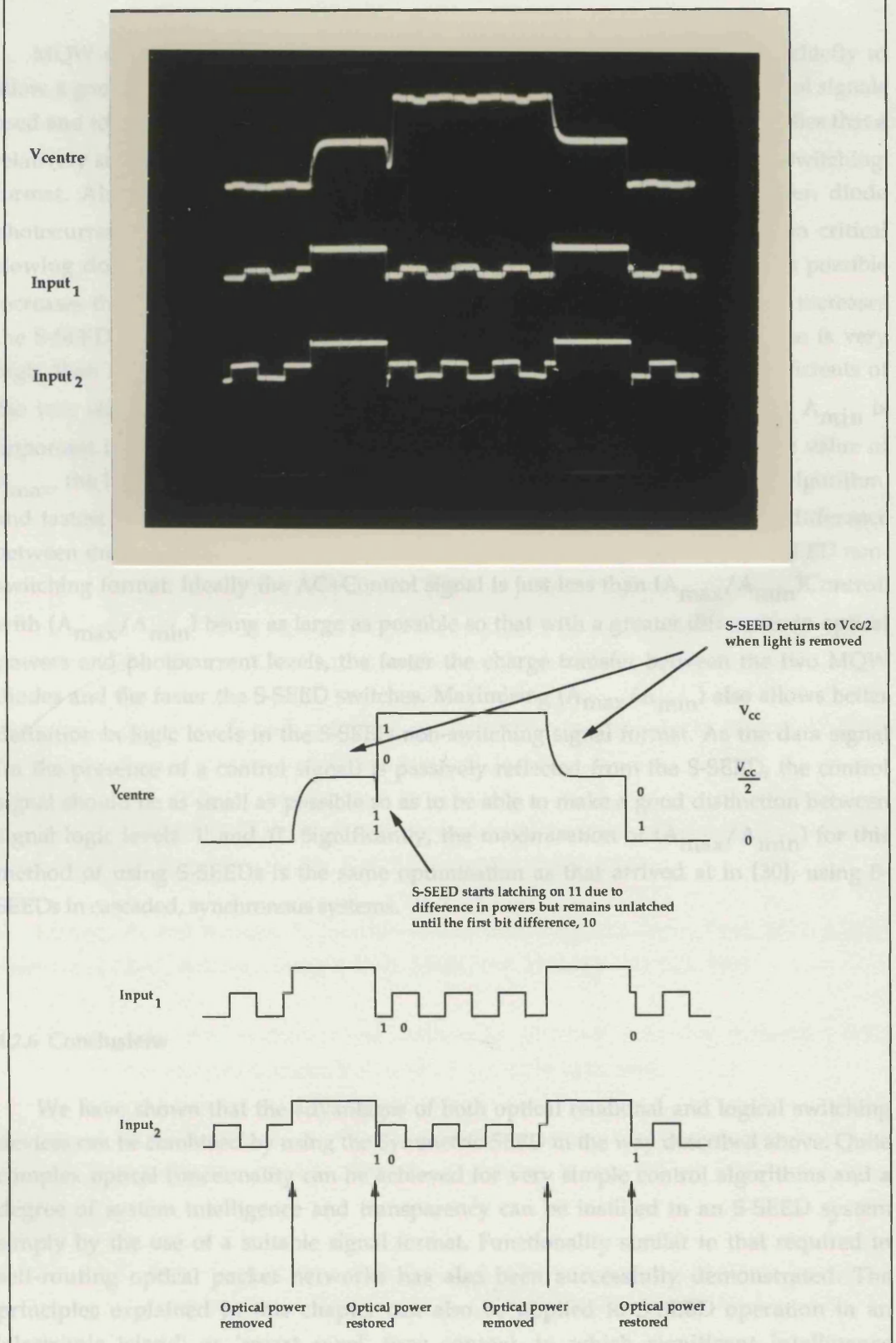


Figure 4.2.9 S-SEED: Switching on first bit difference of two data streams

4.2.5 Device and switch optimisation

MQW device optimisations applicable to this way of using S-SEEDs are chiefly to allow a good degree of tolerance in the relative magnitudes of the AC and control signals used and to keep switching times to a minimum. Maximising (A_{max}/A_{min}) implies that a relatively small control bias is required to convert the signal into 'S-SEED non-switching' format. Also, maximising (A_{max}/A_{min}) means that the separation between diode photocurrents upon switching is greater. Thus after taking into consideration critical slowing down, switching times will be faster (5.2). Making A_{max} as large as possible increases the device maximum responsivity for a given optical power and also increases the S-SEED switching contrast ratio. (If device absorption in the low bias case is very high, then reflection is very low ($R_{min}\approx 0$) and the ratio of the reflection coefficients of the two stable states (ie. the contrast ratio) is high). Having low values of A_{min} is important in reducing the insertion loss of the S-SEED because the greater the value of R_{max}, the less lossy is a system of cascaded S-SEEDs. For the Banyan routeing algorithm, and fastest possible latching on the first bit difference, it is required that the difference between the two signals 10 or 01 is as large as possible but still remaining in S-SEED non-switching format. Ideally the AC+Control signal is just less than (A_{max}/A_{min})Control, with (A_{max}/A_{min}) being as large as possible so that with a greater difference in optical powers and photocurrent levels, the faster the charge transfer between the two MQW diodes and the faster the S-SEED switches. Maximising (A_{max}/A_{min}) also allows better definition in logic levels in the S-SEED non-switching signal format. As the data signal (in the presence of a control signal) is passively reflected from the S-SEED, the control signal should be as small as possible so as to be able to make a good distinction between signal logic levels '1' and '0'. Significantly, the maximisation of (A_{max}/A_{min}) for this method of using S-SEEDs is the same optimisation as that arrived at in [30], using S-SEEDs in cascaded, synchronous systems.

4.2.6 Conclusions

We have shown that the advantages of both optical relational and logical switching devices can be combined by using the Symmetric-SEED in the way described above. Quite complex optical functionality can be achieved for very simple control algorithms and a degree of system intelligence and transparency can be instilled in an S-SEED system simply by the use of a suitable signal format. Functionality similar to that required in self-routing optical packet networks has also been successfully demonstrated. The principles explained in this chapter can also be applied to S-SEED operation in an 'electronic island' or 'smart pixel' type context, in which significant intelligence (additional to that obtainable from the electronic processing) can be obtained through the use of this type of simple optical control algorithm [31]. For this particular application, there is a case for arguing that if the logic operation is simple enough then it may be worth doing all-optically, rather than using electronics. This is especially true

for the case when the system performance is limited by the input-output capability rather than the processing ability of the system. The self-routeing S-SEED functionality demonstrated however is only in a single switching device. The issues involved in cascading these devices are far from trivial. However the demonstration is useful in that it shows single stage functionality and again shows the quite sophisticated, added benefits that optical technology can bring to systems design.

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CHAPTER 5

SEED systems, applications and optimisations

The Quantum Confined Stark Effect (QCSE), ie. the change in optical absorption which accompanies a change in the electric field applied perpendicular to thin quantum well layers, has been demonstrated in a number of material systems. These include: GaAs-AlGaAs [1], InGaAs-InP [2], InGaAsP-InP [3], GaSb-AlGaAs [4], InAsP-InP [5] and InP-InAs [6]. To date the best SEEDs have been made using GaAs-AlGaAs materials, however improved devices for enhanced system performance may be fabricated using different materials and quantum well structures, eg. coupled quantum wells [7] or asymmetric wells [8]. What however is the improvement that can be achieved by the use of these different structures and material systems? The state of current SEED technology is such that a wide range of SEEDs can be fabricated with very finely tuned device characteristics. This leads to the question of how we choose the best quantum well designs for using SEEDs in high-performance systems applications? - This chapter deals with some of the issues, optimisations and trade-offs in this design process.

5.1 SEED systems

A number of systems applications using SEED devices have already been addressed in the preceding chapters. Chapter 3 described the SEED optical 'tap'/self-linearised modulator [9] whose absorption, and hence reflection of an incident optical signal is linearly proportional to an external biasing current. A serial-to-parallel convertor type configuration was also proposed which exhibited quite sophisticated functionality for a very simple design. Optimisations for using SEEDs in this manner are the maximisation of the ratio of maximum to minimum absorption (A_{max}/A_{min}) of the SEED to allow the largest possible dynamic power range of linear modulation. Also, increasing the maximum reflectivity (R_{max}) of the device low-absorption state, so that the optical signal is not significantly attenuated as it is cascaded through the system is desirable (ie. low insertion loss). Having the largest possible value for A_{max}, also gives very efficient photodetection and a flat input/output response at low incident optical power levels. Chapter 4 of this thesis describes a new way of using S-SEEDs which can yield functionality similar to that required in a distributed-control, self-routing, optical packet switch [10]. Maximising (A_{max}/A_{min}), increases the width of the S-SEED bistable hysteresis curve, therefore making the required input switching contrast ratio of the S-SEED high, ensuring system immunity to noise, fluctuations in the power supply and allowing wide tolerances for the control and input signals used. Setting A_{max} as large as possible gives high contrast switching as for the case when $A_{max} \approx 100\%$, an infinite

switching contrast ratio is effectively achieved, since no light is reflected from the device in the 'off' state. An high switching contrast is useful in cascaded switching systems in which a large number of device outputs are summed onto a single input and also high contrast switching is useful in telecommunications applications where a high extinction ratio is required between two signal channels [11]. Thus for the S-SEED systems previously discussed in this thesis, the obvious device optimisations (aside from speed considerations which are addressed later), are low insertion loss (low A_{min}), for system cascadability and very high values of A_{max}, for high contrast switching and high extinction ratios. Less obviously, the maximisation of the ratio of the maximum to minimum device absorption (A_{max}/A_{min}), is a recurring theme in the optimisation of optical logic systems using SEEDs.

Current optical computing systems demonstrated by AT&T Bell Laboratories, based on the use of S-SEEDs are made up of at least two stages of cascaded S-SEED flip-flops or S-SEED logic gates. These devices are operated in a time-sequential manner with initially low power signal data beam inputs setting the state of the S-SEED. Subsequently, higher power clock beams are used to 'read out' the state of the device. The higher power outputs are then passed on as the inputs to the next stage in the cascade. This is known as time-sequential gain, since the output signals are greater than the input signals that originally set the state of the device. For this way of using S-SEEDs, the insertion loss is not a critical parameter, since at each stage in the cascade, the optical signal is regenerated by the clock signals. If the output beams are derived from the same source, then the state of the device is insensitive to fluctuations in the optical power supply. The time-sequential mode of operation also has the advantage of effective input/output isolation because small reflections of the output beams back into the device will not cause the device to change states. Also, since the signal inputs and outputs are differential in nature, then specific operating power levels need not be defined and device operation is possible over many decades power range.

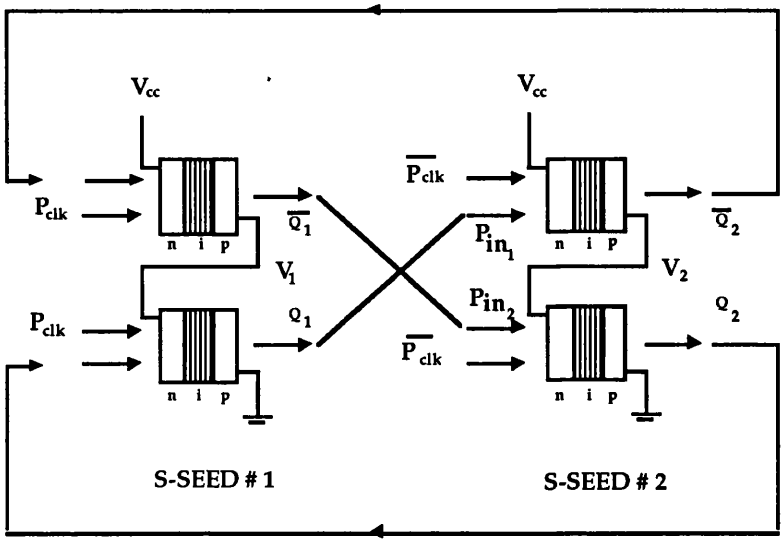

Figure 5.1a S-SEED photonic ring counter

There are several ways of performing optical logic operations using S-SEEDs. These include: differential logic with preset beams and/or output attenuators [12-13], differential M-state logic [14], single-ended and differential logic using electrically interconnected quantum well diodes [15] and differential logic using sense amplification [16]. S-SEEDs can be cascaded to perform a wide variety of optical logic functions and systems applications, eg. multiplexers, demultiplexers, shift registers [17] and all-optical switching networks [18]. Two typical S-SEED logic systems are shown in figures 5.1a and 5.1b: Figure 5.1a shows an S-SEED photonic ring counter in which the outputs from the first S-SEED are crossed over and fed into the inputs of the 2nd S-SEED, whose outputs are then used as the inputs to the first S-SEED. With each successive clock cycle, each flip-flop output and therefore input, toggles between a logic 1 and a logic 0 [19]. Figure 5.1b shows an S-SEED cascaded logic gate in which the state of the 2nd stage S-SEED is set using a preset pulse at one of its inputs and whose output state only changes for certain combinations of its inputs. Both NAND and NOR logic operations can be made by pre-setting the 2nd stage S-SEED to either of the two possible stable states [20]. For ease of understanding, both the S-SEED configurations of figure 5.1 have been drawn showing transmissive SEEDs. The same architectures however, apply to reflective SEEDs. Thus various system architectures can be built up by simply cascading S-SEED logic gates to perform logical functions with arbitrary complexity. The speed at which these logic operations can be performed using the S-SEED in this manner, (alongside the advantages that parallel optical communication links brings to the equation), is key in deciding whether these devices will be useful in real systems applications. The following section will address the 'ideal' SEED device characteristics for possible use in high bit-rate and highly signal tolerant processing systems.

5.2 S-SEED speed considerations - The 'ideal' SEED

The speed of S-SEED switching and hence the 'system bit-rate' is limited by the time it takes the photocurrents of the S-SEED to charge up the capacitances of its constituent devices. The switching time is therefore inversely proportional to the difference in the input optical powers to the S-SEED and hence its photocurrents (2.3.4). The system bit-rate can therefore be calculated by determining the absolute powers from the outputs of the first stage of the system cascade, which are inputted to the second stage of devices.

The first step in calculating the system bit-rate for the S-SEEDs operating in the types of configurations shown in figures 5.1a and 5.1b, is to calculate the optical power incident on the 2nd device stage. These powers are related to the optical reflection, R, or transmission of the 1st stage of SEED devices, the fan-out of the 1st stage S-SEEDs and the optical losses incurred in passing the light beams between the two stages of devices [21].

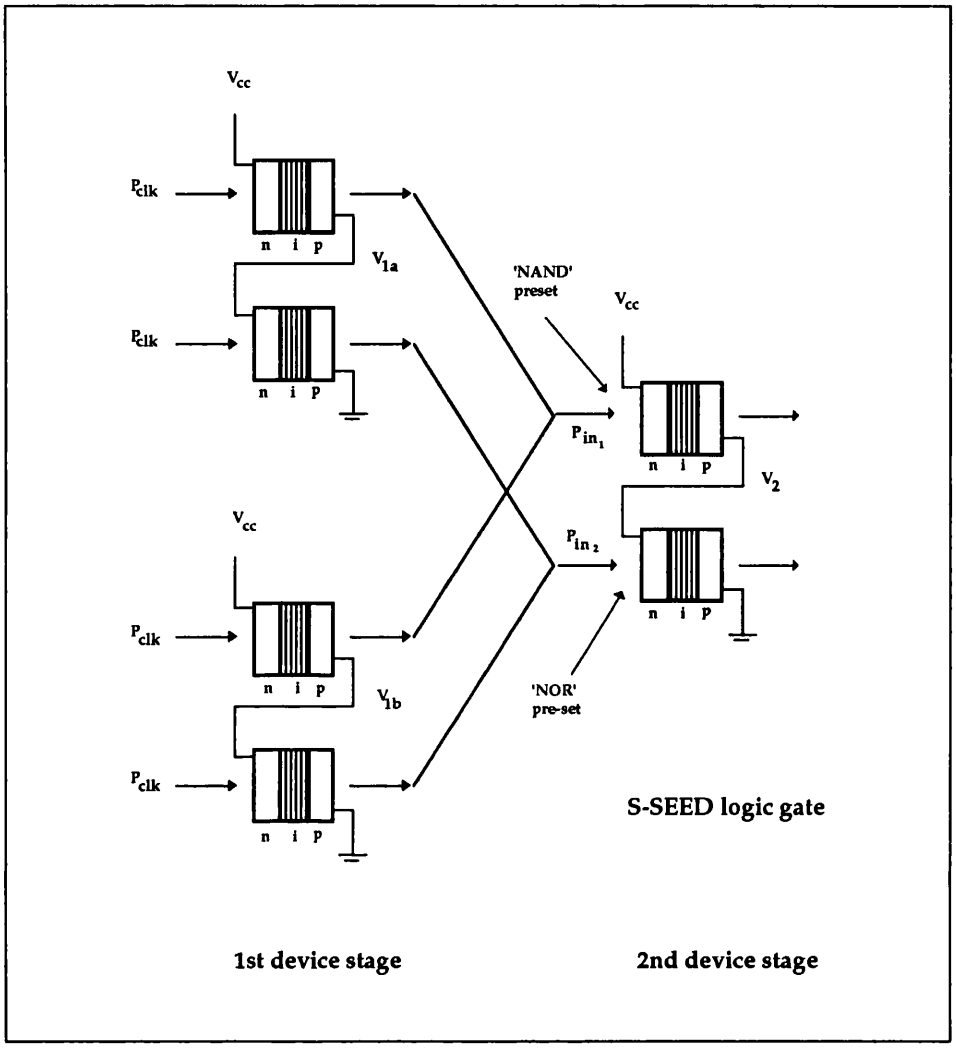

Figure 5.1b Cascaded S-SEED differential logic gates

The input optical powers to the 2nd stage S-SEED are given by:

$$P_{in_1}(t) = P_{clk}(t)\, R\,[V_1(t)]\, T_{opt}\, Fan_{in}/Fan_{out}$$

and

$$P_{in_2}(t) = P_{clk}(t)\, R\,[V_{cc} - V_1(t)]\, T_{opt}\, Fan_{in}/Fan_{out}$$

Where $R\,[V_1(t)]$ and $R\,[V_{cc} - V_1(t)]$ are the optical reflectivities/transmivities from the quantum well diodes in the 1st S-SEED stage at their respective voltages, $V_1(t)$ and V_{cc}-$V_1(t)$, P_{clk} is the optical power in each of the clock beams, Fan_{in} is the Fan-in of the 2nd stage of devices (either 1 for the photonic ring counter or 2 for the logic gates), Fan_{out}

is the fan-out of the first stage of devices and T_{opt} is the transmission of the interconnecting optics. If we assume that the first stage of S-SEEDs have fully switched then the reflection from these devices corresponds to a maximum and minimum, R_{max} and R_{min}, at voltages approximately equal to V_{cc} and 0 across each of the MQW diodes respectively. The optical powers incident on the 2nd stage of S-SEEDs can therefore be readily calculated.

Switching time of the 2nd stage S-SEED can be calculated using Kirchoff's current law to solve in this case $V_2(t)$, the centre voltage of the 2nd stage S-SEED, as a function of time, for the incident optical powers, P_{in_1} and P_{in_2}.

$$C_{tot} \frac{dV_2(t)}{dt} = S\,[V_{cc} - V_2(t)]\,P_{in_2}(t) - S\,[V_2(t)]\,P_{in_1}(t) = \Delta i(t) \qquad \text{(equation 5.1)}$$

Where $\Delta i(t)$ is the difference in the respective device photocurrents ($i_1(t) - i_2(t)$) of the 2nd stage S-SEED, S [V] is the responsivity (photocurrent/incident power [A/W]) of each diode in the S-SEED for a given voltage, $V_2(t)$ or V_{cc}-$V_2(t)$ and C_{tot} is the total capacitance of the 2nd stage S-SEED.

Equation 5.1 is of the form: $$C_{tot} \frac{dV_2(t)}{dt} = \Delta i\,[V_2(t)]$$

To calculate the switching time of the S-SEED, the voltage change going from one state to another (V_2: 0 to V_{cc} or V_2: V_{cc} to 0), can be divided up into small steps, ∂V, for which the current is approximately equal (figure 5.2). We can then calculate the switching time ∂t in each interval [21].

$$\partial t = C_{tot} \frac{\partial V}{\Delta i(V_2)}$$

multiplying top and bottom by $\partial V(t)$ gives:

$$\partial t = C_{tot} \frac{\partial V}{\Delta i(V_2)} \cdot \frac{\partial V}{\partial V} = C_{tot} \frac{(\partial V)^2}{P(\partial t, \partial V)}$$

where $P(\partial t, \partial V)$ is the rate of transfer of energy or the electrical power $\Delta i(V_2)\partial V$ required for a ∂V change in device capacitance voltage $V_2(t)$, in a time interval, ∂t.

Summing ∂t over the entire switching voltage swing, $\Delta V = V_{cc}$ [21], effectively integrates equation 5.1 and gives an S-SEED switching time, Δt:

$$\Delta t = \sum_{V_2=0\ \text{(state 2)}}^{V_2=V_{cc}\ \text{(state 1)}} \partial t = \frac{C_{tot} V_{cc}^2}{P(\Delta t,\ \Delta V)} \qquad \text{(equation 5.2)}$$

Where $P(\Delta t, \Delta V)$ is the electrical power transferred upon switching from one stable state to the other, and is equal to the shaded areas between the two S-SEED loadline curves, i_1 and i_2 (figure 5.2). Therefore increasing the area between the two curves, by maximising the separation between the two photocurrents on switching, maximises the speed at which charge is transferred in changing the state of the S-SEED, thereby consequently decreasing the switching time, Δt.

The electrical energy transferred on switching is equal to the electrical power, $P(\Delta t, \Delta V)$ multiplied by the switching time, Δt.

Electrical switching energy, $E_{elec} = P(\Delta t, \Delta V)\Delta t = C_{tot}V_{cc}^{2}$

It is already known that by increasing the difference between the photocurrents i_1 and i_2, by inputting input optical powers which are as different as possible, reduces the S-SEED switching time, Δt (2.3.4). However, for given fixed input power levels, what are the device characteristics that give optimum S-SEED switching speeds?

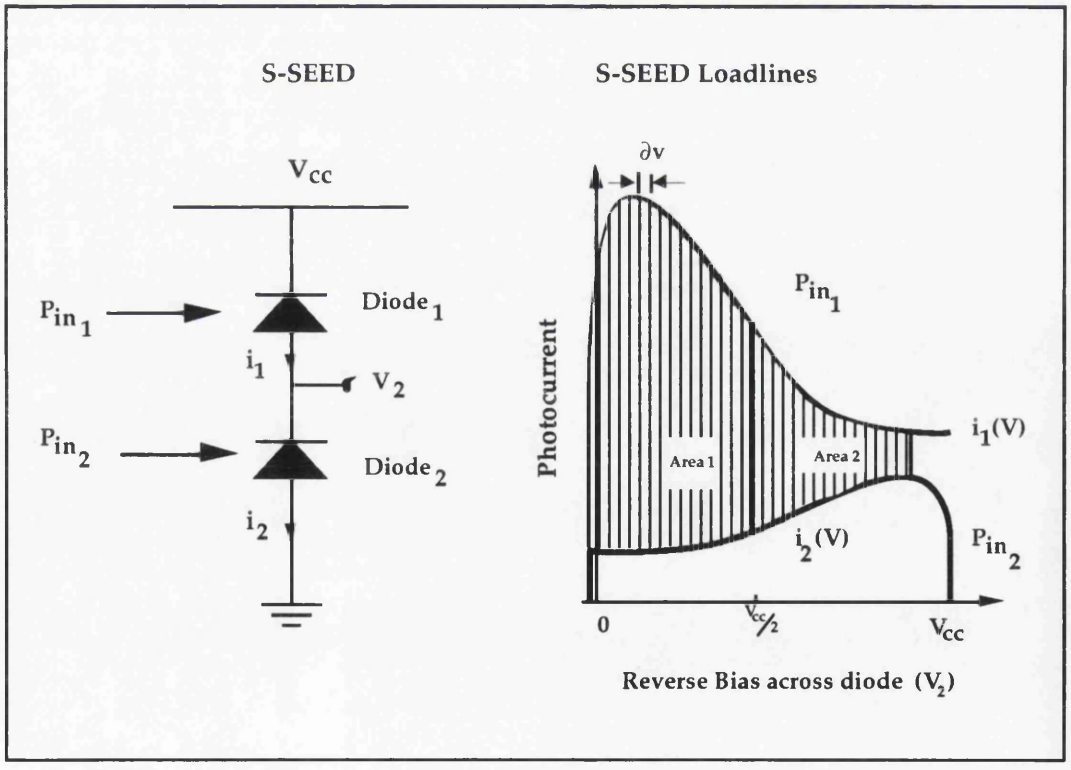

Figure 5.2 S-SEED loadline and power transfer characteristic

The S-SEED can be switched by optically creating a charge $Q = C_{tot}V_{cc}$ to switch the S-SEED from the high-voltage to low-voltage state, discharging one of the diodes and charging the other. This requires an absorbed optical switching energy:

Optical switching energy, $E_{opt} = \frac{hc}{e\lambda} C_{tot} V_{cc}$

Where C_{tot} is the total S-SEED capacitance, V_{cc} is the S-SEED supply voltage, e is the individual electronic charge. {This equation makes the assumption that the device exhibits unity quantum efficiency, (ie. one electron is collected at the device terminals for each photon absorbed)}. In a real device however, the absorbed optical energy will vary as some (large) fraction of the total incident energy, so this energy sets the scale of optical switching energies. In switching with slowly varying powers, the optical switching energy can be defined as the product of the difference between the incident optical powers, ($\Delta P = P_{in_1} - P_{in_2}$) and the switching time, Δt: $E = \Delta P \Delta t$. This resulting energy is still approximately equal to E_{opt} although it can be several times larger depending on the actual device absorption characteristics. In general, E_{opt} is comparable with or smaller than the electrical switching energy, E_{elec}. On switching there is a partial cancellation of the two charging and discharging photocurrents i_1 and i_2, which acts to increase the total electrical energy required, with respect to the ideal value of the optical power required for switching, E_{opt}. Also on switching, device absorption changes from a high to low or low to high value so that the effective device absorption on switching is less than the maximum, therefore more optical power is required to switch the S-SEED in a given switching time.

$$E_{opt} \approx E_{elec} \approx C_{tot} V_{cc}^2$$

The maximisation of the electrical power transferred on S-SEED switching, for a given pair of input powers, P_{in_1} and P_{in_2}, is achieved by maximising the power area between the two curves i_1 and i_2 (figure 5.2).

For S-SEEDs and MQW modulators as a whole, the fraction of the transmitted or reflected optical power, R, can be approximated by (1 - Absorption, A). {For reflection devices and resonant devices there can be both a reflected and transmitted component. For non-resonant devices however, this is an accurate description of device behaviour and for resonant devices is correct to a first approximation}. The maximum reflection, R_{max} of an input power corresponds to (1 - the minimum absorption, A_{min}) and the minimum reflection of an input optical power, R_{min} corresponds to (1 - the maximum absorption, A_{max}). Therefore for the case when the 1st stage S-SEED is fully latched in the stable state $V_1 \approx 0$, and the clock beams with power P_{clk}, read out the state of the device, then the P_{in_1} input to the 2nd stage S-SEED is a maximum, $P_{clk}(1-A_{min})$ and the P_{in_2} input to the 2nd stage S-SEED is a minimum, $P_{clk}(1-A_{max})$.

The optical input powers to the 2nd stage S-SEED are therefore, $P_{in_1} = P_{clk}(1-A_{min})$ and $P_{in_2} = P_{clk}(1-A_{max})$, respectively. Knowing the input optical powers, P_{in_1} and P_{in_2} and the 2nd device stage responsivity characteristics, the photocurrents i_1 and i_2 which act to switch the state of the S-SEED can be calculated.

The responsivity characteristics of each of the two 2nd stage S-SEED diodes shown in figures 5.1a and 5.1b, can be approximated by a curve which goes from a value corresponding to maximum absorption, A_{max} at V_2=0 volts for $diode_1$ (V_2=V_{cc}: $diode_2$), to a minimum value, corresponding to a minimum absorption, A_{min} at V_2= V_{cc} for $diode_1$ (V_2=0 for $diode_2$), with the fall off in responsivity with voltage being approximately linear. The photocurrents, i_1 and i_2 generated, can be found at any voltage V=V_2 (V_2: 0 to V_{cc}), by multiplying the relevant incident optical power P_{in_x}, by the corresponding device responsivity [A/W].

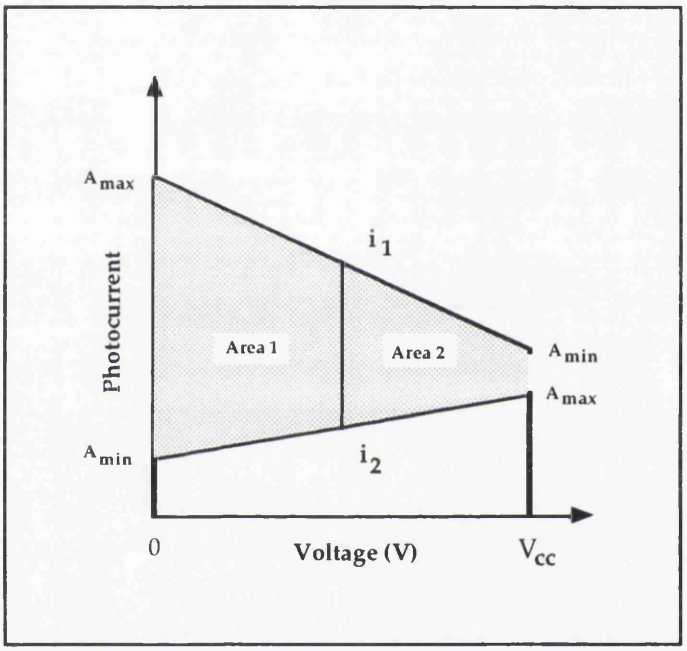

Figure 5.3 Responsivity approximation of an S-SEED

If we initially assume that the inputs to the 2nd stage S-SEED corresponds to P_{in_1} equal to a maximum $P_{clk}(1-A_{min})$ and P_{in_2} a minimum, $P_{clk}(1-A_{max})$, then the photocurrents at any voltage, V_2 can be calculated as follows:

$$i_1(v) = \frac{e\lambda}{hc} P_{clk} (1-A_{min})(A_{max} - \Delta A\frac{V}{V_{cc}})$$

$$i_2(v) = \frac{e\lambda}{hc} P_{clk} (1-A_{max})(A_{min} + \Delta A\frac{V}{V_{cc}})$$

Where $\Delta A = A_{max} - A_{min}$

The area between the two curves i_1 and i_2, corresponds to a Power, $P = \int_0^{Vcc} (i_1 - i_2)\, dV$

$$= P_{clk} \frac{e\lambda}{hc} \int_0^{Vcc} \left[A_{max} - A_{min} + \left(A^2_{max} - A^2_{min} - 2A_{max} + 2A_{min} \right) \frac{V}{V_{cc}} \right] dV$$

$$= P_{clk} \frac{e\lambda}{hc} \left[(A_{max} - A_{min})V + \left(A^2_{max} - A^2_{min} - 2A_{max} + 2A_{min} \right) \frac{V^2}{2V_{cc}} \right]_0^{Vcc}$$

$$= P_{clk} \frac{e\lambda}{hc} \left[\left(A^2_{max} - A^2_{min} \right) \frac{V_{cc}}{2} \right] \qquad \text{(equation 5.3)}$$

It is seen that increasing the clock power, P_{clk}, increases the electrical power, P transferred and hence reduces the switching time, Δt (equation 5.2). However for a fixed clock power, the area between the curves $i_1(V)$ and $i_2(V)$, and hence the transmitted electrical power, is a maximum for the case when $A_{max}=1$ and $A_{min}=0$. This corresponds to the case when the reflected optical power from the 1st stage S-SEED and received by the 2nd stage S-SEED is 100% and 0% for the high and low states respectively and with 100% of the light incident on the 2nd stage being absorbed regardless of which state the second devices are in. Therefore for $A_{max}=1$ and $A_{min}=0$, the switching time, Δt of the S-SEED is at its smallest. In reality however, this can only be achieved by using separate detectors for the signal beams and modulators for the control beams for the 2nd stage of S-SEEDs since the detectors would have to absorb all of the light incident on them regardless of voltage. In practice however the same S-SEED devices are used as both detectors and modulators. If there is insufficient absorption in the high-reflection state however, then there will be very little photocurrent generated when it is tried to change the state of the device and thus the device takes a much longer time to switch in the opposite direction. There is therefore a balance between the minimum absorbed power and the maximum transmitted power that will give the optimum switching speed in a system. This can be observed in figure 5.2: It can be seen that the power area under the curves, between V_2: 0 to $V_{cc}/2$ (area 1) is significantly greater than the power area between V_2: $V_{cc}/2$ to V_{cc} (area 2). Therefore the time taken for the S-SEED to go from $V_2=V_{cc}$ to $V_{cc}/2$ (area 2), will be significantly longer than that required to go from V_2: $V_{cc}/2$ to 0 volts (area 1). When the minimum device absorption A_{min} is further decreased. This imbalance becomes greater and the time taken for switching from $V_2=V_{cc}$ to $V_{cc}/2$ becomes the main contributor to the total switching time, Δt.

By dividing the switching time into two components $\Delta t = \Delta t_1 + \Delta t_2$, which correspond to the times taken for the S-SEED to change its centre voltage V_2 from 0 to $V_{cc}/2$, (Δt_1),

and from $V_{cc}/2$ to 0, (Δt_2), respectively, the optimum values of A_{min} and A_{max}, which maximise the switching speed, can be found [21]. The partial switching times Δt_1 and Δt_2 are inversely proportional to the size of the power area between the two curves i_1 and i_2, for the given voltage swing, 0 to $V_{cc}/2$ (area 1) and $V_{cc}/2$ to V_{cc} (area 2).

Power (area$_1$) and Power (area$_2$) can be calculated:

$$\text{Power (area}_1) = \int_0^{V_{cc}/2} (i_1 - i_2)\, dV = P_{clk} V_{cc} \frac{e\lambda}{hc} \left[\frac{(A_{max} - A_{min})}{4} + \frac{(A^2_{max} - A^2_{min})}{8} \right]$$

$$\text{Power (area}_2) = \int_{V_{cc}/2}^{V_{cc}} (i_1 - i_2)\, dV = P_{clk} V_{cc} \frac{e\lambda}{hc} \left[\frac{3(A^2_{max} - A^2_{min})}{8} - \frac{(A_{max} - A_{min})}{4} \right]$$

Switching time, Δt is inversely proportional to Power (area). To compare S-SEED switching characteristics, we define the unitless coefficient, τ.

$$\Delta t \propto \tau = \tau_1 + \tau_2$$

$$\Delta t_1 \propto \tau_1 = \frac{P_{clk} V_{cc} \frac{e\lambda}{hc}}{\text{Power (area 1)}} \quad \text{and} \quad \Delta t_2 \propto t_2 = \frac{P_{clk} V_{cc} \frac{e\lambda}{hc}}{\text{Power (area 2)}} \qquad \text{(figure 5.2)}$$

Plotting $\tau = \tau_1 + \tau_2$ versus A_{min} for different values of A_{max} (figure 5.4), it is seen that fastest switching speeds of the S-SEED system occur for the largest possible value of A_{max} (A_{max} = 1). This is as expected since for A_{max}=1, the device photocurrent is a maximum and the difference in input powers is a maximum due to one of the inputs being zero (R_{max} = 0). It is seen that for each value of A_{max} there is an optimum A_{min} for which the switching time, Δt is a minimum. This is the tradeoff previously mentioned and is such that if there is insufficient absorption in the low absorption state then switching times will be slower. It can be observed in figure 5.5, that the fastest cascaded S-SEED switching time corresponds to an optimum value of device minimum absorption, A_{min} = 0.22, for A_{max} = 1. Thus for optimum S-SEED speed performance, the maximum absorption A_{max} should be $A_{max\ (opt)}$ = 100% and the minimum absorption $A_{min\ (opt)}$ =22%. This approximately corresponds to a maximum and minimum reflectivity, R_{min}=0% and R_{max}=78%.

{Reference [21] gives the different optimum value of A_{min} = 42%. This is because a much simpler model for estimating the power areas 1 and 2 is used, which overestimates the magnitude of power area$_1$ and underestimates power area$_2$. This represents a much more pessimistic view of the dynamics of the device switching behaviour and results in a larger minimum absorption to give optimum $\Delta t = \tau_1 + \tau_2$. However, the switching time, τ remains within 10% of the minimum (for A_{min} = 22%) for A_{min} up to 44%. It is the value

of A_{max} which is the most sensitive parameter: a 10% reduction in $A_{max}$from 100% to 90%, almost doubles the switching time. Also for lower values of A_{max}, the significance of A_{min} on switching times becomes more significant).

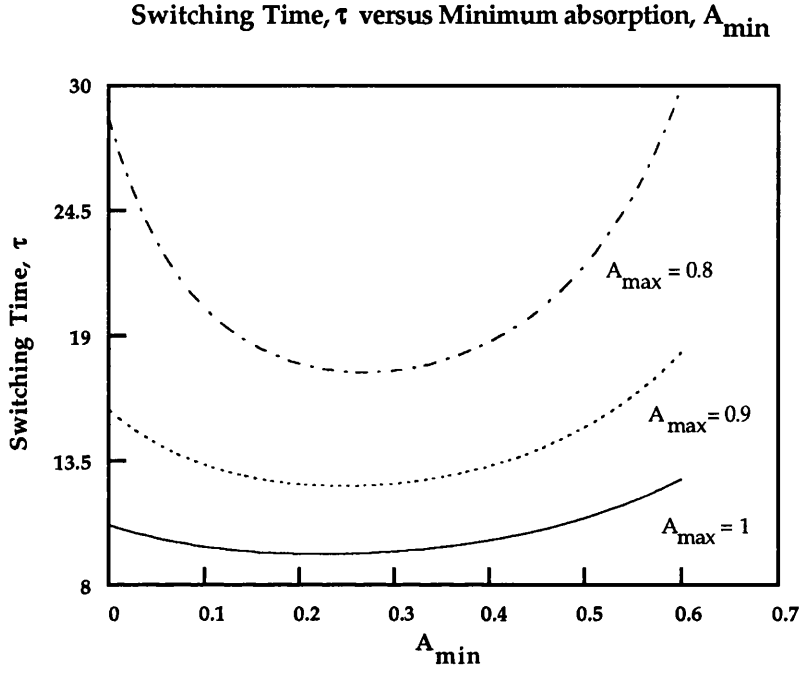

Figure 5.4 Switching Time, τ versus A_{min} for three different A_{max}

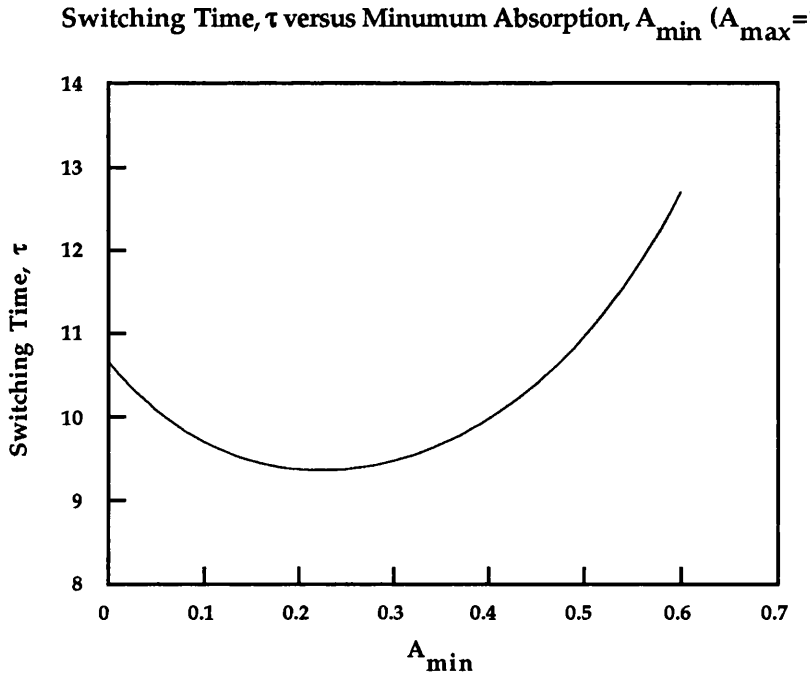

Figure 5.5 Switching Time, τ versus A_{min} (A_{max} = 1)

Therefore making S-SEEDs using the modulation enhancing properties of the asymmetric Fabry-Perot modulator which can give a maximum absorption of 100% yields S-SEED switching devices which are significantly faster than previously possible.

It is interesting to note that the electrical switching energy, E_{elec} is directly proportional to V_{cc}^2 (equation 5.2). The electrical power transferred upon switching however is directly proportional to V_{cc} (equation 5.3). The result of this seems to imply that the total switching time, Δt, is directly proportional to the S-SEED operating voltage, V_{cc}. Thus decreasing the required S-SEED supply voltage, V_{cc} by using a Fabry-Perot cavity which requires less amounts of cavity absorbing material, enables faster switching S-SEEDs to be made. However for decreasing operating voltages, for decreasing intrinsic region width, individual device capacitance, C increases with $1/V_{cc}$. The net result is that reduced operating voltages does not effect the S-SEED switching speed. It is in fact the electric field which is important with respect to switching time, Δt. The smaller the required electric field change on switching, the less energy is required to cause this change, hence reducing the switching time [23].

5.3 Signal beam tolerances

On designing S-SEEDs for use in real applications, it is important to take on board other criteria, besides system speed, when determining optimum device characteristics. If the devices used are not tolerant to variations in their input signals then the device will not easily lend itself to large scale systems applications. For instance, for the case of the input signal beams, it must be ensured that their 'Input Contrast Ratio' is sufficiently greater than the width of the bistable loop so that they can cause the S-SEED to switch and change its state. Additionally, for the case of the time-sequential gain mode of operation, the S-SEED bistable region must be sufficiently wide so as to be able to read out the state of the device without a small difference in clock power causing the device to switch. The 'Output Contrast Ratio' (OCR) of the clock beams, which are the input beams to the next stage in the cascade, should be greater than the 'Required Input Contrast Ratio' (RICR) required for switching. The Signal Margin can be defined as the ratio of the OCR, (R_{max}/R_{min}) to the RICR (A_{max}/A_{min}) (see 4.2.1) and represents the extent which the OCR is greater than the RICR.

$$\text{Signal Margin} = \frac{R_{max}}{R_{min}}\left(\frac{A_{min}}{A_{max}}\right) = \frac{1-A_{min}}{1-A_{max}}\left(\frac{A_{min}}{A_{max}}\right) \qquad \text{where } R = 1 - A$$

For cascaded flip-flop systems as shown in figure 5.1a, if the signal margin is maximised, the allowed variations between the input signals causing the state of the S-SEED to be set and reset, can be maximised. For cascaded logic gate applications, maximising the signal margin, maximises the allowed variations of the signal beam when both beams are acting to change the state of the device. However, when the two

logic inputs are different, maximising the width of the hysteresis loop and hence the RICR, maximises the allowed variations in the signal beams. For logic operations, both a wide bistable loop and a large signal margin is therefore important. This is best achieved by making A_{max} and (A_{max}/A_{min}) as large as possible. {The maximisation of the RICR (A_{max}/A_{min}) is also a key optimisation for the applications using the S-SEED in conjunction with control bias signals, as described in chapter 4 of this thesis. Also, a larger RICR gives rise to a larger dynamic power range possible when these devices are used as linear modulators (chapter 3)}.

It is fortunate that the S-SEED device characteristics for maximum system bit-rate operation give good system signal tolerances. For a device with maximum absorption A_{max} = 100%, the minimum reflected power, R_{max} is 0%. This effectively results in a very high OCR which is always sufficiently greater than the RICR to allow S-SEED switching. For R_{max} = 0%, the inputs to the S-SEEDs are as distinct as possible since one of the inputs is zero. Also, for A_{max}=100%, device responsivity is very close to the theoretical maximum ($e\lambda/hc$) = 0.69 A/W at 860 nm. The required optical switching energy is therefore closer to the ideal since most of the incident light is converted into photocurrent, and for a given input optical power, the switching time, Δt is faster. For the best speed performance, minimum device absorption A_{min} was found to be approximately 22% (figure 5.5). The value of the RICR for an S-SEED utilising this device structure is therefore $A_{max}/A_{min} \approx 4.5$. This represents a very high system tolerance, in that one of the input beams has to be greater or less than the other by more than 4.5 times, to cause switching. The signal margin is also very high since the S-SEED OCR is very much greater than the RICR, due to the very high contrast switching ratios of this device. This is one of the advantages of using high contrast switching devices in switching system applications since the logic levels are very well defined and fan-in/out can be high.

In conclusion, a MQW modulator with device characteristics, A_{max}=100%, A_{min}= 22%, R_{max}=0% and R_{min}= 78%, probably represents the best 'all-round' device to make up an S-SEED, for use in systems applications. Of course, depending on the actual application, one of the device design criteria may be more important and effect the eventually chosen device characteristics accordingly. However the question remains: Can this 'optimum' device, be fabricated from the technology we have at our disposal today?

5.4 Issues effecting the fabrication of the 'ideal' SEED

The asymmetric Fabry-Perot modulator type SEED as demonstrated in chapter 2 of this thesis, has the property that its maximum absorption can be made very high (A_{max}=1) with the result that its responsivity is high and its minimum reflection, R_{min} is virtually zero. The high contrast device design demonstrated [22] satisfies the condition A_{max}=1, for optimum S-SEED performance and high signal margins (5.3). This SEED achieves A_{max}=1, (R_{min}=0), for a small length of active MQW material and therefore operates at lower voltages than conventional non-resonant SEEDs. The use of a Fabry-Perot cavity however, reduces the temperature and wavelength variations which can be tolerated for a given device performance. Also, fabrication of these resonant

devices is much more difficult, due to variations in wafer growth which adversely affect the device's critically sensitive structural parameters. The issue of device temperature sensitivity for these devices is discussed in [24]. Also, signal tolerancing performance such as contrast and operating bandwidth issues are addressed in [25]. Making these devices smaller, decreases their switching energies due to lower device capacitances and is an obvious step towards increasing their speed performance. For these devices, switching energies and operating speeds scale well with device area [26].

Unfortunately however, the S-SEEDs so far demonstrated both in this thesis and in other work, exhibit rather high values of minimum absorption, A_{min} or insertion loss. These devices suffer inherently from large insertion losses due to the large background absorption at the unbiased e1-hh1 exciton peak wavelength of operation. Upon application of an electric field, the exciton red-shifts and loses oscillator strength, but in the high field case quite a significant amount of absorption remains, causing A_{min} to remain quite high. Figure 5.6 below, shows how increasing the number of wells for the device structure used in chapter 2 (2.5), increases the value of A_{min} or Insertion loss (Log [R_{max}]). It is seen that there is a tradeoff between increasing insertion loss and higher contrast. Beyond 30 wells however, (the case when A_{max}=1), there is nothing to be gained in terms of switching contrast ratio. Increasing the amount of absorbing material decreases the ratio of the maximum to the minimum absorption (A_{max}/A_{min}) since the change in absorption ΔA, (A_{max} - A_{min}), becomes less significant with regard to the maximum possible absorption. Figure 5.7 shows how the required input contrast ratio (RICR) or A_{max}/A_{min}, decreases with increasing number of wells within the SEED device structure. For the high contrast, 30 well SEED structure (2.5.2), the insertion loss is quite high at 6.5dB with a corresponding value of $A_{min}\approx 70\%$ (A_{max}=100%). For the 15 well SEED (2.5.1), minimum absorption is lower at about 44% but maximum absorption is also lower at approximately 80%. Therefore in order to get sufficient maximum absorption in the cavity, say for cancellation effects, increasing minimum absorption is also obtained.

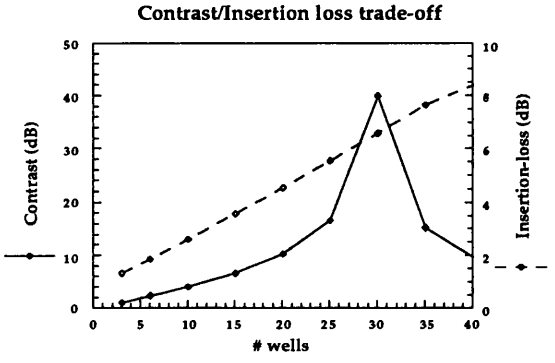

Figure 5.6 Insertion loss/Contrast ratio trade-off for the AFP-SEED

Lower Insertion loss operation can be more readily achieved in the normally-on or bias absorbing (2.1) MQW modulator [27] because in the unbiased state the device is operating at photon energies lower than the band-edge. The background absorption is therefore very much lower. Even lower values of insertion loss can be obtained by increasing the zero field separation between the exciton and the F-P resonance. This however requires larger operating voltages to shift the absorption in and out of the the operating wavelength.

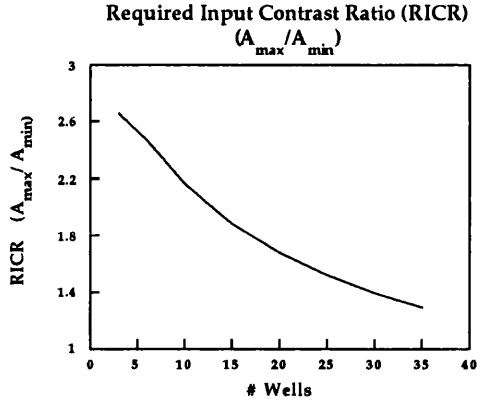

Figure 5.7 RICR versus # wells for AFP-SEED

It can be seen from figure 5.7, that the maximum absorption to the minimum absorption ratio (RICR) is a maximum for very small amounts of absorbing material. This ratio tends towards the ratio of the material absorption coefficients ($\alpha_{max}/\alpha_{min}$) for decreasing number of wells in the absorbing region. For the multiple quantum well structure used for the SEEDs in this thesis, ie. 150Å GaAs wells/ 60Å $Al_{0.3}GaAs$ barriers, $\alpha_{min} \approx 12850\ cm^{-1}$ and $\alpha_{min} \approx 4150\ cm^{-1}$ ($\alpha_{max}/\alpha_{min} \approx 3.1$): Appendix B. It can therefore be deduced that the ratio (A_{max}/A_{min}) is fundamentally limited in magnitude by the ratio ($\alpha_{max}/\alpha_{min}$) of the multiple quantum well material, since increasing the amount of absorbing material in the cavity acts to decreases the RICR. Thus to implement the 'ideal' SEED device, with $A_{max}/A_{min} \approx 4.5$, it requires a material with absorption coefficient ratio, $\alpha_{max}/\alpha_{min}$, significantly greater than 4.5.

In the SEEDs demonstrated in this thesis, relatively wide quantum wells (ie. 150Å) are used. This is because for wider quantum wells, larger changes in the material absorption coefficient are possible for small changes in applied electric field [28,29]. When an electric field is applied, the quantum wells tilt and the electrons and holes move to the bottom corners of the well. The change in energy levels however is always relative to the centre of the well, so that in wider wells, the bottom corner is at a much lower energy with respect to the centre of the well than would be the case for narrower wells, hence for wider wells, larger shifts in particle energies occur for a given electric

field (figure 2.1). Also, because the wavefunctions of the particles are widely separated spatially to the corners of the wells, the overlap integral of the two wavefunctions is very small and thus the exciton oscillator strength for these wide wells decreases much more rapidly than would be the case for narrower wells when an electric field is applied.

Therefore, larger changes in device absorption can be achieved at the unbiased e1-hh1 exciton peak for wider wells than for the narrower wells, for a given electric field change. However with increasing well width, the exciton is less confined and its oscillator strength is decreased. Therefore for wider wells, total absorption decreases but the change in absorption coefficient $\Delta\alpha$ ($\approx \alpha_{max} - \alpha_{min}$) is increased relative to the maximum. Consequently, for a fixed amount of absorption in a cavity, more absorbing material is required because the magnitude of the wider well absorption coefficients are smaller due to decreased confinement. Therefore more wells, requiring larger operating voltages are required to satisfy a given absorption condition. Therefore the optimum choice of well width is a trade-off between increasing absorption coefficient ratio, $\alpha_{max}/\alpha_{min}$ and increasing well material, (and operating voltages for a given electric field), which acts to decrease the total device absorption contrast, RICR (A_{max}/A_{min}).

What ideally is required, is a material structure which yields high values of absorption at the unbiased e1-hh1 exciton peak and which drops to a low value giving absorption coefficient ratios ($\alpha_{max}/\alpha_{min}$) $>\sim 5$, upon application of an electric field.

An example of a material structure which might offer increased performance in this respect is that of coupled quantum wells [7,30,31]. In a coupled well two quantum wells are separated by a very thin barrier forming a composite well between two thicker barriers. When an electric field is applied, the electron is essentially pulled into one well and the hole into the other. This considerably reduces the overlap between the electron and hole wavefunction, so that the probability of finding an electron and hole in the same place is very small and hence the optical absorption at this point is very low. This modulator structure can be viewed as working by changing the strength of the optical absorption rather than actually shifting the absorption edge. This material structure works well and may have improved absorption contrast ratios over conventional 'rectangular' well type structures. This structure can also exhibit the required negative differential resistance characteristic for use in SEED configurations [7].

Another way of looking at the change in absorption of coupled quantum wells upon application of an electric field is to say that the effective absorption edge has been 'blue-shifted'. On applying an electric field, the lowest allowed energy transition becomes weaker as the electrons and holes are pulled into opposite wells. However, some of the higher energy level transitions become stronger and since they are at a higher energy than the original lowest level transitions, the absorption edge can be viewed as having been effectively blue-shifted with the applied field. This is not really a blue shift in the true sense of the meaning and is known as a pseudo-blue shift. 'Blue shifting' has a

distinct advantage over the conventional red-shifting of the absorption edge, as is the case for ordinary rectangular multiple quantum wells. If the absorption edge is blue shifted, then the absorption when an electric field is applied could be made very low, rather than being limited by the background absorption of red-shifted spectra. This might yield high absorption contrasts and low extinction ratios. The effectiveness of the structure would also be less dependent on good exciton peaks and operate over a much wider spectral range. Another structure which makes use of such a blue-shifting phenomenon is that of asymmetric quantum wells, ie. one wide well and one narrow well in a closely coupled configuration [8, 32.] This material's possible use in an optically bistable SEED has also been proposed. This blue shift can be viewed as coming from the applied electric field, cancelling the built-in polarisation of the electron and the hole in such an asymmetrical structure. It is not clear however whether useful devices can be made for use at room temperature using blue shifts in skewed or asymmetric wells in the GaAs/AlGaAs system [33]. However, true blue shifts and S-SEED bistability has been demonstrated using InGaAs quantum wells grown strained on GaAs substrates [34]. Such growth gives piezoelectric fields inside the wells. As an external field is applied to cancel the built-in piezoelectric field, large blue shifts can be obtained.

Other proposed device material structures make use of Wannier-Stark localisation in superlattices [35,36], which are effectively many coupled quantum wells with their spacing small enough so as to allow interaction between adjacent wells. This effect is very similar to that observed in coupled quantum wells. In a superlattice without field, the optical absorption does not have an abrupt absorption edge due to the existence of mini-bands. However on application of an electric field, the mini bands are destroyed and states localised within individual periods of the superlattice are recovered. Thus a sharp absorption edge is recovered and this effect can be used to make electroabsorption modulators [37]. This pseudo blue shift can be used in devices to demonstrate SEED optical bistability and switching [38,39]. Advantages of the superlattice type structure include the possibility of a larger spectral range for usable operation and lower residual absorption, A_{min} which would entail devices with high absorption ratios. Disadvantages however occur in the growth of these materials as very accurately grown thin barrier widths are required.

A number of materials are being investigated for possible use in SEED applications. Longer wavelength devices would be useful especially if operating at the windows of optical fibre low attenuation. For optical computing applications however, which operate over relatively short distances with interconnection using bulk optics, the GaAs/AlGaAs material system and its associated wavelengths of operation offer very good performance. However the prospect of using strained material systems, which offer the ability to be able to effectively tailor the energy transitions and excitonic features in a multiple quantum well material, is a very exciting one.

5.5 SEED performance dependence on negative device resistance

The condition for SEED bistability is $\frac{dI_p}{dv} < \frac{dI}{dv}$ (2.1)

This condition for the R-SEED implies that the resistive load R, must have negative slope conductance larger than the negative slope conductance of the SEED device, ie. $R > \left(\frac{dI_p}{dV}\right)^{-1}$, the resistive loadline must have slope at least as oblique as the region of negative device conductance.

ie. $\frac{dI_p}{dv} < 1/R$ (*)

$\frac{dI_p}{dv} \propto$ change in device absorption, ΔA for a voltage swing, ΔV.

(The value of the negative conductance is simply the slope of the diode current-voltage characteristic at a given voltage and power).

$\Delta A = A_{max} - A_{min}$ for $\Delta V = V(A_{max}) - V(A_{min})$ and

$$I_p = A\frac{e\lambda}{hc}P_{in},\ \Delta I_p = \frac{e\lambda}{hc}P_{in}\Delta A$$

The photocurrent through the modulator is calculated by multiplying the Responsivity $A\frac{e\lambda}{hc}$, by the incident optical power P_{in} on the device. The change in photocurrent ΔI_p is calculated using the change in absorption ΔA for the voltage swing ΔV.

ΔI_p increases with increasing optical power, P_{in} (See figure 5.8). Therefore $\frac{dI_p}{dv}$ increases with increasing P_{in}, or alternatively, the fall in device photocurrent with applied voltage becomes more steep with increasing optical power.

As $\frac{dI_p}{dv}$ becomes greater the minimum Resistive load required for R-SEED switching becomes smaller, ie condition (*) is met for smaller values of R. Therefore, for higher power and photocurrent levels a lower feedback resistance, is required for R-SEED switching. Conversely, increasing the value of the resistive load in an R-SEED, decreases the optical power required for R-SEED switching.

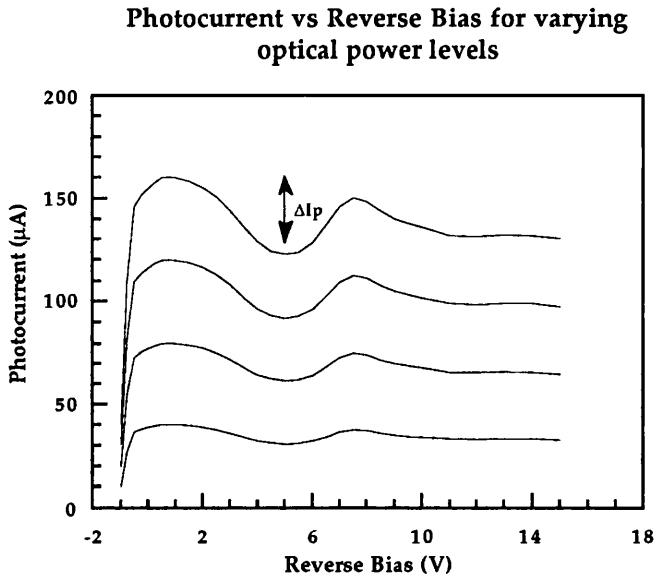

Figure 5.8 Photocurrent vs. voltage characteristic for increasing optical power

See figure 5.9 below showing theoretically how ΔA varies with the number of 150Å GaAs/60Å $Al_{0.3}Ga_{0.7}As$ quantum wells used in the asymmetric Fabry-Perot type SEED structure described in chapter 2 of this thesis. ΔA is a maximum for the 15 well structure (QT74). The magnitude of ΔA has important implications for S-SEED operation (2.3), in that the width of the bistable region is proportional to the change in device photocurrent with applied device bias. Large ΔA also implies large $\frac{dIp}{dv}$, thereby decreasing the resistive load for a given optical power or decreasing the optical power required for switching for a given resistive load.

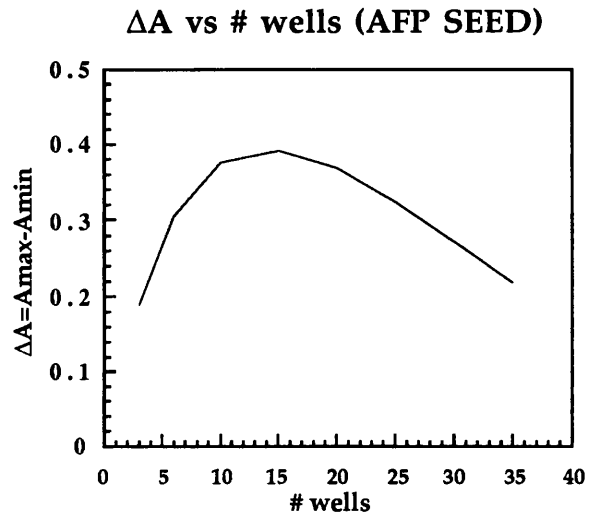

Figure 5.9 Maximum change in absorption, ΔA versus number of wells

The minimum bias voltage, V_{cc} required for R-SEED operation is determined by the intersection of the minimum resistance loadline (required for switching) with the reverse bias voltage axis. The maximum slope of the resistive loadline for switching at a given optical power, corresponds to:

$$\frac{dIp}{dv} = \frac{e\lambda}{hc} P_{in} \frac{\Delta A}{\Delta V}$$

Intersection with the X-axis occurs at:

$$V_{cc\,(min)} = I_{max} / \frac{dIp}{dv} = \frac{e\lambda}{hc} P_{in} A_{max} / \frac{e\lambda}{hc} P_{in} \frac{\Delta A}{\Delta V} = \frac{\Delta V}{\Delta A} A_{max}$$

(I_{max} is the photocurrent corresponding to the maximum absorption A_{max}, for a given incident optical power P_{in})

Therefore $V_{cc(min)} = \Delta V / \Delta A_{rel}$, where ΔA_{Rel} = relative change in device absorption $\Delta A / A_{max}$. See figure 3.5 below showing the minimum bias voltage $V_{cc(min)}$ required for R-SEED switching.

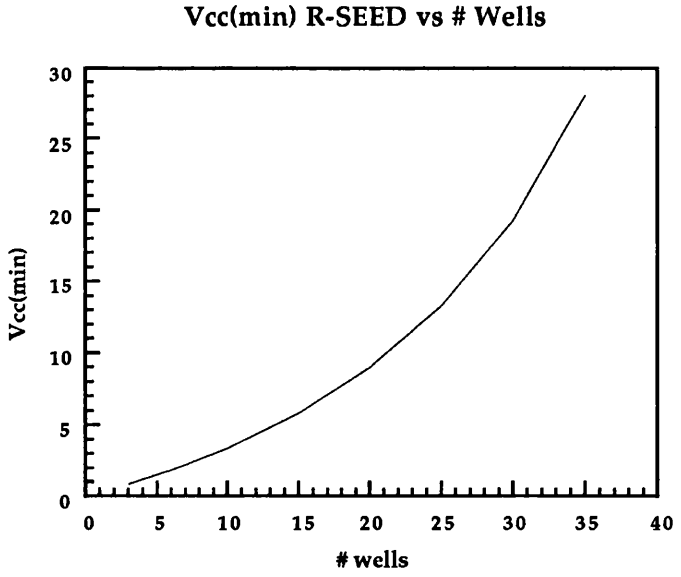

Figure 5.10 Minimum R-SEED operating voltage V_{cc} versus number of wells

It is seen that $V_{cc(min)}$ increases rapidly with increasing intrinsic region width. This is because with more wells and higher background absorption, the relative change in device absorption, ΔA_{Rel} gets smaller and smaller for a larger and larger voltage swing, ΔV. Hence $V_{cc(min)}$ gets rapidly larger. This is another manifestation of the trade-off

between increasing the amount of absorbing material in a device intrinsic region in order to achieve a high maximum absorption, and decreasing the effect of the change in device absorption on application of an electric field. For the case of R-SEEDs, increasing the number of wells gives better switching contrast ratios, but at the expense of very rapidly increasing operating voltages (figure 5.10).

The magnitude of the negative conductance, $g_m = \frac{dIp}{dv}$ is especially important when these devices are used in SEED oscillators [40,41]. Large values of g_m enable low pump thresholds to achieve higher frequency oscillation. The circuit oscillates once the magnitude of the negative differential conductance, g_m is sufficiently large to overcome the losses of the rest of the circuit, and it oscillates at the resonant frequency of the circuit's inductive-capacitive component. The maximum frequency of oscillation, $f_{max} \leq g_m Q/2\pi C$; where Q is the Inductor quality factor, $Q=2\pi fL/R$. Negative conductance and maximum oscillation frequency linearly increase with the optical pump power. However at large powers, g_m increases sub-linearly due to absorption saturation caused by excitonic excitation, therefore fast and efficient carrier sweep-out are necessary. As previously discussed, $g_m \propto \Delta A$. Therefore maximum ΔA and g_m are desirable device performance parameters.

The maximum number of wells corresponding to the maximum value of g_m (ΔA) is a trade-off between having too short an absorption region, resulting in low photocurrent and having the device absorption so large that all the light is absorbed and photocurrent is less sensitive to an applied electric field (figure 5.9). In these applications it is best to have the largest possible slope of negative conductance (ie. the largest possible change in device absorption and hence photocurrent, for the smallest possible voltage swing) in order to give low voltage R-SEED operation and high frequency SEED oscillation.

5.6 High power operation limitations of SEEDs

We have seen in (2.3.4) that S-SEED switching times increase when the difference in the optical power intensities at the inputs is increased. Maximising the difference in optical powers, increases the difference in the photocurrents which act to charge/discharge the individual SEED modulator capacitances. However, because of the build up of photo-induced carriers in the multiple quantum wells, caused by the finite escape time of electrons and holes from the device intrinsic region, the maximum intensity of the optical inputs is limited. This is because the excitonic features of the multiple quantum well material, saturates at a certain carrier level and are effectively 'bleached' so that the electroabsorption characteristics of the device degrade. This exciton saturation limits the system speeds and contrast ratios possible and effectively puts an upper limit on the maximum optical intensities which can be used. Therefore for fast SEED operation at high powers, devices having a very fast and efficient carrier sweep-out rate are favoured in order to minimise the build up of free carriers in the mqw material which leads to saturation.

There are three physical mechanisms that contribute to the field dependence of the carrier lifetime in a quantum well in an electric field [42,43]. These are: recombination, thermionic emission and tunneling. In materials with low impurity concentrations, the component of the carrier recombination rate is usually negligible in comparison to the faster tunneling and thermionic emission rates. The thermionic emission lifetime is principally dependent on the height of the quantum well barrier over which the carriers must be emitted. As the applied electric field is increased, the thermionic emission rate increases because the barrier height is decreased as the well is tilted. The barrier height of these wells can be decreased by using lower values of x in the GaAs-$Al_xGa_{1-x}As$ system. The tunneling rate is determined by the quantum mechanical transmission of the particles through the finite potential barrier. The basic phyical trends in the tunneling rate characteristic are that the tunneling rate increases with electric field, due to the decrease in the effective barrier height and increases with decreasing barrier thickness. There is also a phenomena known as 'resonant tunneling' which occurs when electric field aligns sublevels in adjacent wells and the tunelling rate is enhanced by a coherent process [43].

The main characteristic dependencies of carrier sweep-out time are:

1. Sweep-out time decreases with increasing field because both thermal emission and tunneling lifetimes decrease due to the reduction in the effective barrier height.

2. Sweep-out times increase with increasing barrier width due to the increase in tunnelling time.

3. Sweep-out time increases with ΔE_g (2.1.1) due to the increase in both the thermal emmission and tunneling times. For the GaAs-$Al_xGa_{1-x}As$ system, this means that sweep-out times increase with x, and

4. Sweep-out times decrease with the temperature due to the decrease in the thermal emmission rate.

There is a lot of speculation as to which of the two effects, thermionic emission or tunneling are dominant in determining the carrier escape time. However it is useful to note that thermionic emission is exponentially dependent on T^{-1}, and tunneling is exponentially dependent on the barrier thickness. Of course a thermally assisted tunneling process would be highly sensitive to both. References [42-45] show how the exciton saturation intensity can be increased by using low or thin quantum well barriers, without significant loss to the electroabsorption performance. Also it has been shown that the exciton saturation intensity increases with applied field. The issue of sweep-out time and material saturation are key issues which need to be addressed to ensure that these devices can be operated at speeds fast enough to be useful in systems applications.

5.7 Conclusions

It has been shown in this chapter that for maximum speed performance in a cascaded S-SEED system, SEED devices with maximum and minimum absorption of 100% and 22 % respectively should be used. However for a wide range of A_{min} (up to A_{min} = 44%), switching times only differ by 10% from this optimum. A_{max} is a much more critical parameter than A_{min}, when it comes to determining S-SEED system switching speeds. The Fabry-Perot multiple quantum well devices as described in chapter 2 of this thesis are therefore clearly optimum for use in high speed S-SEED systems because of their maximum possible absorption of 100%. However the minimum absorption of these devices needs to be decreased to give better signal tolerances, wider hysteresis loops and also for marginally faster switching times. By comparing values of τ for the different SEED device structures used in this thesis (5.2), the speed of the high contrast S-SEED in (2.5.2) is estimated to be 1.7 times below that of the optimum and the lower contrast SEED (2.5.1) is estimated to have a switching time approximately twice as long as that of the optimum. The technique of comparing τ's is a very convenient method for comparing the relative switching times of different S-SEEDs with the same material structure. This is because increases (decreases) in the the supply voltage V_{cc} are balanced out by consequent decreases (increases) in the device capacitance (equation 5.2). Some of the design issues for signal tolerancing in SEED systems were also discussed and the significance of the actual slope of the negative device resistance defined with regard to both R-SEEDs and SEED oscillators. Different material structures which might give improved tolerances and speeds for use in SEED systems were also described

5.8 References

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CHAPTER 6

Conclusions

6.1 Conclusions

This thesis has shown how the self electro-optic effect device [1] (SEED) can be improved by the use of an asymmetric Fabry-Perot cavity [2]. Improved SEEDs with high contrast and low operating voltages were demonstrated for use as bistable logic elements [3] and self-linear modulators/optical 'taps' [4]. The limitations and optimisations of these devices were discussed with respect to a number of systems applications and a new way was proposed of operating the SEED tap as a node interface in a daisy-chain cascade type configuration [chapter 3]. This device can self-adjust and vary the amount of light it 'taps' or absorbs in order to compensate for attenuation or fluctuations in power of the optical signal as it passes through the system. This idea was extended theoretically to obtain the functionality of an optical to electronic, serial to parallel, self-adjusting, single stage convertor and which serves as an example of how new optical technologies and techniques can be used in a very simple and effective way in order to implement circuits, normally requiring quite complex electronics.

Current optical switching devices are limited in their usefulness for implementation in real systems. These devices fall into two categories: 'Relational' devices with high bandwidth and no bit-sensitivity, or 'logic' devices with bit-sensitivity but low bandwidth [5]. A new way of operating the symmetric or S-SEED [6] is proposed, which allows the advantages of both classes of devices to be combined [7-9]. This technique makes use of control optical beams to cause the device to behave either logically or relationally. This technique is similar to that used to obtain time sequential gain in conventional S-SEED systems [10] in that two high-power optical beams are simultaneously applied to the S-SEED inputs, in order to read out the state of the device. However with suitable signal formats, this simple device can exhibit quite complex functionality which would normally require relatively sophisticated electronics. The use of this 'S-SEED with intelligence' [8] is proposed for use in a distributed control, self-routeing optical packet switched network and functionality very similar to that required in a single-stage, exchange-bypass element is demonstrated. Although there are significant difficulties and problems associated with cascading S-SEEDs operating in this fashion to form meaningful processing systems, this example again serves to remind us how optical logic might be utilised in new ways, to give rise to more simple, higher performance systems than previously possible or even systems that were previously impossible to implement!

A lot of work has been carried out on integrating electronic functionality around optical input-output devices. These 'electronic islands' or 'smart pixels' [11] make use of the high speed capabilities of small areas of very high speed electonics interconnected

by high-capacity and massively parallel optical communications links. The advantages of both optical and electronic technologies are thus combined to form what is hoped to be a superior implementation over previously all-electronic architectures.

The use of optical technology helps overcome some of the limitations facing electronic circuit designers today. These issues include the pin-out bottleneck, clock distribution and the need for low on-chip power dissipation [12]. There can be no doubt as to the benefits that optical techniques can bring to these types of applications. Economic justification, low research and development spend and short lead times in industry however, seem to dictate the direct replacement of electronic functionality with an optical implementation with similar functionality (eg. co-axial cable communication links being replaced with optical fibre). This has been a highly effective strategy in telecommunications applications where communication distances are very large and the advantages of using optical techniques are irrefutable. As traffic loading and bit-rates increase, the cost advantage of using high capacity optical fibre over conventional electrical techniques will shift to shorter and shorter distances. The penetration of optical fibre is spreading more and more towards the periphery of the network, into business locations and ultimately into our homes! [13].

In optical computing and processing applications we see a similar story, in which the distances over which optical communication techniques are used in preference to electrical techniques, are decreasing. Only recently, inter-building and equipment suite interconnection using optical fibre were just being initiated. Now however we can already see rack to rack optical communication and even optical communication between chips on the same circuit board. In the smart pixel type architectures the trend is towards integrating more and more electronic processing functionality around the optical input/output in order to make the pixel 'smarter' or more intelligent [14]. However, as more and more electronics is integrated around a pixel, the electronic processing systems will again experience the restrictions and limitations which led to optical techniques being introduced in the first place. This process appears cyclical in that more optics is required to again improve system performance. The result of this is that the use of optical communication techniques enters the very heart of electronic processing units. However there is a breakpoint beyond which, the further introduction of optics is unjustified. Current optical logic devices are large relative to their electronic counterparts due to the requirement to get light actually into and out of a device [15]. Consequently, these devices have high switching energies and poor speed performance. The direct replacement of electronic logic devices with similar function optical logic devices is thus effectively ruled out for these reasons and the all-optical computer is extremely unlikely to approach the capabilities of conventional VLSI electronics bar some huge breakthrough in optical logic devices. It is therefore necessary to think more originally than simply directly replacing electronics with optics. There are possibly far more advantages to be gained than can be imagined by looking at entirely new architectures and ways of implementing various applications. The advantages that optics brings to the equation, ie. massive parallelism, high-connectivity, virtually unlimited bandwidth and that of free-space imaging could be used in entirely new ways to produce functionality that was previously impossible or very difficult to achieve electronically but can much more readily be implemented using optical techniques. It is here also, that extensive rewards

are to found rather than purely tit for tat technology replacement.

It is hoped that this thesis and my research work within goes some little way to demonstrating how previously costly, complicated and processing intensive implementations, using electronics might be dramatically simplified and improved by the judicious yet original use of optical switching and communications techniques.

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Appendix A

Fabry-Perot modulator equations

$$\text{Reflectivity, } R = \frac{R_f\left[1-(R_\alpha / R_f)\right]^2}{(1-R_\alpha)^2}$$

$$\text{Absorption, } A = \frac{(1-R_f)\left(1-e^{-\alpha d}\right)\left(1+R_b e^{-\alpha d}\right)}{(1-R_\alpha)^2}$$

$$\text{Transmissivity, } T = \frac{(1-R_f)(1-R_b)e^{-\alpha d}}{(1-R_\alpha)^2}$$

Where $R_\alpha = \sqrt{R_f R_b}\, e^{-\alpha d}$

These equations assume a resonant cavity

Absorption (A) + Transmission (T) + Reflection (R) = 1

Appendix B

Absorption spectra for the 150Å GaAs wells/60Å $Al_{0.3}Ga_{0.7}As$ barrier multiple quantum well material used in this thesis