A 0.4 nJ Excitation Energy Bridge-to-Digital Converter for Implantable Pulmonary Artery Pressure Monitoring

Mustafa Besirli[1], Kerim Ture[1], Diego Barrettino[1], Maurice Beghetti[2], Marco Mattavelli[1], Catherine Dehollain[1], Franco Maloberti[3]

[1]École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland
[2]Pediatric Cardiology Unit, Geneva University Hospitals (HUG), Geneva, Switzerland
[3]University of Pavia, Pavia, Italy
Email: mustafa.besirli@epfl.ch

***Abstract*—This paper presents an energy-efficient, duty-cycled, and spinning excitation bridge-to-digital converter (BDC) suitable for measuring the pulmonary artery pressure of heart failure patients with an implantable system. The duty-cycled bridge uses resistances of 6.2 kΩ and, with a supply of 1.2 V, consumes 0.4 nJ excitation energy. A novel spinning method is applied to the bridge and the capacitive DAC simultaneously in such a way to achieve an offset-independent digital output and to eliminate the need for complex instrumentation amplifiers with offset-reduction techniques or calibration. The SAR ADC fabricated in 0.18-µm CMOS consumes 19 nW at 1.2 V. With a sampling rate of 1 kS/s, the converter achieves the ENOB of 9.2 bits.**

Keywords—medical implantable devices, pressure sensors, SAR ADC, bridge-to-digital converter, duty-cycled, offset compensation.

I. Introduction

Heart failure (HF) is a serious and progressive clinical condition which occurs when the heart is unable to pump enough blood to meet the needs of the body. HF is one of the most important causes of mortality, disability, and health care expenditure in the 21st century, and when it is associated with pulmonary hypertension (PH), the risk increases further [1]. HF affects more than 64 million people worldwide and is expected to rise further due to ageing population [2]. High rate of HF hospitalization results in a significant economic burden to the health care system and decreases the quality of life of millions of patients. In order to adapt treatments based on how the patient reacts to prescribed drugs and to reduce and prevent recurrent HF hospitalizations, it is crucial to continuously (24/7) and accurately monitor the heart activity, in particular, the pulmonary artery (PA) pressure [3]. In addition, the remote monitoring of HF patients proved to be critical during the COVID-19 pandemic since they are in the main risk group. The PA pressure (PAP) of HF patients can be accurately measured with a remotely powered deep implant, which consists of a pressure sensor, its readout circuit, and communication blocks, and is placed in a branch of the PA. In addition to the high accuracy of the pressure measurement, the remotely powered deep implant must have low power consumption and small size.

This project is supported by a grant CRSII5 180272/1 from Swiss National Science Foundation (SNSF) through Sinergia Program.

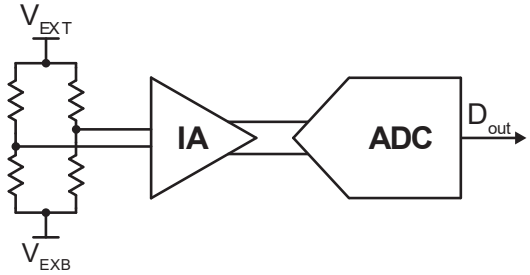

Fig. 1. Conventional bridge-to-digital converter (BDC).

Piezoresistive sensors configured in a Wheatstone bridge are widely used to measure pressure, humidity, and temperature [4]-[7], thanks to their simplicity, reliability, small size and high accuracy. However, they are power hungry, since the bridge resistances are low (usually between 1 kΩ and 10 kΩ). Fig. 1 shows the conventional readout circuit, known as the bridge-to-digital converter (BDC), made by a low-noise instrumentation amplifier (IA) followed by an ADC. In conventional BDCs, the top excitation voltage (V_{EXT}) of the bridge is connected to a DC biasing voltage, and the bottom excitation voltage (V_{EXB}) is grounded [8].

The bridge measurement can achieve high resolution and linearity, but its excitation energy consumption is higher than the interface circuit conversion energy [6] due to low bridge resistances, thus limiting the overall sensor energy-efficiency. Moreover, the offset of the IA affects the accuracy, thus requiring offset-reduction circuits or calibration. Duty-cycling the excitation reduces the bridge excitation energy from 125 times [4] to 6000 times [5] compared to static biasing. However, the limit caused by the offset is still a concern. This paper exploits the duty-cycling of the bridge for cancelling the IA offset at the same time. The circuit reduces the excitation energy consumption by a factor of 640 times and avoids the use of complex IAs [6] that foresee offset-reduction techniques or need calibration. This method makes the bridge sensor suitable to be used in deep implants, since it achieves both high accuracy and low energy consumption.

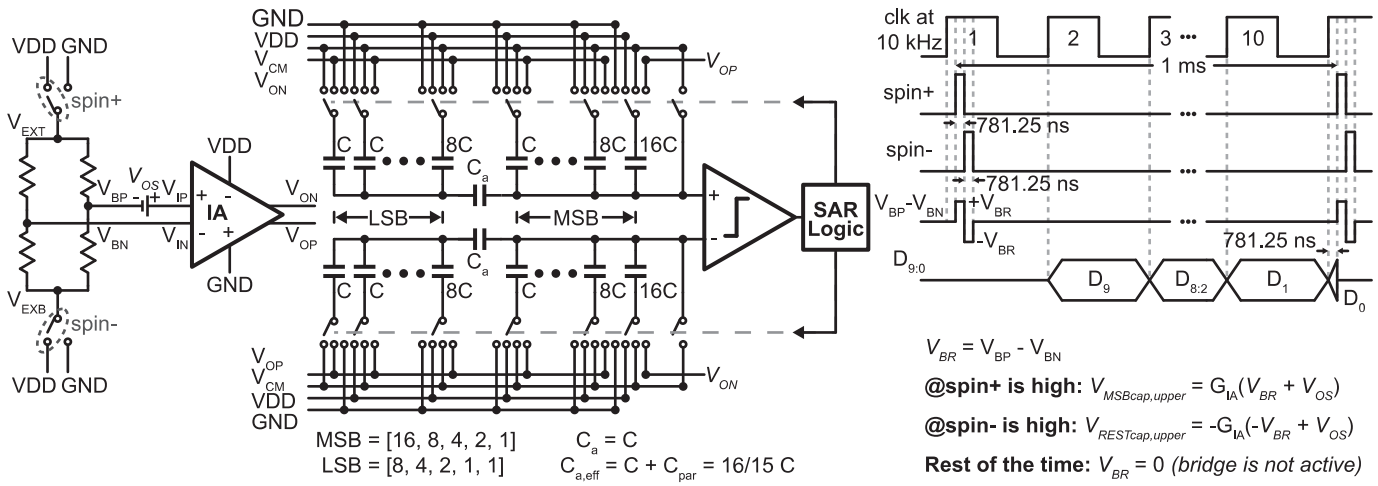

Fig. 2. Circuit diagram of the highly duty-cycled and spinnning excitation BDC and its timing diagram.

II. Proposed Duty-Cycled and Spinning Excitation BDC

Fig. 2 shows the circuit diagram of the proposed duty-cycled and spinning excitation BDC to measure the PAP of HF patients with a remotely powered deep implant. Switches controlled by spin+ and spin- signals spin both the bridge excitation (V_{EXT}, V_{EXB}) and the capacitive DAC's sampling inputs (V_{OP}, V_{ON}). Switches reverse the bridge connections so that during one phase, the bridge's output is $+V_{BR}$, and during the other phase, the output is equal and opposite $-V_{BR}$. The result is like the one obtained with the chopper-stabilized method; the IA's output is the amplification of the chopped signal, plus the amplification of the offset of the IA. Instead of using a second chopper [9], the circuit uses the following strategy. Half of the positive array of the cascaded DAC charges to V_{OP} during the first spin, and half of the negative array charges to V_{ON}. When the bridge signal reverses, the second half of the positive array charges to V_{ON}, and the second half of the negative array charges to V_{OP}. The result is that the total charge on the array depends only on the bridge signal and compensates for the offset. However, there is a residual offset due to the mismatch between the two halves of the capacitive arrays, but this error is negligible if the resolution of the SAR ADC is not too high.

The timing diagram in Fig. 2 shows a spin+ high for 781.25 ns to connect the top excitation voltage (V_{EXT}) to VDD while the bottom excitation voltage (V_{EXB}) goes to GND for generating the bridge output $+V_{BR}$. The spin+ goes low before spin- rises, thus avoiding a short circuit. It lasts for another 781.25 ns for generating the bridge output $-V_{BR}$. The biasing of the bridge lasts for only 1.5625 µs out of 1 ms conversion time. Therefore, the excitation energy consumption is 640 times less than an equivalent static DC biasing. When spin+ is high, V_{OP} charges the MSB capacitor (16C) of the SAR positive array, while V_{ON} charges the SAR negative array's MSB capacitor (16C). All the other capacitors remain floating during spin+. When spin- is high, V_{ON} charges the remaining capacitors (equivalent to 16C) of the SAR positive array while the MSB is floating. A similar operation holds for the capacitors of the negative side. In this way, the total charges in the positive and negative DAC arrays depend only on the two phases of the bridge signal. The given operation performs a correlated double sampling action over the IA offset, and compensates for it, since the MSB capacitor and the rest of the array have equal value.

III. SAR ADC Prototype and Implementation

A 10-bit 1 kS/s SAR ADC has been designed and fabricated in 0.18-µm CMOS technology. Fig. 2 shows the architecture of the proposed SAR ADC. It comprises differential capacitor networks, a low power dynamic comparator and a synchronous SAR control logic [10]. The dynamic comparator consists of a StrongARM latch followed by an RS latch [11]. In addition, the prototype includes a spinning control logic that generates spin+, spin- and two clock signals at 1 kHz and 10 kHz from a 1.28 MHz applied clock. A fully-differential architecture was employed to suppress the supply noise and to have a good common-mode noise rejection. The bridge sensor and the IA in Fig. 2 are off-chip components.

The capacitive DAC uses the V_{CM}-based switching method [10] to reduce the switching power. Moreover, the split capacitor technique, instead of the full binary-weighted arrays, reduces the arrays' total capacitance, thus reducing power and area. For the selected technology and 3σ design, the unit capacitance (C) must be higher than 17.2 fF. Besides, the capacitive DAC's split structure requires a low parasitic capacitance in the array's LSB internal node. This circuit employs a relatively large unity value of C = 76.8 fF to make the parasitic of the interconnection metal lines negligible and relax the kT/C noise limitation significantly. The attenuation capacitor (C_a) should be 16/15*C for high linearity; however, this value is not suitable for capacitor matching since its size is not unity. The chosen solution is to have a unity capacitance for C_a and adjust the layout of the top-to-bottom parasitic (C_{par}) of C_a for having an effective capacitance ($C_{a,eff}$) of 16/15*C ≈ 81.9 fF.

The sampling action in the capacitive DAC occurs when spin+ or spin- is high and lasts only 1.5625 µs. This fast sampling with high linearity allows a highly duty-cycled bridge sensor and results in a significant reduction in the excitation energy consumption of the bridge. The timing diagram in Fig. 2 shows that the LSB estimation happens during the same period than the sampling as it requires only 1.5625 µs and one conversion cycle is completed in only 10 clock periods.

IV. Measurement Results

The prototype with the ADC and excitation switches was fabricated and tested. Fig. 3 shows the die micrograph whose core area is 197 × 181 µm^2. The measured FFT spectrum with the input frequencies at 199.9 Hz and 479.9 Hz is shown in Fig. 4. The supply voltage is 1.2 V and the sampling rate is the nominal 1 kS/s. At 199.9 Hz input frequency, the measured SNDR and SFDR are 57 dB and 66.5 dB, respectively. The resultant ENOB is 9.2. At 479.9 Hz, close to Nyquist, the measured SNDR and SFDR are 55.3 dB and 61.7 dB, respectively, showing a negligible drop of performance. Thus, the effective resolution bandwidth (ERBW) is higher than Nyquist bandwidth since the SNDR drop is less than 3 dB over the entire bandwidth. The DNL and INL are illustrated in Fig. 5. At 1 kS/s sampling rate, the peak DNL and INL are +0.3 / –0.36 LSB and +1.8 / –1.3 LSB, respectively.

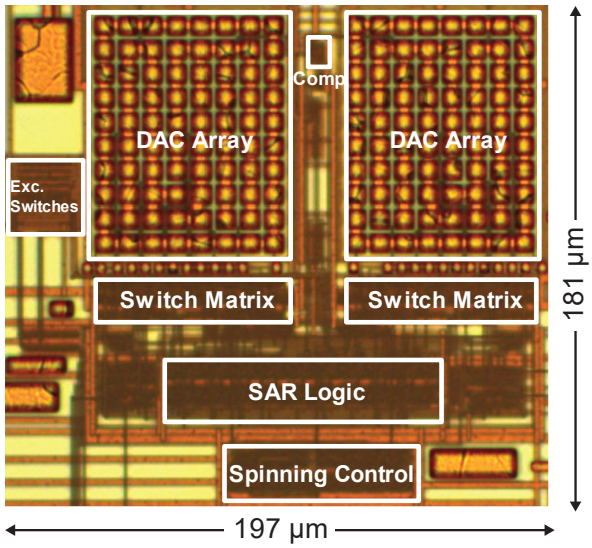

Fig. 3. Die micrograph of the prototype.

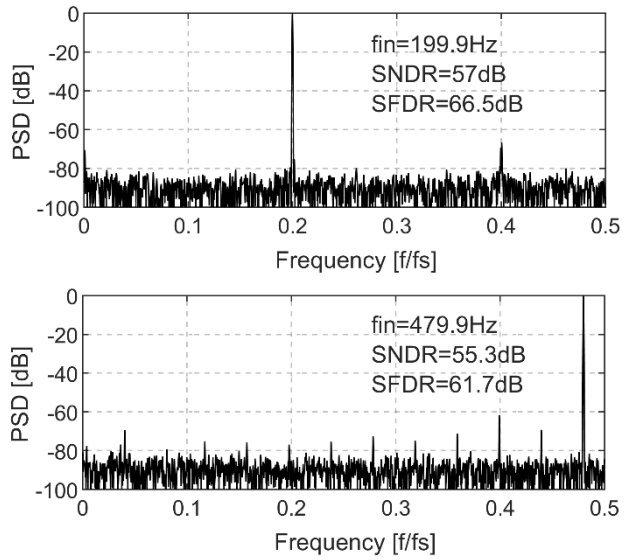

Fig. 4. Measured 8192-point FFT spectrum at 1 kS/s.

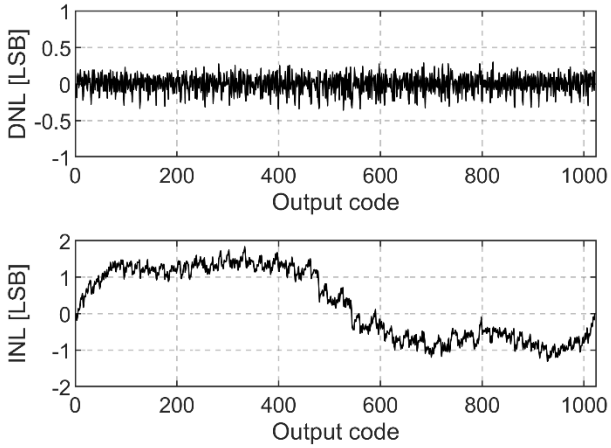

Fig. 5. Measured DNL and INL.

The test circuit uses multiple supply voltage connections to allow a detailed measurement of the power consumption in the comparator, capacitive DAC, and SAR logic. The experimental verification shows that the comparator, capacitive DAC, and SAR logic consume 0.5, 5.8 and 12.7 nW at 1.2 V, respectively. Overall, the circuit consumes only 19 nW, at the nominal 1kS/s sampling frequency resulting in a figure-of-merit (FOM = Power/2^{ENOB}*2*ERBW) of 32.3 fJ/conversion-step. The power consumption of the spinning control logic was not considered. As an example, if the bridge uses a 47 kΩ thermistor, the bridge current is 25.5 µA at 1.2 V. The 640 times power reduction leads to a bridge power of 47.9 nW, which is only a few times more than the prototype ADC. Table I summarizes the measured performance of the prototype ADC.

The proof of offset-independent output code and negligible residual offset results from the measurements with two IAs with different input offsets. Fig. 6a shows the first amplifier's (THS4551 [12]) output signals with a peak-to-peak output voltage of 511 mV. The output offset is 596.5 mV – 607.3 mV = –10.8 mV. Fig. 6b shows the second amplifier's (THS4121 [13]) output signals with the same peak-to-peak output voltage of 511 mV, leading to an output offset of 621.6 mV – 599.8 mV = 21.8 mV. In both cases, the SAR ADC ($D_{9:0}$) gives the input's exact value, showing the offset cancellation, and that the possible residual offset does not affect the circuit performance.

Table II compares the energy performance of the bridge sensor excitations only. The conversion energy of the bridge, which has been used to compare the performance of different bridge excitations, is defined as

$$E_{Conv\_bridge} = \frac{V_{supply}^2}{R_{bridge}} \times \left(\frac{T_{conv}}{N_{duty\_cycle}} \right), \qquad (1)$$

where V_{supply}, R_{bridge}, T_{conv} and N_{duty_cycle} are the bridge supply, bridge resistance, conversion time and number of duty-cycling, respectively. The bridge's excitation energy in this work is about 0.4 nJ/conversion-step, which is better than the state-of-the-art and is mainly due to the low supply voltage and the high duty-cycling. A novel spinning method is applied to the bridge and the capacitive DAC simultaneously in such a way to achieve an

offset-independent digital output and to eliminate the need for complex IAs with offset-reduction techniques or calibration.

TABLE I. PERFORMANCE SUMMARY OF THE SAR ADC

Technology	0.18-µm CMOS
Resolution	10 - bit
Sampling Rate	1 kS/s
Supply Voltage	1.2 V
SNDR	57 dB
SFDR	66.5 dB
ENOB	9.2 - bit
DNL	+0.3 / −0.36 LSB
INL	+1.8 / −1.3 LSB
FOM=Power/2^{ENOB}*2*ERBW	32.3 fJ/conversion-step
Power Consumption	
Comparator	0.5 nW
Capacitive DAC	5.8 nW
SAR Control Logic	12.7 nW
Total	19 nW

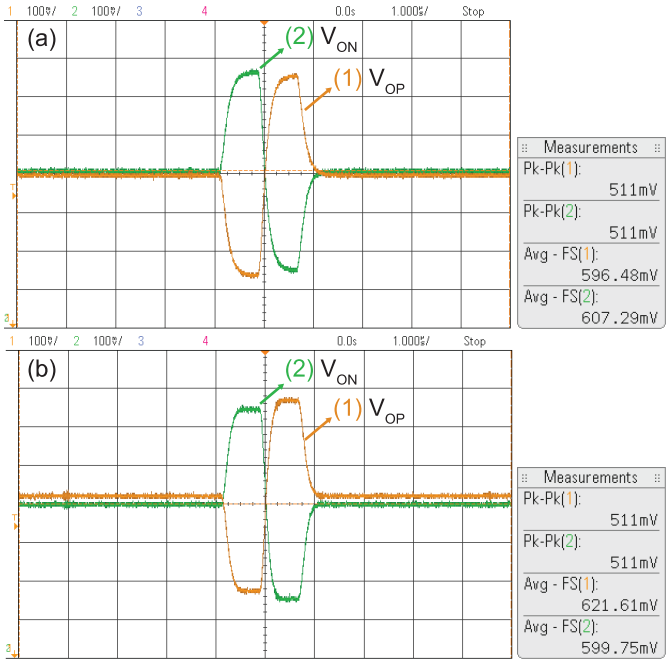

Fig. 6. Output voltages of the first (a) and second (b) amplifiers.

TABLE II. PERFORMANCE SUMMARY OF THE BRIDGE EXCITATION AND COMPARISON

	This Work	[4]	[5]	[6]	[7]
Bridge Supply (V)	1.2	1.8	3.6	5	1.8
Bridge Resistance (kΩ)	6.2	1	6	3.7	5
Bridge Static Power (mW)	0.23	3.24	2.16	6.76	0.65
Duty-cycling Factor	~580x	~17.5x	~4320x	Non	~256x
Conversion Time (ms)	1	1	1	0.5	0.27
Energy/Conversion of Bridge (nJ/conversion-step)	0.4	185	0.5	3378	0.68

V. CONCLUSION

This paper presented a duty-cycled and spinning excitation bridge-to-digital converter suitable for measuring the PAP of HF patients with a deep implant. The design exploits the duty-cycling of the bridge for cancelling the IA offset at the same time. The circuit reduces the excitation energy consumption by a factor of 640 times and the bridge's excitation energy in this work is 0.4 nJ/conversion-step, which is better than the state-of-the-art. The used spinning method provides an offset-independent digital output, thus avoiding the use of complex IAs that foresee offset-reduction techniques or need calibration. The SAR ADC in the BDC was fabricated in 0.18-µm CMOS technology and achieved 9.2 ENOB at a sampling rate of 1 kS/s. The prototype ADC draws only 19 nW power from the 1.2 V supply and has a FOM of 32.3 fJ/conversion-step. The measurement results show that the proposed duty-cycled and spinning BDC can be used in deep implantable devices that continuously monitor the PAP since it can achieve high accuracy and low power consumption at same time.

REFERENCES

[1] P. Ponikowski et al., "Heart failure: preventing disease and death worldwide," ESC heart failure, vol. 1, no. 1, pp. 4–25, September 2014.

[2] S. L. James et al., "GBD 2017 Disease and Injury Incidence and Prevalence Collaborators. Global, regional, and national incidence, prevalence, and years lived with disability for 354 diseases and injuries for 195 countries and territories, 1990-2017: a systematic analysis for the Global Burden of Disease Study 2017," Lancet, vol. 392, no. 10159, pp. 1789–1858, November 2018.

[3] W. T. Abraham and L. Perl, "Implantable hemodynamic monitoring for heart failure patients," Journal of the American College of Cardiology, vol. 70, no. 3, pp. 389–398, July 2017.

[4] R. Grezaud et al., "A robust and versatile, −40°C to +180°C, 8Sps to 1kSps, multi power source wireless sensor system for aeronautic applications, " 2017 Symposium on VLSI Circuits, Kyoto, Japan, 2017, pp. C310-C311.

[5] S. Oh et al., "A 2.5nJ duty-cycled bridge-to-digital converter integrated in a 13mm3 pressure-sensing system, " 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2018, pp. 328-330.

[6] H. Jiang, S. Nihtianov, and K. A. A. Makinwa, "An energy-efficient 3.7-nV/√Hz bridge readout IC with a stable bridge offset compensation scheme," IEEE Journal of Solid-State Circuits, vol. 54, no. 3, pp. 856–864, March 2019.

[7] A. Rezvanitabar, G. Jung, Y. S. Yaras, F. L. Degertekin and M. Ghovanloo, "A Power-Efficient Bridge Readout Circuit for Implantable, Wearable, and IoT Applications," IEEE Sensors Journal, vol. 20, no. 17, pp. 9955-9962, September 2020.

[8] H. Jiang and K. A. A. Makinwa, "Energy-efficient bridge-to-digital converters," 2018 IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, USA, 2018, pp. 1-7.

[9] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," Proceedings of the IEEE, vol. 84, no. 11, pp. 1584-1614, November 1996.

[10] Y. Zhu et al., "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1111-1121, June 2010.

[11] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, Spring 2015.

[12] Texas Instruments, "Low-noise, precision, 150-MHz, fully differential amplifier," THS4551 datasheet, April 2016 [Revised April 2021].

[13] Texas Instruments, "High-speed fully differential I/O amplifiers," THS4121 datasheet, February 2001 [Revised October 2004].