DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Timing-Error Tolerance Techniques for Low-Power DSP: Filters and Transforms

A thesis submitted for the degree of Engineering Doctorate

Paul N. Whatmough

Department of Electronic and Electrical Engineering

University College London

May 2012

Statement of Originality

I, Paul N. Whatmough confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Signed: ______________________________

Date: ________________________________

Abstract

Low-power Digital Signal Processing (DSP) circuits are critical to commercial System-on-Chip design for battery powered devices. Dynamic Voltage Scaling (DVS) of digital circuits can reclaim worst-case supply voltage margins for delay variation, reducing power consumption. However, removing static margins without compromising robustness is tremendously challenging, especially in an era of escalating reliability concerns due to continued process scaling. The Razor DVS scheme addresses these concerns, by ensuring robustness using explicit timing-error detection and correction circuits. Nonetheless, the design of low-complexity and low-power error correction is often challenging.

In this thesis, the Razor framework is applied to fixed-precision DSP filters and transforms. The inherent error tolerance of many DSP algorithms is exploited to achieve very low-overhead error correction. Novel error correction schemes for DSP datapaths are proposed, with very low-overhead circuit realisations. Two new approximate error correction approaches are proposed. The first is based on an adapted sum-of-products form that prevents errors in intermediate results reaching the output, while the second approach forces errors to occur only in less significant bits of each result by shaping the critical path distribution. A third approach is described that achieves exact error correction using time borrowing techniques on critical paths. Unlike previously published approaches, all three proposed are suitable for high clock frequency implementations, as demonstrated with fully placed and routed FIR, FFT and DCT implementations in 90nm and 32nm CMOS. Design issues and theoretical modelling are presented for each approach, along with SPICE simulation results demonstrating power savings of 21 – 29%.

Finally, the design of a baseband transmitter in 32nm CMOS for the Spectrally Efficient FDM (SEFDM) system is presented. SEFDM systems offer bandwidth savings compared to Orthogonal FDM (OFDM), at the cost of increased complexity and power consumption, which is quantified with the first VLSI architecture.

Biography

Paul N. Whatmough was born in Derby, U.K. in 1981. He received the B.Eng. degree (first class Hons.) in Electronic Communications Engineering from the University of Lancaster, U.K., in 2003 and the M.Sc. degree (with distinction) in Communications Systems and Signal Processing from the University of Bristol, U.K, in 2004. He started the Engineering Doctorate degree at University College London, U.K., in November 2008. During his Doctoral studies he also completed three electives in Strategy at the London Business School, in addition to the APMP IPMA Level D, SCQF Level 7 certification in project management.

From 2005 to 2008, he held the position of Research Scientist in the Wireless Group at Philips Research Labs, Redhill, U.K. (which became NXP Semiconductors, Corporate Research in 2006), working on multi-standard highly-digital transceiver architectures and circuits, particularly in the area of power amplifier efficiency enhancement techniques.

In 2008, he joined the Silicon Research Group in the R&D department of ARM Ltd., Cambridge, U.K., while working towards the Engineering Doctorate degree. His current research interests are in low-power circuits, algorithms and architectures relating to Wireless, DSP and Embedded Computing.

Mr. Whatmough is a member of the IET and IEEE. He was the recipient of the IET Undergraduate Student Project Award in 2003, the IEEE Communications Chapter Award in 2004 for his postgraduate dissertation research on low-power Viterbi decoder implementation for WLAN, and the European Wireless Technology Conference (EuWiT) Young Engineer Prize in 2008.

Acknowledgements

I would like to thank all those at UCL who have supported me throughout this endeavour. I am very grateful to my academic supervisor Professor Darwazeh, who was a great source of encouragement, especially during the preparation of this thesis. I would like to thank my fellow students Marcus Perrett and Safa Isam whom I had the pleasure of collaborating with on the baseband transmitter study in Chapter 6. Thanks also to Paul McKenna and the administration team at UCL.

I am very grateful to my industrial supervisors at ARM, David Bull and Danny Kershaw, who have provided technical and moral support, inspiration and motivation. My sincere thanks also to Shidhartha Das for all the encouragement and late night collaboration on conference papers and last minute tapeouts.

My family and friends have been a great source of inspiration to me through their own achievements; I am very grateful for their support and encouragement. Finally, I would like to thank my partner Stephanie: I am forever indebted to you for your encouragement, support and dedication. You also make a great cup of tea.

This doctoral research was jointly sponsored by the U.K. Engineering and Physical Sciences Research Council (EPSRC) and ARM Ltd., U.K. under the Engineering Doctorate programme. The financial support of both organisations is gratefully acknowledged.

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List of Abbreviations

2D	-	Two Dimensional
3GPP	-	Third Generation Partnership Project
ANT	-	Algorithmic Noise Tolerance
APR	-	Automatic Place and Route
ARM	-	Advanced RISC Machines
ASIC	-	Application Specific Integrated Circuit
ASK	-	Amplitude Shift Keying
AVS	-	Adaptive Voltage Scaling
AWGN	-	Additive White Gaussian Noise
BC	-	Best Case
BER	-	Bit Error Rate
BF	-	Butterfly
BIST	-	Built In Self Test
BTI	-	Bias Temperature Instability
CMAC	-	Complex Multiply Accumulate
CMOS	-	Complementary Metal Oxide Semiconductor
CORDIC	-	COordinate Rotation DIgital Computer
CPPR	-	Common Path Pessimism Removal
CPU	-	Central Processing Unit
CS	-	Carry-Save
DCT	-	Discrete Cosine Transform
DDS	-	Direct Digital Synthesis
DFT	-	Discrete Fourier Transform
DRAM	-	Dynamic Random Access Memory
DSM	-	Deep Sub Micron
DSP	-	Digital Signal Processing
DVFS	-	Dynamic Voltage Frequency Scaling
DVS	-	Dynamic Voltage Scaling
ECC	-	Error Correction Coding
EDA	-	Electronic Design Automation
FDM	-	Frequency Division multiplexing
FF	-	Flip-Flop
FFT	-	Fast Fourier Transform
FIFO	-	First In First Out
FIR	-	Finite Impulse Response
FOFDM	-	Fast Orthogonal Frequency Division Multiplexing
FPGA	-	Field Programmable Gate Array
FSD	-	Fixed complexity Sphere Decoder

FTN	-	Faster Than Nyquist
GP	-	General Purpose
GPRS	-	General Packet Radio Service
GSM	-	Global System for Mobile communications
HCI	-	Hot Carrier Injection
HC-MCM	-	High Compaction Multi-Carrier Communications
HSPA	-	High Speed Packet Access
IC	-	Integrated Circuit
IIR	-	Infinite Impulse Response
IP	-	Intellectual Property
KSA	-	Kogge-Stone Adder
LER	-	Line Edge Roughness
LMS	-	Least Mean Squared
LP	-	Low Power
LSB	-	Least Significant Bit
LTE	-	Long Term Evolution
LTEA	-	Long Term Evolution, Advanced
LUT	-	Look-Up Table
MAC	-	Multiply Accumulate
MASK	-	M-ary Amplitude Shift Keying
MIMO	-	Multiple Input Multiple Output
ML	-	Maximum Likelihood
MMSE	-	Minimum Mean Square Error
MSB	-	Most Significant Bit
MSFF	-	Master Slave Flip-Flop
OCV	-	On-Chip Variation
OFDM	-	Orthogonal Frequency Division Multiplexing
OvOFDM	-	Overlapped Orthogonal Frequency Division Multiplexing
PAPR	-	Peak to Average Power Ratio
PDS	-	Path Delay Shaping
PoFF	-	Point of First Failure
PSNR	-	Peak Signal to Noise Ratio
PVT	-	Process Voltage Temperature
QAM	-	Quadrature Amplitude Modulation
QPSK	-	Quadrature Phase Shift Keying
RAM	-	Random Access Memory
RB	-	Ring Buffer
RCA	-	Ripple-Carry Adder
RDF	-	Random Dopant Fluctuations
RFF	-	Razor Flip-Flop
RISC	-	Reduced Instruction Set Computer

ROM	-	Read Only Memory
RPL	-	Razor Pulse Latch
RPR	-	Reduced Precision Redundancy
RTL	-	Register Transfer Level
SD	-	Sphere Decoder
SDC	-	Significance Driven Computation
SEFDM	-	Spectrally Efficient Frequency Division Multiplexing
SEU	-	Single Event Upset
SNR	-	Signal to Noise Ratio
SNR	-	Signal to Noise Ratio
SoC	-	System on Chip
SPICE	-	Simulation Program with Integrated Circuit Emphasis
SQNR	-	Signal to Quantisation Noise Ratio
SR	-	Shift Register
SRAM	-	Static Random Access Memory
STA	-	Static Timing Analysis
TDDB	-	Time Dependent Dielectric Breakdown
TSVD	-	Truncated Singular Value Decomposition
UMTS	-	Universal Mobile Telecommunication System
VLSI	-	Very Large Scale Integration
WC	-	Worst Case
ZF	-	Zero Forcing

Chapter 1. Introduction

The first trans-Atlantic radio frequency transmissions conducted by Marconi and Fleming[1] in 1901 occupied a huge band of radio spectrum, transmitting a meagre amount of information by modern standards [1]. Subsequently, the rate of technology development in communication systems has been truly remarkable. The numerous and increasingly ubiquitous mobile communications devices of today of capable of achieving very high throughput rates, in turn motivating strong emphasis on the joint goals of power efficiency and spectral efficiency. This thesis addresses these interrelated goals, with a strong emphasis on Integrated Circuit (IC) implementation of DSP systems.

This chapter begins by motivating the need for low-power DSP design techniques in order to allow for continuing improvements in spectral efficiency, within a fixed power budget. Trends relating to standardised cellular communication systems are described and related to developments in IC manufacturing technology. Finally, a brief introduction is given to the promising techniques that are central to

[1] Fleming, inventor of the vacuum tube, was chair of Electrical Engineering at UCL for 42 years. It is a little known fact that he designed the 20,000 V transmitter station used in Marconi's experiments.

the research work of the thesis. The organisation of the thesis is then described, before identifying the key contributions of this work.

1.1 Motivation for Resilient Low-Power DSP

Advancements in signal modulation, detection, source coding, channel coding and multiple access techniques [2] have ensured that historical improvement in spectral efficiency has been approximately linear over the last century, according to Cooper's Law[2]. However, this improvement in spectral efficiency has, in recent years, been achieved mainly through gratuitous use of DSP techniques. Figure 1.1 shows a remarkable trend in the development of downlink throughput rates in standardised cellular communication systems of an order of magnitude increase every five years.

For many decades, this was enabled by advances in successive generations of IC manufacturing technologies, which allowed rapidly increasing DSP workloads to be supported without exceeding the limited power budget of a battery powered mobile device.

Scaling of transistor geometry according to Moore's Law [3] has increased speed and reduced manufacturing cost of ICs, along with a reduction in power dissipation due to Dennard's law [4]. Currently, power efficiency has become of critical significance due to the fact that while Dennard scaling has previously allowed increases in DSP workload within a roughly fixed battery volume, the supply voltage scaling which enables this has all but stopped in the last decade.

[2] Cooper developed the first handheld mobile phone at Motorola. He later observed that the number of simultaneous "conversations" (voice or data) possible over the radio spectrum has doubled every 30 months for the last century.

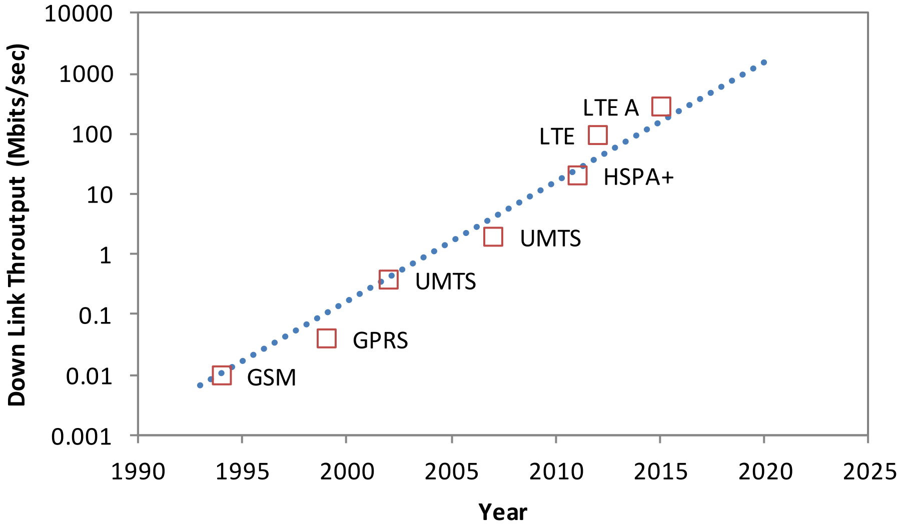


Figure 1.1: Trends in throughput for 3GPP cellular systems. The trend line shows an order of magnitude increase in throughput every 5 years. Adapted from [5].

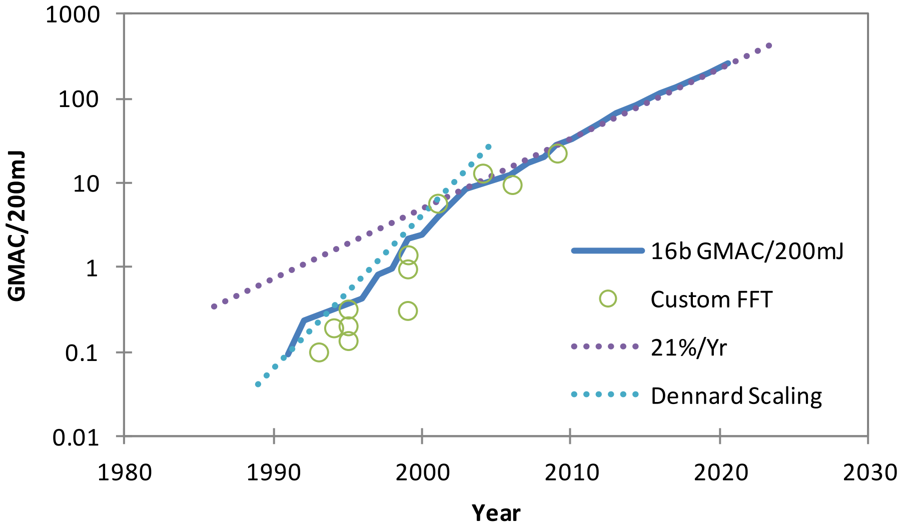


Figure 1.2: Trends in energy constrained real 16-bit multiply accumulate (MAC) operations on custom hardware, including reported FFT implementations. Adapted from [5].

Figure 1.2 shows the historical trend for power constrained computational performance of DSP hardware in terms of 16-bit multiply-accumulate (MAC) operations. Around the start of the new millennium, improvements due to process scaling have slowed to approximately 21% per year, which means that further increases in DSP workload open up an increasing gap in the power budget [5]. The work in this thesis is motivated by the need to support future improvements in throughput and spectral efficiency, through increased DSP workloads, without compromising power efficiency.

The main focus of the research is the reduction of design margins for process, voltage and temperature variability, in order to address the power efficiency gap. Digital circuit design of key building blocks of DSP filters and transforms are examined. These building blocks are widely applicable amongst diverse applications including wireless communication systems and the processing of audio, image and video signals. To increase power efficiency, a framework is applied to reduce wasteful worst-case supply voltage margins, which traditionally account for performance variability due to manufacturing process, supply voltage and temperature variations. The Razor technique [6], developed by Ernst et al. in 2004, uses timing-error detection in digital circuits to provide feedback in order to reduce design margins using supply voltage scaling, leading to quadratic savings in power consumption. This approach has been demonstrated to offer considerable power savings in reported microprocessor implementations [7][8][9][10]; however, it generates intermittent logical errors which require correction, complicating the design process.

While the Razor concept has been studied mainly in the context of microprocessor variation resilience and power efficiency, the work in this thesis addresses application to custom DSP hardware. The implicit error tolerance of many DSP algorithms is exploited to relax the complexity and power consumption of the error correction mechanism. Two new approximate error correction approaches are proposed. The first is based on an adapted sum-of-products form that prevents errors in intermediate results reaching the output, while the second approach forces errors to occur only in less significant bits of each result by shaping the critical path distribution. A third approach is described that achieves exact error correction using time borrowing techniques on critical paths. Unlike previously published approaches, all three proposed are suitable for high clock frequency implementations, as demonstrated with fully placed and routed Finite Impulse Response (FIR), Fast Fourier Transform (FFT) and Discrete Cosine Transform (DCT) implementations in 90nm and 32nm Complementary Metal Oxide Semiconductor (CMOS). Design issues and theoretical modelling are presented for each approach, along with SPICE simulation results demonstrating power savings of 21 – 29%.

This thesis also offers insight into how future developments in spectral efficiency will come at the cost of increasing DSP workloads by looking at a promising modulation technique called Spectrally Efficient Frequency Division Multiplexing (SEFDM). Focussing on the practical implementation of the transmitter, the existing theoretical work in this area is extended with the first Very Large Scale Integration (VLSI) architecture study for the signal generation algorithms, revealing the required overheads in circuit area and power consumption required to enable future improvements in spectral efficiency. Two new variants of a digital baseband transmitter architecture for SEFDM are then presented in 32nm CMOS, based on a signal generation algorithm which employs the FFT. Reconfigurable implementations for adaptable bandwidth compression ratios are also considered.

The research described in this thesis was largely completed at the sponsor company, ARM Ltd. Incorporated in 1990, Advanced RISC Machines (ARM) is the world's leading semiconductor Intellectual Property (IP) supplier. The ARM business model was the first to target the design and licensing of IP as opposed to selling manufactured ICs. Over 20 billion ARM based ICs have been shipped, as of 2011, making the ARM 32-bit microprocessor architecture the most widely used in the world. ARM was spun off from Acorn Computers Ltd., with investment from VLSI Technology and Apple Computer [11].

1.2 Thesis Organisation

Recent trends in IC manufacturing technology are further elaborated from the designer's perspective in Chapter 2, describing the challenges of worst case design for power constrained applications. The emerging difficulties of parametric variability effects are discussed, including recent trends regarding process technology, supply voltage noise and reliability concerns. A survey of previously published approaches to adaptive techniques is then presented, with a focus on DSP-related applications.

Chapter 3 starts to explore the application of timing-error detection and mitigation to DSP datapaths. The design concept of a novel FIR filter algorithm is presented that exhibits robustness to intermittent timing-errors. To illustrate the concept, a layout macro is implemented in 90nm CMOS technology, with detailed analysis from SPICE simulation demonstrating compelling power reduction.

In Chapter 4, a generalised approach to timing-error tolerance for arithmetic datapaths is developed. The concept is based on the manipulation of path delays, such that timing violations result in arithmetic errors of bounded magnitude, which are subsequently analysed in a similar fashion to quantisation noise. A statistical model is developed that links Signal-to-Noise Ratio (SNR) and timing-error rate. FIR and DCT macros are presented in 32nm CMOS process technology to explore and illustrate the concept.

A new extremely low overhead approach to mitigating timing-errors, through the targeted use of time borrowing techniques is proposed in Chapter 5. Timing-error detecting transparent latches are used to permit time borrowing in order for timing violations to resolve without resulting in logic errors. The latches are used selectively in order to prevent excessive buffering due to hold time violations. A novel control approach is developed and FIR and FFT macros are presented in 32nm CMOS technology.

Chapter 6 presents a departure from the preceding work, with a shift in focus away from the challenge of margin elimination for power efficiency, to consider power efficiency of future communication systems with improved spectral efficiency. The design and implementation of an SEFDM baseband transmitter is presented in 32nm CMOS technology. After comparing signal generation algorithms for the SEFDM signal, a number of VLSI architecture optimisations are presented, along with a newly designed approach for bandwidth reconfigurability, comparing circuit area and power dissipation against conventional Orthogonal Frequency Division Multiplexing (OFDM) implementations. The work in this chapter was in collaboration with UCL doctoral students Marcus Perrett and Safa Isam.

Finally, Chapter 7 summarises the work in this thesis and discusses the significance of the proposed techniques, while also giving a feel for the potential for industrial exploitation.

1.3 Contributions

The main research and engineering contributions of this thesis are summarised below:

- Application of Razor circuit-level error detection techniques with error correction achieved through an algorithmic approach. Developed a novel FIR filter algorithm for timing-error tolerance that is suitable for filters with arbitrary impulse responses (Chapter 3). Implemented an FIR macro in 90nm CMOS technology.
- Developed a new approach for timing-error tolerance in arithmetic datapaths, which modifies path delay using a novel carry-merge adder (Chapter 4). Demonstrated by design of FIR and DCT macros in 32nm CMOS. Derived a statistical formulation of SNR as a function of the timing-error rate.
- A new approach for timing-error tolerance that makes use of time borrowing to recover correct results (Chapter 5), introducing the concept of a Razor latch. The approach is supported by the design of FIR and FFT macros in 32nm CMOS.
- Developed a hybrid Razor/canary based supply voltage control scheme (Chapter 5) to address the increased demands placed on the control loop in replay-free schemes.
- Presented the first study of the implementation of an SEFDM transmitter. The study includes analysis of implementation trade-offs with a number of signal generation algorithms, before presenting the design of a number of novel VLSI architectures for fixed and reconfigurable bandwidth compression. Designs are presented for various configurations of baseband transmitters in 32nm CMOS.

1.4 Publications

This research has resulted in the following peer reviewed conference and journal contributions:

1. P. N. Whatmough, I. Darwazeh, “On the Performance of Timing-Error Tolerant Programmable FIR Filters,” *London Communications Symposium*, 2009.
2. P. N. Whatmough, I. Darwazeh, D. M. Bull, S. Das, D. Kershaw, “A Robust FIR Filter with In Situ Error Detection,” *IEEE International Symposium on Circuits and Systems*, pp. 4185-4188, 2010.
3. P. N. Whatmough, I. Darwazeh, “Robust Digital Signal Processing for Wireless SoCs”, *London Communications Symposium*, 2010.
4. P. N. Whatmough, S. Das, D. Bull, I. Darwazeh, “Error-Resilient Low-Power DSP via Path-Delay Shaping,” *IEEE/ACM Design Automation Conference*, pp. 1008-1013, 2011.
5. P. N. Whatmough, M. Perrett, S. Isam, I. Darwazeh, “VLSI Architecture for a Reconfigurable Spectrally Efficient FDM Baseband Transmitter,” *IEEE International Symposium on Circuits and Systems*, pp. 1688-1691, 2011.
6. P. N. Whatmough, I. Darwazeh, “A Reconfigurable Spectrally Efficient FDM Baseband Modulator,” *London Communications Symposium*, 2011.
7. P. N. Whatmough, S. Das, D. M. Bull, I. Darwazeh, “Selective time borrowing for DSP pipelines with hybrid voltage control loop,” *IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 763-768, 2012.
8. P. N. Whatmough, M. Perrett, S. Isam, I. Darwazeh, “VLSI Architecture for a Reconfigurable Spectrally Efficient FDM Baseband Transmitter,” *IEEE*

Transactions on Circuits and Systems I: Regular Papers, invited, pp. 1107-1118, 2012.

9. P. N. Whatmough, S. Das, D. M. Bull, I. Darwazeh, “Circuit-Level Timing Error Tolerance for Low-Power DSP Filters and Transforms,” *IEEE Transactions on VLSI Systems*, to appear in 2012.

1.5 Patent Applications

The research in this thesis has resulted in the following US patent filings, made on behalf of the author:

1. P. N. Whatmough, D. M. Bull, S. Das, “Sensing Supply Voltage Swings Within an Integrated Circuit,” US Patent Application, 2012.
2. P. N. Whatmough, D. M. Bull, S. Das, “A Data Processing Apparatus and Method Using Monitoring Circuitry to Control Operating Parameters,” US Patent Application, 2011.
3. P. N. Whatmough, D. M. Bull, S. Das, “Delay Monitoring Circuit Calibrated by Razor Error Detection,” US Patent Application, 2011.

Chapter 2. Adaptive Voltage Scaling for DSP Applications

Canonical static CMOS digital logic has a number of distinct advantages, which have resulted in it being the dominant digital circuit style. The regenerative output has a logic level swing that is not dependent on relative device sizes but is instead equal to the supply voltage, which along with the CMOS high input and low output impedances, gives rise to remarkably high noise margins [12]. It is well known that the supply voltage, V_{dd}, of static CMOS circuits is a key parameter to the digital designer, as it allows us to trade-off switching speed ($\propto C_{eff}V_{dd}I_d^{-1}$) with a quadratic reduction in dynamic power consumption ($\propto C_{eff}V_{dd}^2$) for a given effective switched load capacitance, C_{eff}, and drain current, I_d. The power saving incentive of reducing V_{dd} is so strong that a range of techniques have been developed in an attempt to overcome the associated reduction in switching speed. In particular, the micro-architectural techniques of pipelining and parallelism, which essentially allow us to trade circuit area for increased speed and throughput, have become an important part of the digital design repertoire [13].

In this chapter, a number of themes central to this thesis are introduced. Parametric variability effects are described, considering how manufacturing process variation, supply voltage noise and reliability concerns influence IC design in sub-micron CMOS technology. The power consumption overhead of static worst-case voltage margins are discussed, before introducing the concept of adaptive Dynamic Voltage Scaling (DVS) schemes to address static margins. The remainder of the chapter is a literature review of timing-error detection and correction techniques, focussing on DSP applications.

2.1 Introduction

Supply voltage scaling is a popular approach to reduce power dissipation in digital static CMOS circuits. However, scaling the supply voltage of static CMOS reduces the signal swing, which results in two effects. Firstly, the internal noise of the system is reduced, since lower charging currents lead to reduced cross talk and supply voltage noise. Secondly, the design becomes more sensitive to external noise sources that do not scale. In the context of a large System-on-Chip (SoC), there are many distinct macros on the same IC, each of which is a significant noise source strongly coupled through supply and signal routing, the implied reduction in noise margins starts to look very unattractive. Therefore, a balance is required between noise margins and power efficiency.

The main focus of this thesis is to design circuits with reduced power dissipation, achieved through modulating supply voltage. An alternative technique to tune speed and power dissipation is to tune the threshold voltage through the body effect. The technique of Adaptive Body Bias (ABB) has been widely studied and even used commercially in older technology generations [14][15]. However, the body effect diminishes with technology scaling, which renders ABB increasingly ineffective [16]. Also, Dynamic clock Frequency Scaling (DFS) is not explicitly considered in this work. Instead, it is assumed that the clock frequency has already been minimised for the given application and cannot be reduced further.

2.2 Parametric Variability Effects in Digital CMOS Circuits

IC design has always been subject to Process, Voltage and Temperature (PVT) variations which make it impossible at design time to determine exactly how a circuit will perform. To cope with these sources of variation, the concept of worst-case (WC) margin has been a mainstay of the design process. The following is a brief review of the most significant current trends in parametric variability.

2.2.1 Manufacturing Process Variation

Recent generations of IC process technologies have exhibited increasing process variation effects, with ever widening distributions for key parameters such as transistor width (W) and gate length (L); carrier mobility (μ); oxide capacitance (C_{ox}); oxide thickness (t_{ox}); threshold voltage (V_t) and metal interconnect resistance (R_{wire}) and capacitance (C_{wire}). It is often the case that the control of minimum-sized features does not generally track feature scaling itself. For this reason, the relative device and interconnect variations tend to increase with minimum feature size scaling. In short-channel devices, V_t is one of the most poorly controlled parameters, with 3σ variations on the order of 30% or more of mean [17]. The sources of variation include Random Dopant Fluctuations (RDF), Line Edge Roughness (LER) and oxide thickness variation [18]. Unlike analogue designs, which tend to avoid poorly controlled minimum-sized devices [19], digital circuit cells make extensive use of minimum-sized devices to curtail circuit area, and are thus strongly affected by the relative increase in variation effects.

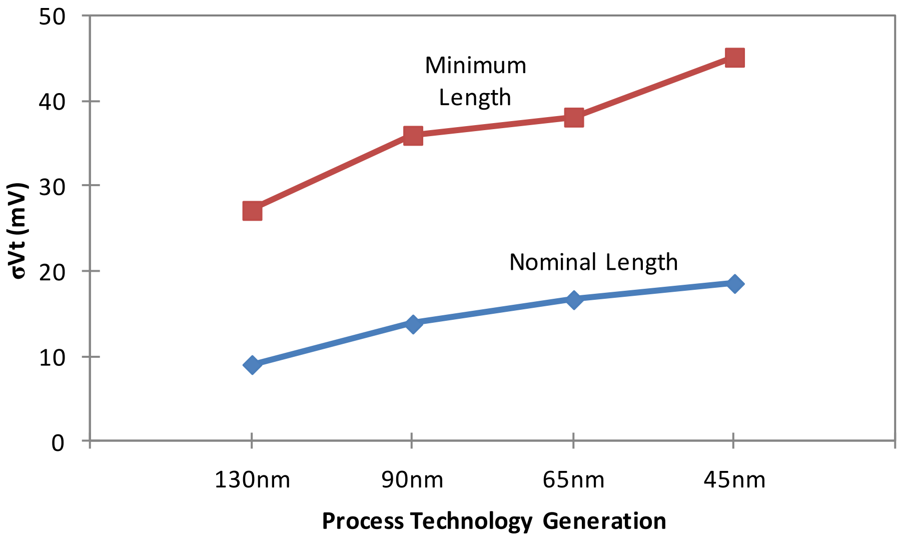


Figure 2.1: Variation of parameter Vt is poorly controlled and increasing with continued technology scaling. Adapted from [20], where the actual length of "minimum" and "nominal" devices are proprietary and not disclosed.

Figure 2.1 shows how process scaling has led to progressively worse control of V_t over successive generations. Of course, since each new technology generation seeks to lower the target (mean) V_t, the relative variation ($\sigma V_t / \mu V_t$) increases rapidly. In a high performance 45nm process[3], a minimum sized device with $\overline{V_t} =$ 250mV has a σ/μ of approximately 20% [20]. Much of this process variation is in fact systematic, however, as the complexity of mask design for sub-wavelength resolution lithography increases, it is becoming increasingly difficult to separate the systematic effects from those that are truly random and hence they must be lumped in with the latter.

2.2.2 Supply Voltage Variation

Relentless scaling of CMOS technology has resulted in a rapid increase in the number of devices integrated on a single die. Although supply voltages have

[3] The choice of threshold voltage has become such as strong trade-off between sub-threshold conduction and switching speed that many recent process nodes offer multiple variants to support different applications. These are typically either high-performance, high-leakage (often denoted "G" or "GP") or lower-performance, low-leakage (denoted "LP").

dropped, due to this increased integration, power budgets have largely remained constant or increased slowly[4]. This has resulted in an increase in chip supply current. As supply voltage decreases and current increases, the supply grid impedance must drop with a squared scaling factor in order to maintain a fixed percentage noise budget. While advances in packaging technology, namely flip-chip packages, have helped minimise the contribution of the IC package to the grid impedance, power supply noise has become an issue even for digital logic circuits [12]. A high-performance microprocessor in a 1V, 90nm technology may consume as much as 100A of supply current, which for a 10% noise budget demands a supply grid impedance as low as 1mΩ [21]. Achieving this at GHz frequencies is extremely challenging. Power gating and clock gating further exacerbate the situation as they increase the peak-to-average ratio of supply current. It is often the case that subtle interactions of power gating and/or clock gating events trigger the most severe inductive droop events. This type of interaction on an SoC is often very difficult to analyse during design time, especially when there are multiple Central Processing Unit (CPU) cores that will eventually be executing software that may not have been written yet.

In recent years, there have been various attempts to address the issue of power supply noise at the circuit level, such as on-chip regulation [22], and through process technology developments, such as area-efficient decoupling capacitors [23]. However, excessive decoupling is expensive in terms of circuit area and gate leakage currents, while on-chip regulation with good efficiency and low output noise remains extremely challenging for the high load currents required of a large digital circuit.

[4] This is true for energy constrained battery-power devices and also thermally limited applications such as desktop and server CPU products

2.2.3 Reliability Concerns

With the aggressive scaling of CMOS geometries, a number of reliability, or aging phenomena, have become more prominent. The effects can be significant under normal operational conditions and include mechanisms such as Bias Temperature Instability (BTI), Hot Carrier Injection (HCI) and Time-Dependent Dielectric Breakdown (TDDB). Of these, BTI and HCI stress have become major reliability concerns in digital circuit design [24].

BTI stress effects were initially observed when PMOS devices were subjected to negative (static) bias stress at elevated temperature, causing an increase in V_t over time. More generally, any transistors subject to low duty cycle gate voltages may experience a shift in V_t over their lifetime [25]. BTI is often a concern with elements of a design which are subject to strict delay values, yet may remain at a given logic state for extended periods, such as heavily gated clock buffers. HCI stress is a result of electron trapping near the drain region. It causes a degradation of the electrical parameters when the device is switching [25]. These effects used to be considered to be a process engineering issue, but as the mechanisms become unavoidably more prominent and increasingly difficult to screen for during manufacturing test, they are increasingly starting to emerge as an issue to be tackled by designers at the system level. To this end, a number of aging degradation sensors and adaption techniques have been described in the literature [26].

Another key reliability concern is referred to as Single Event Upsets (SEUs) [27]. These are typically attributed to alpha particle strikes or the influence of cosmic rays, but could equally be due to signal integrity problems such as inductive or capacitive crosstalk. The susceptibility of a circuit to an SEU depends on the energy of the incoming particle or (noise event) and the location of the strike [27].

The minimum electron charge required to flip the quiescent state of a digital circuit node is referred to as the critical charge, given by $Q = CV_{dd}$, where C is the capacitance of the node and V_{dd} is the supply voltage. IC process scaling directly aims to reduce both of these quantities and hence, reliability concerns due to SEUs have become an increasing concern [28]. This is especially true in applications such as server infrastructure, which make use of such vast quantities of CPU and Dynamic Random Access Memory (DRAM) ICs that even statistically low SEU rates can result in a steady stream of logic errors. Safety critical applications such as automotive and those operating in harsh environments such as space or particle physics experiments are also effected by SEUs. In many cases, SEUs have been directly addressed with some form of redundancy and checking, such as the use of an Error Correcting Code (ECC) on data before transmission over a bus fabric or storage in a Random Access Memory (RAM) [29].

While reliability issues are not directly addressed in this work, they are a strong motivation for the use of error tolerant design techniques for their own sake. The timing-error detection techniques presented in section 2.4 are capable of detecting delay faults in general, including those due to aging and SEUs. Also, it is implied that these mechanisms will represent an increasing contribution to design margins as process technology geometries continue to scale.

2.3 Limitations of Static Design Margins

Margining is the name given to the process of determining suitable design constraints given performance, power consumption, yield and robustness specifications. Static margins are included at design time and cannot ordinarily be influenced post-silicon. A key problem with WC margins is that they must enable the design to meet conflicting requirements of maximum clock frequency, power dissipation and robustness over PVT corners while achieving sufficient yield to meet the required profit margins. This presents a dichotomy as the PVT distribution widens, because fast chips will meet clock frequency requirements easily (but consume too much power), while slow chips may easily meet power dissipation specification but struggle to achieve the required clock frequency. In turn, considerations for robustness present similar difficulties, since minimisation of static margins is in fact a process of directly reducing supply noise tolerance.

As parametric variability increases, traditional WC design is forced to take account of increasing extremes of the performance distribution. In many cases, it is not clear which of an ever increasing number of PVT corners are indeed the worst case for analysis[5]. True WC conditions are often extremely rare combinations of complex interactions across an SoC, which are almost impossible to predict at design time using a design flow predominantly based on static analysis. Hence, as is oft stated, the conventional worst case design style leaves too much performance on the table.

It is, however, all too easy to come to the conclusion that worst case design should be eschewed entirely with a move to an alternative design style, such as one of the many variants of asynchronous logic [30]. Anecdotal evidence from the historical development of the commercial digital VLSI industry suggests this is unlikely to be the case:

1. The worst case design style has proven perennially successful at enabling incredible complexity to be handled through the use of Electronic Design Automation (EDA) tools.

[5] This is mainly referring to setup time analysis. It is common to more readily accept exaggerated hold time margins as they are essential to make the IC work at any clock frequency, whereas insufficient setup margins only limit maximum clock frequency. Nonetheless, excessive hold margins have a detrimental effect on circuit area and power consumption.

2. Efforts to embrace typical case performance at the circuit level, have been found to come at the cost of significant synchronisation overhead and have largely resisted repeated attempts at commercialisation[6]. A few niche successes, such as smartcard ICs are possibly the exception that proves the rule.

It is therefore likely that any shifts in design approach in response to escalating parametric variability issues will build upon traditional synchronous design styles.

A recent trend that helps break the limitations of WC margins is the use of post-silicon tuning. Each IC is measured during manufacturing test to determine the optimal supply voltage or body bias setting given the observed process strength [31]. The approach can also be extended to calibrate the optimal supply voltage with respect to temperature for a given die [10]. While this approach is very attractive, it requires a considerable amount of expensive testing time and demands careful selection of test patterns over which to perform the calibration. Hence, it is often too expensive for low-margin Application Specific Integrated Circuit (ASIC) products.

A further development of supply voltage tuning at test time is to perform tuning continuously, on-chip, while in functional operation. For example, the pseudo-synchronous approach of Razor [6] has been shown to allow very significant optimisation of parametric yield. The approach allows for tuning of supply voltage[7], in order to trade-off power consumption and clock frequency. Since robustness is treated as a separate concern, handled explicitly by an error correction mechanism, many limitations of WC margining are overcome with dynamic post-silicon tuning. The Razor prior art is considered in detail in the following section.

[6] A recent example is Handshake Solutions, a spin-off of a Philips Research project started in 1986. Handshake were started in 2004 and folded in 2010.

[7] Dynamic frequency scaling (DFS) is largely ignored in favour of voltage scaling alone, with the assumption that the clock frequency has been tuned as low as possible while supporting the computational throughput.

2.4 Adaptive supply voltage schemes

Dynamic voltage scaling[8] is a well-known approach to trade off performance and power consumption of digital circuits. DVS provides a means to minimise adaptively the worst-case supply voltage margin used to account for PVT variation, using a suitable feedback signal to close the control loop. Two standard approaches to generate this control information are “canary” monitoring circuits [32][33] and in-situ timing-error detection (“Razor”) [8]. Both approaches provide a control signal, derived on-chip, which tracks the operating point of a digital circuit. This observed operating point is statistically often significantly below the worst-case corner used at design time to meet setup time requirements and therefore accurate estimation can allow supply voltage reduction with an associated reduction in power consumption proportional to V_{dd}^2.

The canary circuit typically consists of a critical path replica, which is either fixed at design time, or composed of tunable elements [10]. The propagation delay through this replica path is then monitored while supply voltage (and/or clock frequency) is scaled, until the replica path fails to meet setup timing. The replica path can track global PVT variations on the die at low area and power overhead and with low disturbance to the design flow [10]. However, because such canary paths are typically present in just a few discrete locations on chip, they are unable to account for local effects such as intra-die process variation, local heating, local supply noise and noise coupling. Hence, a margin must be added to the canary path in order to ensure it fails before the main circuit it is intended to protect.

[8] The terms DVS and adaptive voltage scaling (AVS) are used somewhat interchangeably. Dynamic voltage and frequency scaling (DVFS), however, is considered a different technique that involves engineering discrete voltage/frequency tuples at design time.

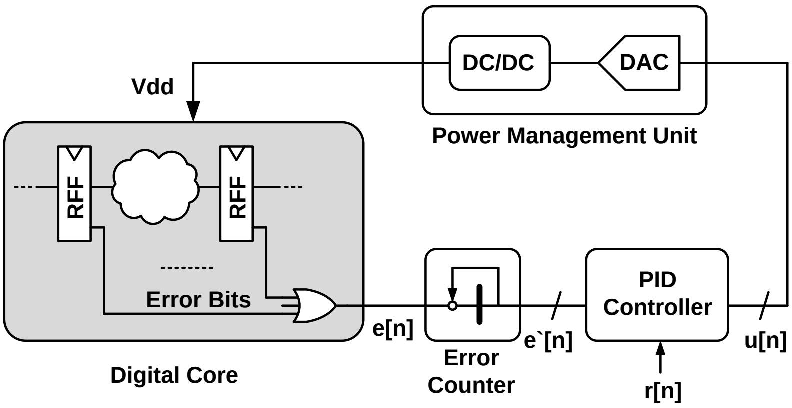


Figure 2.2: Closed-loop dynamic voltage scaling using timing-error rate feedback.

Razor overcomes this limitation using an in-situ approach to reduce the margins associated with the canary circuit [6]. A timing-error detecting (Razor) flip-flops are added to critical paths across the design and these are subsequently used to detect the on-set of timing-errors[9] while scaling supply voltage. Thus, static margins implemented to account for worst-case global and local PVT variations are minimised, leading to greater reduction in power consumption.

Figure 2.2 shows the closed loop control scheme conventionally used for Razor DVS. Razor Flip-Flops (RFF) are used to detect late transitions at critical path end-points, each generating a single error bit. These error bits are combined with a wide-OR gate, giving a global error bit flag, $e[n]$. A counter is used to integrate $e[n]$ over N cycles to give an error rate, $e'[n]$, which is compared with the target error rate set point, $r[n]$, before adapting the supply voltage using the supply voltage control variable, $u[n]$, which represents the new supply voltage demand. A power management unit, which can either be a separate IC or integrated on chip, is then used to generate a scalable supply voltage.

[9] The terms timing violation, timing error and Razor error are used interchangeably to refer to a detected transition at a FF data input during a predefined error detection window.

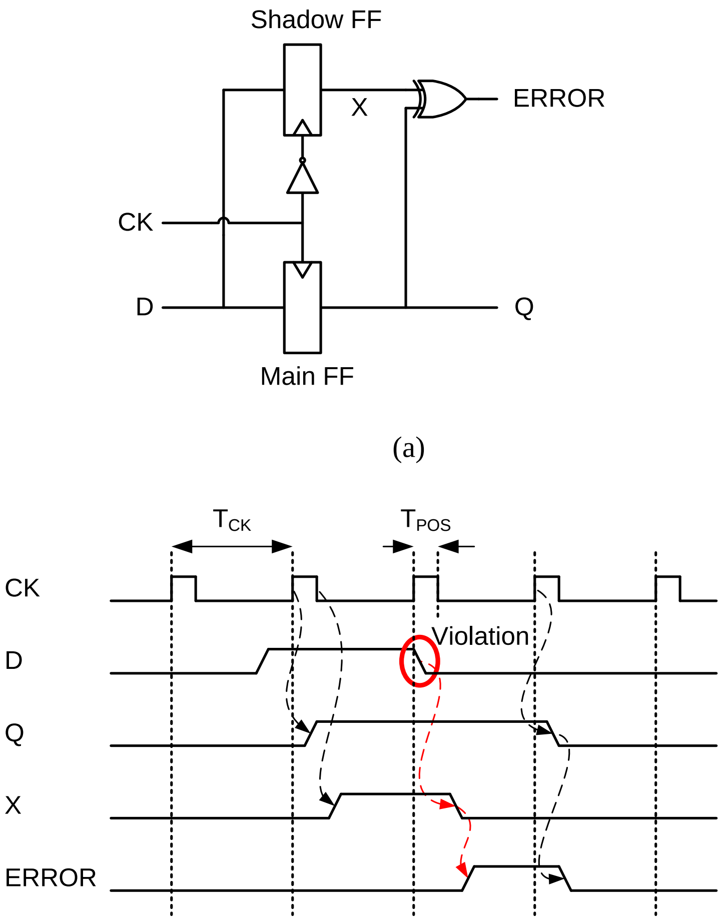
The timing-error detection capability allows the DVS loop to track the ideal operating voltage for a given error rate and hence removes margins normally included for PVT variation. This leads to an improvement in power consumption due to an almost optimal (rather than WC) operating voltage. However, this approach also leads to sporadic timing-errors on the critical paths and requires additional design effort in order to engineer the system to prevent the main circuit from failing.

2.5 Review of Timing-Error Detection

The Razor technique combines both timing-error detection and correction [6]. For the sake of clarity, the methods for detecting timing-errors are considered first, followed by a review of timing-error correction techniques in the following section. The goal of timing-error detection is to detect signal transitions during the setup and hold time window of a flip-flop. This can be achieved by at least two distinct approaches. A third approach to detecting (timing) errors based on various forms of redundancy will be discussed later in this chapter. In subsequent chapters, a number of different error detecting circuits are employed in different scenarios; some of the trade-offs are considered first in this section by way of introduction.

2.5.1 Double Sampling

The first approach is to sample the signal on the input data pin twice: once at the start of the setup and hold window and once at the end. The two samples can then be compared with an XOR gate in order to determine if the input signal has changed during this time, as shown in Figure 2.3. In the figure, the clock high phase (T_{POS}) determines the error detection window, with the first sample instance defined by the rising edge of clock signal CK, and the second by the falling edge.



(a)

(b)

Figure 2.3: Example of a timing-error detection flip-flop based on comparing two samples of the D signal: (a) simplified schematic and (b) diagrammatic timing waveforms.

This is a fairly simple approach which can be implemented with standard digital cells[10]. The additional Flip-Flop (FF) doubles the clock input loading, which is very unattractive for low-power applications. A more fundamental issue with double sampling is that it does not actually guarantee that there were no signal transitions during the setup and hold window, just that the input data signal was identical at the two sample instances. Hence, non-monotonic transitions (i.e. brief pulses that return to the original value before the second sample instance) cannot be detected by this

[10] At least in terms of the logic functions required. Realistically, the circuits need to be placed in the same cell in order to minimise wiring delays that may diminish the error detection window.

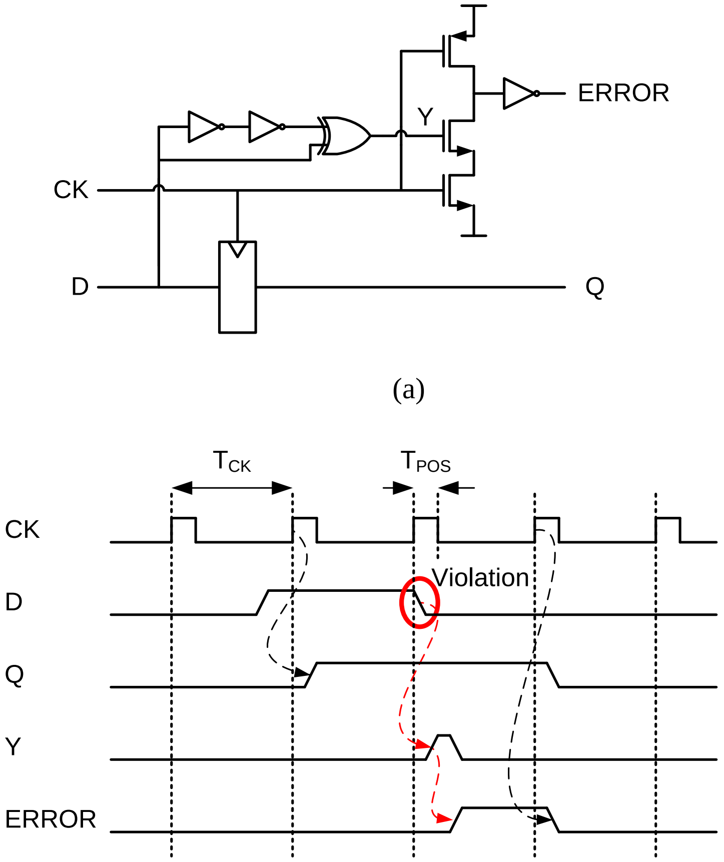
approach. The original RFF used a double sampling approach [7] and was also surveyed in [34].

2.5.2 Transition Detection

The second key approach is to incorporate a transition detector that is enabled during the setup and hold window. The transition detector is created with a simple dynamic gate and has an inherent advantage of being sensitive to arbitrary transitions (even pulses) during the detection window[11]. Figure 2.4 illustrates the basic operation of this scheme. A chain of inverters and an XOR gate are used to detect a transition of either polarity, generating a pulse at node Y, which discharges the dynamic node during when clock signal CK is low. Arguably, the requirement for a dynamic gate is a disadvantage as it requires more careful design and characterisation and is more sensitive to noise effects as compared to static logic, especially at advanced technology nodes [12].

Both styles of circuit require some form of reference that is equal to the detection window, which is typically related to the main flip-flop setup and hold time. The reference can be incorporated into the clock by making use of a pulse clock which has a high-phase equal to the detection window. Pulse clocks require careful design of clock distribution networks in order to ensure the pulse width is not degraded by uneven rise and fall times in clock buffers due to variations in PMOS and NMOS devices. Alternatively, an inverter-chain can be incorporated into the cell to generate a pulse of the required width. A detailed comparison of timing-error detection circuits is given in [34].

[11] Circuit design issues limit the minimum detectable pulse width, since the pulse can collapse in the inverter delay chain due to finite slew rate limitations.



(a)

(b)

Figure 2.4: Timing-error detecting flip-flop based on transition detection: (a) simplified schematic and (b) diagrammatic timing waveforms.

Introducing timing-error detection to a logic stage imposes an additional design consideration in the form of an increased hold timing constraint. The detection window is typically somewhat pessimistic and hence larger than the conventional setup and hold time for the FF. Generally, this can be overcome by padding any short paths with buffers at the cost of circuit area and power. Nonetheless, trade-offs between detection window size, hold time buffering and WC logic stage delay variation lead to a challenging optimisation for the circuit designer. This is perhaps in contrast to the aim of the Razor scheme to reduce the impact of dynamic variation.

2.6 Review of Timing-Error Correction

The detection of timing-errors can be used to achieve closed-loop control of supply voltage such that it tracks PVT variations. A side-effect of this approach is intermittent logic errors due to the timing violations. These logic errors must be addressed somehow at the circuit or system level to maintain correct operation. Having looked at the error detection problem in the previous section, the following is a survey of techniques from the literature which aim to provide an error correction mechanism for logic errors arising from low-voltage operation.

2.6.1 Razor

The Razor scheme combines circuit-level timing-error detection with micro-architectural error correction achieved through a replay mechanism. Initial implementations of Razor systems have focused on RISC microprocessors [8][9][10]. In the case of a microprocessor, when timing-errors are detected, speculative state within the processing pipeline is flushed and correct state is achieved by re-execution from a check-pointed golden state. The control mechanisms for achieving this replay are typically already present in a modern microprocessor in order to cope with conventional speculative execution [35]. Replay correction was generalised to a DSP system in [36], for the implementation of an accelerator for the Sobel image processing algorithm. In this example, functional units are decoupled using shift registers, such that when a timing-error is detected, a centralised controller can roll back the state in the shift registers, before recommencing operation from the last valid results. This gives a robust approach and the design process can be automated for high-level synthesis. However, the full benefits of voltage scaling cannot be realised with this approach, since the power dissipation of the shift registers represents a significant overhead.

There exist many applications for low-power, high performance digital circuits, that heavily datapath dominated, with little control, where the cost of additional control logic to achieve check-pointing and replay in the fashion of a microprocessor would be prohibitive. In addition, explicit recovery cycles due to timing-errors adversely impacts instantaneous processing throughput, leading to variable computational latency that can be difficult to tolerate for many real-time systems. Avoiding replay entirely, yet retaining robust operation in the face of timing-errors, is a very attractive goal in these applications and is the main ambition for the research in this thesis. The inherent noise robustness of many DSP algorithms suggests that there may be a more efficient approach to error correction in this domain. In the following section, a brief review of significant literature in this area is outlined following this approach.

2.6.2 Algorithm-Level Timing-Error Detection and Correction

A number of elegant approaches have been proposed that indeed avoid explicit replay for DSP circuits in the presence of timing-errors. This is typically achieved by allowing intermittent logic errors to occur in some limited or controlled fashion. The algorithms and/or circuits must then be adapted to mitigate the performance impact of transient timing-errors, such that algorithmic performance degrades gradually as the timing-error rate increases.

The Algorithmic Noise Tolerance (ANT) approach, originally developed by Hedge and Shanbhag in 1999 [37], seeks to design DSP datapath circuits whereby some property of the timing-error statistics are known by design. Statistical signal processing techniques inspired by the communications field are then used to exploit the known statistics of the output signal in order to detect timing-errors amongst correct output samples. This is achieved by using some form of statistical estimator to predict the current output sample. Approximate error detection is achieved by comparing the predicted output sample with the noisy sample against an error threshold and when this is exceeded, approximate error correction is achieved by replacing the sample with the predicted output. More specifically, the techniques of linear prediction [38], reduced-precision redundancy [39] and error cancelation [40] have been developed in order to arrive at a low-cost approximation of the current output sample, even in the presence of intermittent errors. This approximation is subsequently used for both error detection and correction. The concept has been well-developed as a framework and applied to a number of DSP applications, including FIR filters [38], FFT [39], Viterbi decoders [41] and motion estimation [42].

In the case of ANT, the essential error rate feedback mechanism (i.e. error detection), is performed by ensuring timing-errors are of large magnitude which is achieved by using ripple-carry arithmetic topologies, forcing timing-errors into the Most Significant Bits (MSBs). In fact, the ripple-carry circuit is also key to the error mitigation approach, since it ensures timing-errors are strongly data dependent and hence exhibit suitable correlation properties with the input signal in the time domain. The use of ripple-carry circuits potentially limit not only performance, but also energy-efficiency, as it leads to slow unbalanced logic stages which require a higher supply voltage for a given throughput as compared to faster balanced arithmetic circuits, such as parallel prefix adders [55]. In addition, there is often significant overhead for the additional statistical estimator and decision blocks. This aspect is not well studied in the literature, where power savings are often related as the savings of the proposed design at scaled voltage relative to the same design at nominal voltage, instead of making reference to an optimised baseline implementation. The following sections provide a brief review the most promising ideas in this vein.

2.6.2.1 Linear Prediction Based ANT

The prediction based ANT technique exploits the correlation between successive output samples of a narrowband DSP algorithm [38]. Hence, a linear predictor can produce an estimate, $y_e[n]$, of the output of the algorithm, $y_0[n]$. The output of the linear predictor is then compared to the current output sample and a simple threshold function is used to produce hard decisions on the reliability of the current output sample. The accuracy required of the estimator is limited by the fact that the timing-errors (when present) are concentrated in the MSBs of the sample, due to the exclusive use of ripple carry adders, and are therefore large in magnitude. The estimator block can therefore have a relaxed precision and general complexity compared to the main DSP block. Approximate error detection is achieved by monitoring the difference between the estimator output and the main DSP block output $(y_0[n] - y_e[n])$, with an error flagged when this exceeds a predetermined threshold. On detection of an error, approximate error correction is performed by using the predictor output sample for $y'[n]$, instead of the noisy $y_0[n]$ sample, as shown in Figure 2.5. The correction is described as approximate because it is subject to the estimation error between the correct result, $y[n]$, and the estimator output (i.e. $y[n] - y_e[n]$).

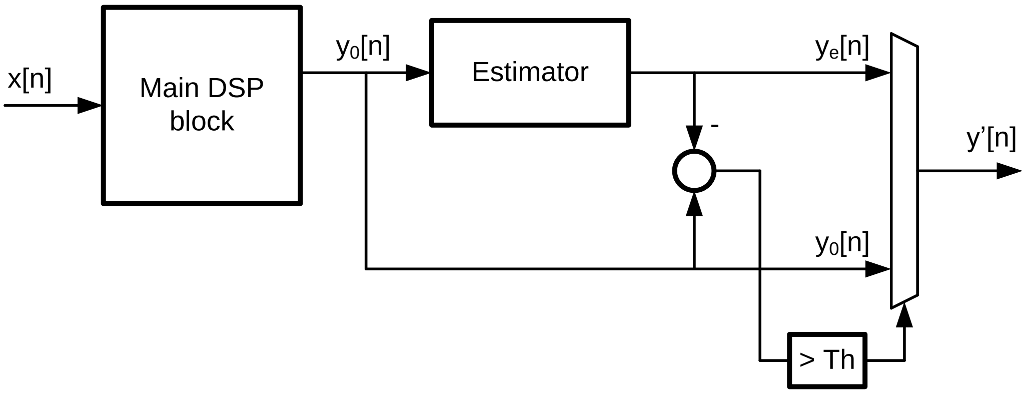


Figure 2.5: Prediction-based ANT scheme.

The use of a linear predictor for error detection presents a number of constraints:

1. The estimator block should have significantly lower logic depth than the main DSP block in order to prevent timing-errors in the estimator itself.
2. The frequency of errors occurring in the main DSP block should be sufficiently low to prevent errors accumulating in the state of the predictor.
3. In order for the error detection to be reliable, the accuracy of the estimator must be greater than the smallest possible timing-error magnitude.

The last two constraints together represent a significant bilateral constraint, because increasing the order of the predictor gives lower estimation error, but at the same time, this requires estimation over a larger window of samples, which increases the chance that one of the samples used for estimation contains a timing-error. In practice, this problem is solved at the circuit level, by using ripple-carry arithmetic to ensure timing-errors are in the MSB positions only. This is explored further in Chapter 3, along with some issues relating to guaranteeing MSB errors. Linear prediction ANT is suitable for algorithms that produce successive output samples that are highly correlated, such that one sample can be estimated from its neighbouring samples. As such, the main application studied to date is narrowband filtering [38].

2.6.2.2 Redundancy based ANT

A DSP system with Reduced Precision Redundancy (RPR) ANT is shown in Figure 2.6. The basic premise is that a replica of the DSP logic is designed with significantly reduced precision such that its critical path delay is less than that of the main DSP block [39]. Hence, it will operate at lower voltage than the main DSP block. The output of the RPR block, $y_r[n]$, can thus be used to detect timing-errors in the output of the main block, $y_0[n]$, whereupon the replica sample is chosen as the output for the system. Designing a RPR replica DSP function with significantly reduced critical path length is possible for ripple-carry adders and multipliers, because the critical path length is linearly dependent on the operand precision. When a timing-error is detected, the main DSP block output sample is replaced with the RPR output sample, leading to a decrease in the system SNR, due to the quantisation noise introduced by the reduced precision in the RPR estimate. The impact of this quantisation noise on the SNR depends on the precision of the RPR block relative to that of the main DSP block and the frequency of timing violations.

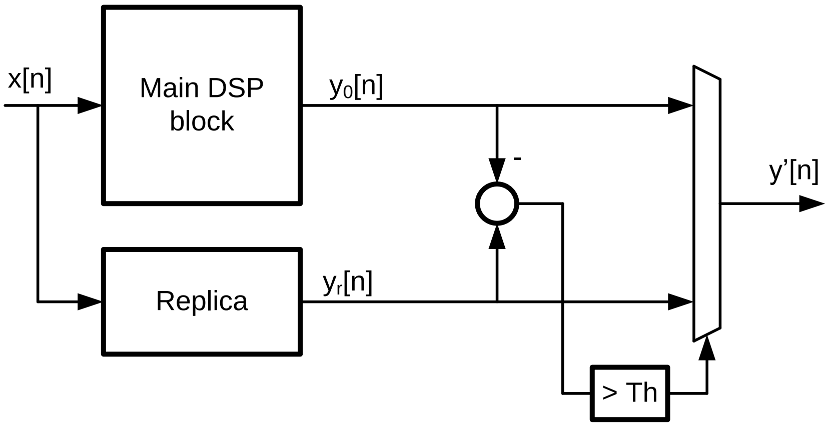


Figure 2.6: Reduced-precision redundancy (RPR) scheme.

The RPR ANT approach is readily applicable to a range of DSP algorithms and has been studied in the context of filters and transforms [39] and in a more developed form has been applied to Viterbi decoders [41] and motion estimation [42]. RPR ANT is based on a redundant datapath, albeit with reduced precision, which has an associated circuit area and power consumption overhead which is not well quantified in the literature. The power consumption of the redundant datapath is critical to achieving an overall power reduction at a reduced supply voltage, relative to a well-designed implementation at nominal voltage.

2.6.2.3 Error Cancellation Based ANT

It has been proposed that adaptive filters could be applied in the ANT framework to cancel strongly data dependent timing-errors which exhibit a deterministic dependence on the input signal [40]. The cross-correlation between the input signal and the output of the main DSP block is used to cancel spurious timing-errors, as illustrated in Figure 2.7. The error cancellation filter can be adaptively calibrated by the well-know Least Mean Square (LMS) algorithm. Such a calibration is commonly used in many practical adaptive systems and could consist of an auto-calibration phase during power up. During the calibration phase, a predefined input signal is passed through the main DSP block and a pre-computed error-free output signal is used as the desired signal. When the tap vector has converged via the LMS algorithm, the calibration is complete and the error signal is subtracted directly from the main DSP block output signal, thereby cancelling the soft errors. The calibration would then be repeated if significant change in supply voltage or temperature was observed, or if the calibration is performed continuously, the system will track environmental changes automatically.

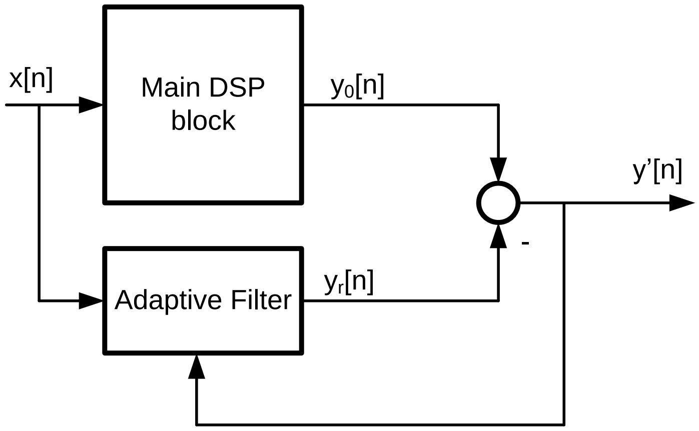


Figure 2.7: Adaptive error cancellation scheme.

This approach has the limitation that delays in the circuit will constantly change in real time as voltage and temperature conditions vary and therefore the cancellation loop must have sufficient bandwidth to adapt to this. The energy overhead associated with the calibration phase should be taken into account when calculating power saving. As with other ANT techniques, the additional circuit blocks are of significant size; their power consumption must be weighed against the savings achievable from reducing the supply voltage. Error cancellation ANT has been applied to an FIR filter in [40].

2.6.3 Algorithm-Architecture Optimisation

Significance Driven Computation (SDC) is an alternative approach employing algorithm-architecture transformations to engineer tolerance of timing-errors for filters [43], 2D DCT [44] and colour interpolation [45]. The approach is based on identifying the most significant computations in the DSP algorithm given specific metrics relating to output signal quality, before reassigning these critical computations to paths with sufficient timing slack such that the probability of timing-errors is low, relative to the remaining paths. In the case of fixed-value multipliers, this variation in path length for different coefficients is achieved by decomposition of the coefficients into sub-expressions which are then combined as required, leading to addition of a smaller number of sub-expressions for more important coefficients. Consequently, as supply voltage is scaled (or operating frequency increased) longer paths begin to fail timing compared to shorter paths leading to a gradual degradation of algorithmic performance with supply voltage. This approach does not offer an intrinsic error-detection mechanism, which needs to be addressed separately with a canary-style circuit. A related approach is presented in Chapter 5, with more relaxed requirements for path length control.

2.7 Conclusions

This chapter has outlined the goal of achieving increased power efficiency by reducing parametric static design margins while maintaining a focus on robustness. After describing some of the key delay variability trends, the limitations of static margining supply voltage were examined, with the conclusion that it is very difficult to optimise power efficiency for a given maximum clock frequency without negatively impacting noise margins, i.e. the system is Pareto optimal. As reliability concerns are currently a pressing issue due to the increasing prevalence of BTI, HCI, SEUs and power supply noise, there no concessions to be made for noise margins.

Timing-error detection and correction approaches, pioneered by the well-known Razor scheme, have the potential to break the limitations of design-time margining, by separating out reliability as a separate concern at run time. There are two aspects to this approach. Firstly, the detection of timing-errors is used to provide a feedback signal to perform closed-loop modulation of the supply voltage in order to track the optimal supply voltage for the given prevalent PVT conditions. Secondly, on detecting a timing-error, it is corrected at the cost of some additional latency, resulting in the system being tolerant of a wide range of delay variation phenomena, while generally retaining a simple synchronous timing model.

The Razor scheme has been mainly explored in the context of microprocessors, but is readily extended to DSP systems. The review of the literature in this area outlines how DSP systems, unlike microprocessors, are inherently robust to timing-errors and therefore offer greater power savings. ANT schemes exploit this property in various elegant ways, but it is apparent that performing error detection at the algorithm level is a heavy burden. An apparent difficulty with many of the reviewed approaches is the reliance on redundancy and slow ripple-carry arithmetic, which translates into overhead in terms of maximum clock frequency, circuit area and power dissipation. Clearly, it is necessary to keep this overhead to an absolute minimum in order to reduce PVT margins relative to a well designed baseline implementation. Many of the published approaches are do not address this point appropriately.

The research undertaken in the subsequent chapters is focussed on combining circuit-level timing-error detection with truly low-overhead error correction approaches, which explicitly avoid redundancy. In addition, clear analysis is presented for all proposed techniques, as compared to a fair conventional baseline. Another important aspect of the research detailed in the following chapters is a rigorous simulation approach using device-level SPICE simulation of fully placed and routed designs with annotated parasitics. In the next chapter, many of these issues are discussed in further depth by presenting analysis of an FIR filter macro incorporating a new error correction approach.

Chapter 3. Approximate Timing-Error Correction in FIR Filters

The previous chapter outlines some limitations of existing timing-error tolerance approaches, such as an overreliance on expensive redundancy techniques, poor suitability to wideband systems and generally unclear ultimate power savings. In this chapter, issues in the context of FIR filters are considered, with a novel architecture that mitigates sub-critical timing violations as they occur in the pipeline structure by momentarily bypassing affected coefficients to prevent errors reaching the output. Timing violations are detected using known in-situ circuit-level techniques based on late transition detection at timing end points. The approach enables operation with a small but non-zero logical error rate, such that process, voltage and temperature margins can be eliminated without compromising stop-band attenuation.

An implementation is presented in 90nm CMOS process technology using a typical commercial standard cell implementation flow and verified using full model SPICE simulations. The filter operates at a maximum clock frequency of 420 MHz at 1 V, with an estimated area and power overhead of 26% and 24%, respectively, compared to a conventional implementation. At the typical process and temperature corner, the proposed architecture can be scaled in voltage down to the point of first failure at 730 mV, thereby achieving a 53% power saving, with no detectable degradation in stop-band attenuation characteristics. The research in this chapter was presented at the IEEE International Symposium on Circuits and Systems (ISCAS) [46].

3.1 Introduction

FIR filters are a key class of DSP functions. Efficient implementation in terms of silicon area and power consumption can be challenging for high-throughput programmable FIR accelerators, since they require many parallel Multiply-ACcumulate (MAC) operations. For DSP applications, the requirements on maximum clock frequency are often modest compared to other domains such as general purpose computing. However, power consumption is often critical, particularly for battery-operated devices. As Deep Sub-Micron (DSM) CMOS geometries scale, PVT variability is greatly exacerbated which impairs power efficiency, since a higher supply voltage is required to safely combat delay variation. This higher supply voltage ensures that the worst-case circuit delay due to PVT variation does not result in timing violations which jeopardise correct operation. In addition, it is unlikely that any ICs will ever be subject to the worst-case parametric variation for which they are margined conventionally. Hence, the designer is forced to make concessions for a worst-case scenario that may rarely occur in practice. For low-power designs, there are significant gains to be made by providing circuit robustness using alternative methods to excessive voltage margin [47].

There is considerable interest in DVS for low-power DSP systems, as reviewed in Chapter 2. In particular, timing-error correction for the FIR filter has been studied in the following forms:

1. Linear Prediction ANT Scheme, which seeks to estimate output samples in order to perform error detection and correction [38]. Key limitations of this approach are significant redundancy, limited maximum clock frequency due to use of ripple-carry arithmetic, and poor suitability to wideband signals.
2. Reduced Precision Redundancy ANT, which uses a redundant pipeline with reduced precision to provide an estimate of the output, which is used for error detection and correction [39]. Although this overcomes the narrowband limitation of linear prediction, it still leads to overhead due to the redundancy and the use of ripple-carry arithmetic.
3. Noise Cancellation ANT, which uses an adaptive filter approach to cancel timing-errors, assuming they are strongly correlated with the input signal [40].
4. The variation tolerant scheme in [43] splits coefficients into groups of increasing significance, before arranging their accumulation in the inverse order to their significance. This results in timing-errors occurring first in less significant coefficients giving a soft degradation in filter performance. The same effect cannot be achieved with programmable filters with arbitrary impulse responses.

The ANT techniques, which were discussed in Chapter 2, seek to exploit the fact that for arithmetic operations constructed of ripple-carry adders, the propagation delay for each output bit increases monotonically with the bit order. Ensuring this condition in the context of a commercial standard-cell DSM design presents a number of concerns at the implementation level:

1. Arithmetic circuit architecture: ANT implementations do not have free choice of arithmetic circuit topology and are instead restricted to ripple-carry architectures at the final stage before a register. Faster structures such as the lookahead topologies can generate the critical carry signals in $\mathcal{O}(log_2N)$ time instead of $\mathcal{O}(N)$. Although such structures also have a greater gate count and therefore greater physical capacitance, the increase in speed implies they will have timing slack relative to the slower ripple-carry architecture and hence can run at a lower supply voltage for the same performance. Since reducing the supply voltage brings a quadratic reduction in dynamic power consumption, the use of a lookahead adder is generally attractive low-power design.
2. Dominant net delays: For DSM processes, net delays can equal or exceed cell delays. Net routing may require additional design effort to preserve the required delay-imbalance which is introduced with the ripple-carry topology.
3. Environmental variability: Circuit delay is not uniquely determined by input data patterns. Local environmental variability effects such as intra-die process variation and local temperature variation as well as transient effects such as coupling noise and IR-drop compound the problem of guaranteeing critical paths at design time.
4. Input signal statistics: For many applications there is no assurance that the input signal continually exercises the full dynamic range and hence some critical paths may not be sensitised on a regular basis. This could lead to

failures in less-critical paths which are subsequently undetectable if they lead to logical errors that are not of sufficient magnitude.

5. Single Event Upsets: Timing violations can also be triggered by SEUs caused by ions or electro-magnetic radiation strikes, which can occur randomly at any circuit node.

To address these issues, algorithmic error detection is replaced in this work with a robust circuit-level technique that has been developed for general purpose microprocessor pipelines. The significant advantage of this approach is that it is not required for timing violations to result in MSB errors and therefore the designer has free choice of arithmetic circuit architecture and do not need to guarantee critical paths at design time. The ability to detect timing-errors allows a DVS system to tune the operating point to the critical supply voltage by maintaining a low but non-zero error rate, which is referred to as the Point of First Failure (PoFF). This enables us to eliminate PVT margin and track changes in environmental conditions while avoiding operation in a significantly sub-critical region which brings only a small incremental power reduction and an exponential increase in timing violations. In order to prevent intermittent timing violations from significantly degrading the filter transfer function, a simple but deterministic error mitigation technique is proposed.

3.2 Proposed VLSI design

In situ error detection is achieved in the proposed design using Razor flip-flops, illustrated in Figure 3.1. Razor flip-flops augment a conventional master-slave flip-flop with a transition detector [9] that operates during the high phase of a pulsed clock (T_{pos} in Figure 3.2).

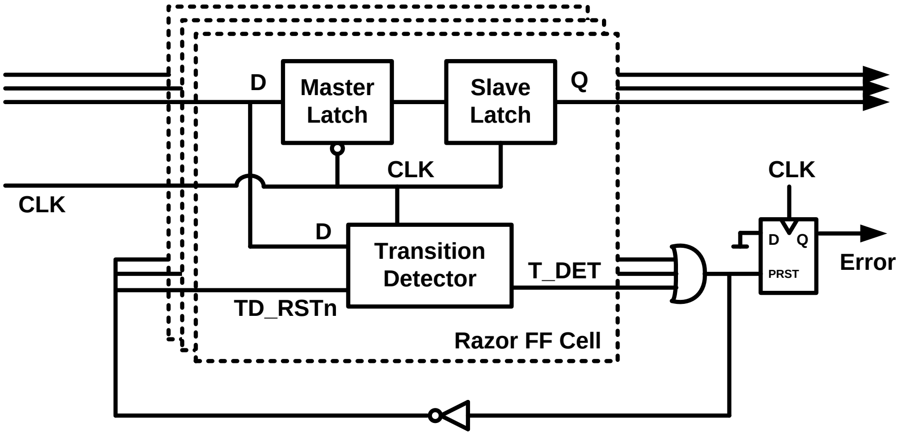


Figure 3.1: Self-resetting Razor flip-flop stage.

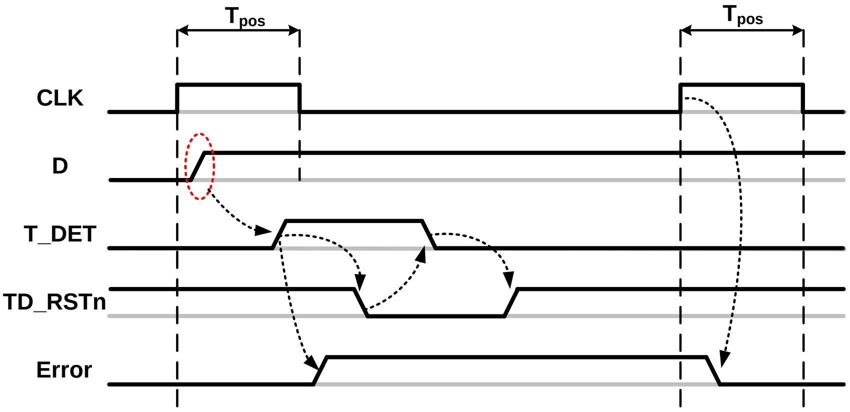


Figure 3.2: Timing of self-resetting Razor flip-flop.

This arrangement can detect late arriving transitions on the input D pin to the Razor cell and flag an error event, as illustrated diagrammatically in Figure 3.2.

The error pins for the individual bits of the pipeline registers are combined with a wide OR function to generate a single error bit for the whole register. This signal fans out to reset all the transition detectors ready for the next cycle and also drives the asynchronous preset pin of a flip-flop with D input tied to logic “0”. This holds the error event stable for the remainder of the cycle, such that it can be used in the subsequent error mitigation logic, bearing in mind that it is a late arriving event relative to the active clock edge.

Razor flip-flops are used to replace conventional flip-flops in the well-known transposed direct-form FIR architecture. Hence, there is a Razor flip-flop following every multiply-accumulate operation and a single-bit error flag that indicates if a timing-error has effected one or more bits of the pipeline stage. An additional benefit to this approach is some protection from SEU at the Razor flip-flop as well as in the combinatorial logic that fans into it [8].

The available options for recovering from a timing-error detected by the Razor pipelines are severely constrained in real-time DSP applications because variable latency is difficult to manage in the face of hard throughput deadlines. It is therefore required that the error recovery mechanism does not introduce additional latent cycles. Our proposed approach adds logic to each pipeline stage such that the individual multiply-accumulate operations, isolated by Razor flip-flop stages, prevent an erroneous tap contribution into the adder chain by bypassing the stage output using a mux and a delay register. Due to the fact that all filter taps are likely to process dissimilar input operands in any one cycle, it is unlikely that more than one tap will experience a timing violation per cycle at the critical operating point and hence the intermittent reduction in filter performance is limited.

This approach also ensures that for a given probability of error (P_e), the worst-case algorithm performance is largely deterministic, an important consideration at the system design level. Without error-mitigation, erroneous tap results, which by nature are often large in magnitude, will propagate into the pipeline, corrupting subsequent correct results further down the pipeline. This represents a modification of the FIR algorithm such that

$$y[n] = \sum_{k=0}^{N-1} \begin{cases} h_k x[n-k], & e_k = 0 \\ 0, & e_k = 1 \end{cases}, \tag{3.1}$$

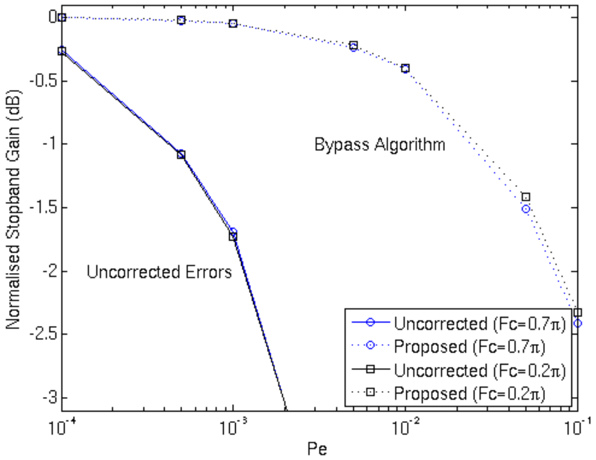


Figure 3.3: Stopband degradation as a function of Pe for two FIR bandwidths. The uncorrected errors are generated using random sign-bit inversion.

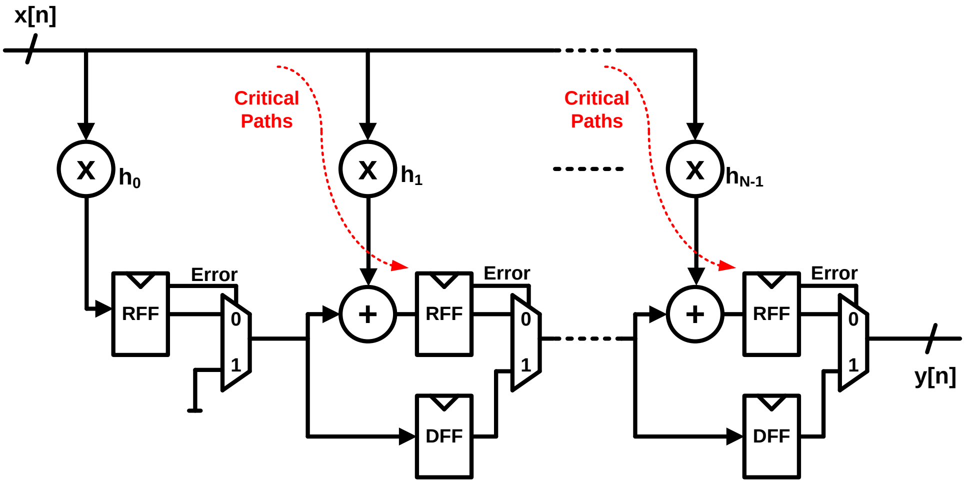


Figure 3.4: Proposed filter structure with timing-error mitigation.

where e_k is a 1-bit flag that indicates the detection of an error at the k^{th} Razor pipeline stage and $x[n]$, $y[n]$ and h_k represent the input signal, output signal and coefficients, respectively. Where h_k is symmetric, it is necessary to bypass both of the equal coefficients in order to maintain phase linearity while mitigating errors. The resulting noise process is equivalent to white iterative randomised sampling of the FIR response, which is described in detail in [48]. Figure 3.3 shows the degradation in normalised stopband gain with this approach as a function of P_e for two FIR filters, one wideband and one narrowband.

The proposed approach of (3.1) gives degradation of less than 0.5 dB for error rates below 0.01, which is a reasonable operating point [9]. The performance is also not strongly dependent on filter or signal bandwidth as we do not rely on correlation properties between samples. Figure 3.4 shows the proposed VLSI architecture. The critical paths through the multiply-accumulate operators are illustrated with red arrows, where “DFF” refers to a conventional library flip-flop and “RFF” indicates a Razor flip-flop. The modifications create a secondary critical path group from the late-arriving mux select through the adder to the next razor flip-flop, which must be suitably constrained to achieve sufficient timing slack.

Hold time constraints are an important consideration with Razor implementations since early arriving transitions that reach a Razor flip-flop during the high phase of the clock will trigger a false error detection event. However, in the proposed architecture this is not an issue, since there are no significant fast paths through the arithmetic logic. Since the coefficients are programmable in our design, symmetric folding or hardwired coefficient multipliers are not employed.

3.3 Simulation Results and Discussion

The proposed architecture was applied to a 16-tap FIR filter in a 90nm CMOS process. The implementation employs 10-bit coefficients, 8-bit input data words and a 20-bit adder chain. The two’s complement arithmetic implementations were chosen freely by the synthesis tool resulting in a delay-optimised Booth Wallace implementation with carry-save representation between the multiply and sum operations. No effort was made beyond a typical timing-driven implementation flow to optimise arithmetic implementations in order to reduce probability of exercising long paths [49] or optimise individual coefficient error rates [43].

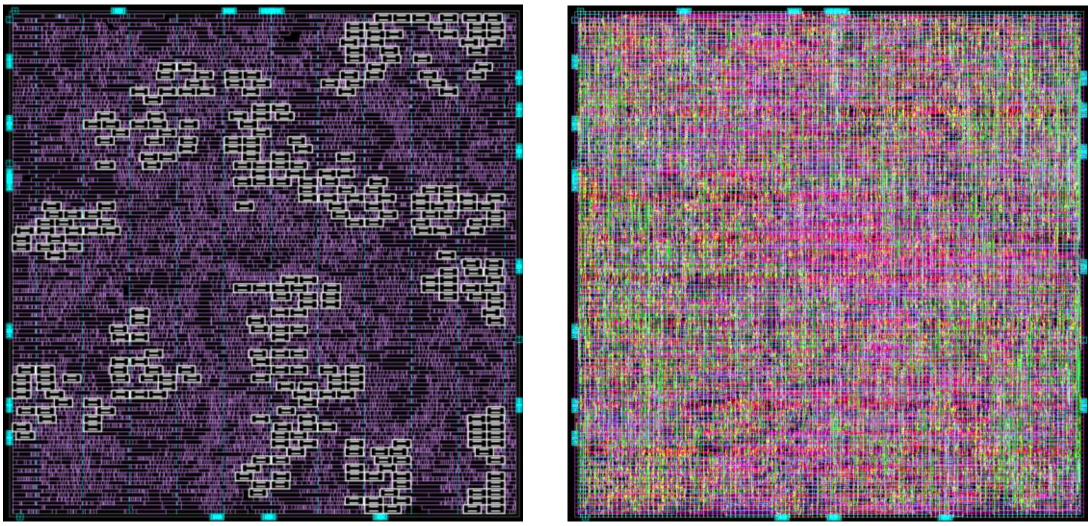


Figure 3.5: Standard cell layout (left), with double-height Razor flip-flop cells in white and with full metal stack (right). Design area is 0.084 mm^2.

There is an area and power overhead for a Razor flip-flop compared to an equivalent library flip-flop. The area overhead per bit is approximately double. Further, the proposed architecture requires an additional mux and flip-flop stage for each filter tap. Total area and power overhead as compared to a conventional transposed direct-form implementation are estimated to be 26% and 24%, respectively, at the nominal supply voltage. Our implementation conservatively uses Razor flip-flops on all bits of the pipeline registers, but depending on application, this could potentially be relaxed somewhat by using a mixture of razor flip-flops for the MSBs and library flips-flops for a number of LSBs, presuming sufficient slack exists as margin. This would greatly reduce the overhead of the error detection at the potential cost of robustness. The total area of the layout is 0.084 mm^2 (of which 60% is combinatorial logic and 40% registers), as shown in Figure 3.5.

Post-layout SPICE simulation with extracted parasitics was used to evaluate the proposed architecture over a range of supply voltage scaling conditions with an otherwise typical environment (TT process, 25°C). The coefficients used for the simulations are for a symmetric low-pass response with normalised cut-off frequency, $\omega_c = \pi/2$ radians/sample. 10,000 input vectors, consisting of uniform noise samples with maximum amplitude of 0 dBFS, were used to test the filter amplitude response up to the Nyquist frequency. The minimum clock period at the slow corner was found using conventional static timing analysis to be 2.4 ns (420 MHz). This clock period was kept constant while the supply voltage was scaled down from the process nominal of 1 V. The algorithmic performance of the proposed filter is gauged using a measure of stop-band rejection. Stop-band rejection is conventionally defined as the attenuation (from pass-band) to the top of the first side-lobe of the amplitude response. However, this metric is inaccurate in our case since the amplitude response becomes somewhat distorted in the presence of logic errors. Therefore, a modified approach is employed, to calculate the stop-band attenuation, η, as the ratio of pass-band power to stop-band power, both of which are defined as integrals of the power spectral density, $\Phi(\omega)$;

$$\eta = 10log_{10}\left(\frac{\int_0^{\omega_c}\phi(\omega)d\omega}{\int_{\omega_c}^{\pi}\phi(\omega)d\omega}\right). \tag{3.2}$$

This gives an averaged measure of frequency selectivity, which is appropriate for describing algorithmic performance.

Results presented in Figure 3.6 and Figure 3.7 indicate a 53% power saving from 28.62 mW at 1 V (full PVT margin) to 13.41 mW at 730 mV, which is the PoFF (proposed zero margin operating point); the reduction in η (3.2) is undetectable. Beyond this point, Pe increases by almost a decade per 10 mV reduction in V_{dd} and η subsequently degrades at 5.5 dB per 10 mV. As expected, this suggests that there is little to be gained from operating beyond the PoFF with the proposed architecture.

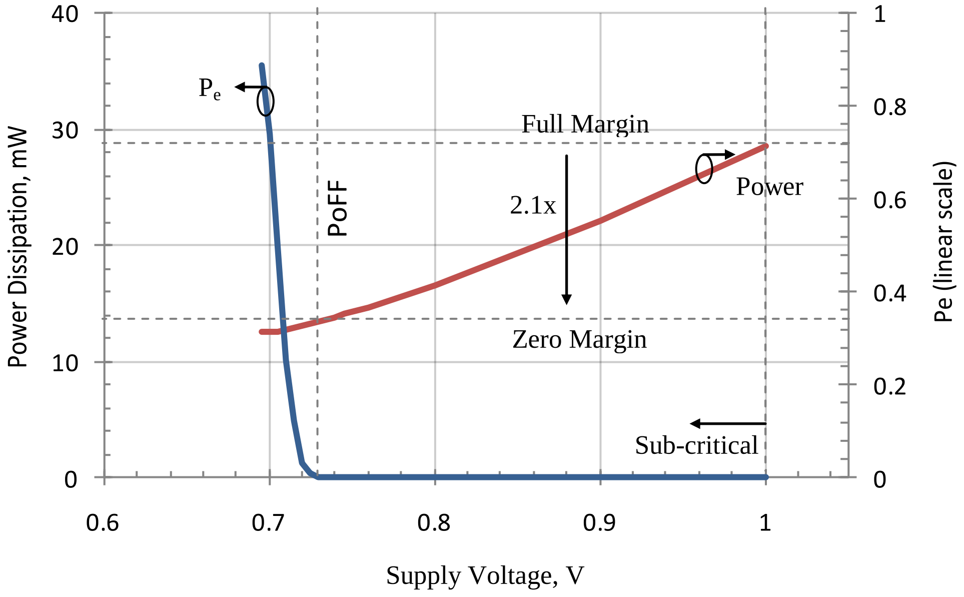


Figure 3.6: Power dissipation and error rate as a function of supply voltage.

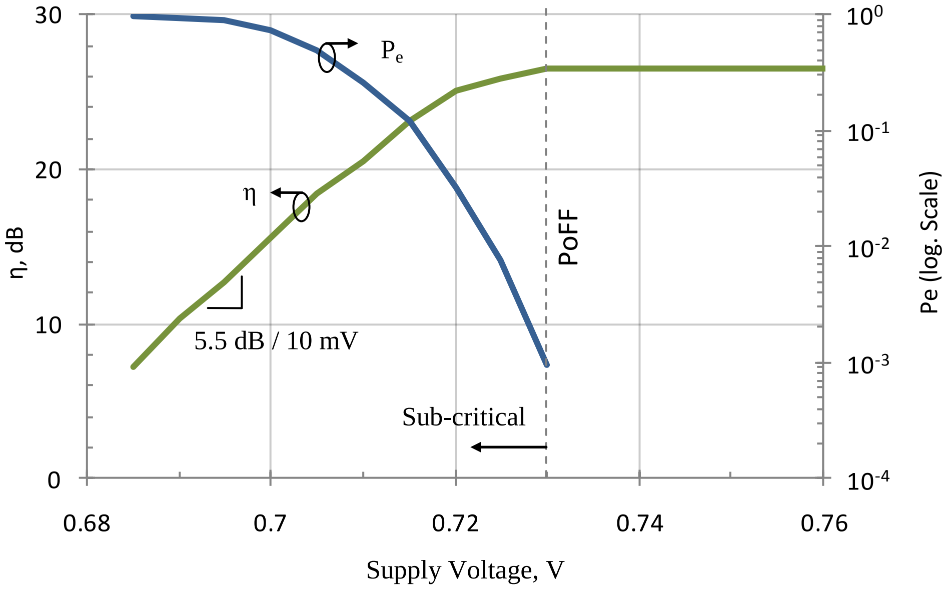


Figure 3.7: Stop-band attenuation and error rate as a function of supply voltage.

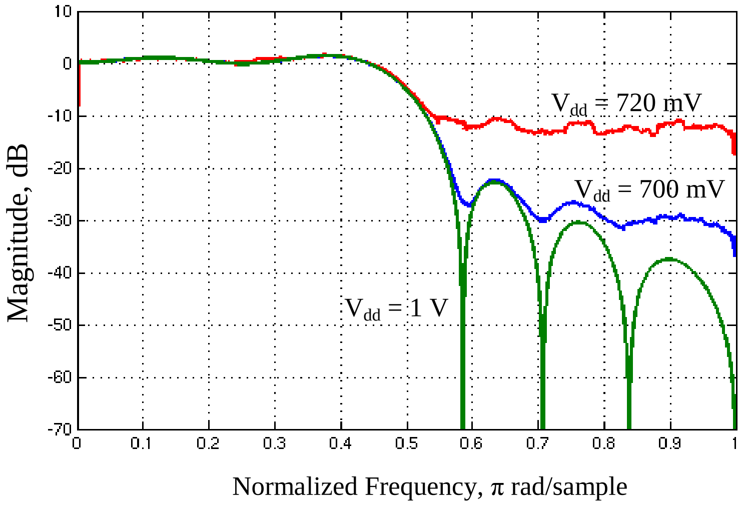


Figure 3.8: Amplitude response degradation at sub-critical supply voltage

Figure 3.8 shows the degradation in amplitude response shape at three supply voltages. With nominal V_{dd} of 1 V, P_e = 0 and η = 26.47 dB; at 720 mV, P_e = 3.2x10^{-2} and η = 25.08 dB; and at 700 mV, P_e = 7.4x10^{-1} and η = 15.5 dB. P_e and η are dependent on both the input data ($x[n]$) samples and the coefficients (h_k) and will therefore vary depending on application. Random stimulus was employed over the full input dynamic range in order to analyze robustness to the worst-case error patterns, since random data contains a disproportionately high number of sign changes which exercise the critical MSB paths in arithmetic logic. Consequently, many real-world signals would generate a significantly lower P_e, in turn leading to a more graceful degradation in η than seen here.

3.4 Conclusions

This chapter describes a novel FIR filter architecture incorporating in-situ error detection and mitigation for low-voltage operation. Unlike existing algorithmic error detection schemes (discussed in Chapter 2), this new architecture does not rely on predictable path delays that increase monotonically with bit order, or expensive redundancy, but instead uses a circuit-level technique to detect timing violations. This approach is thus much more easily realised given practical ASIC commercial design constraints. It is also well suited for wideband signals and does not rely on redundancy in order to correct errors, and as such was found to offer power saving of 53% in a 90nm CMOS process technology. The area and power overhead at nominal supply voltage compared to the transposed direct form is conservatively estimated to be 26% and 24%, respectively.

A drawback of the approach proposed in this chapter, is that it is only suitable for algorithms that can be realised using the sum-of-products formulation. While this is an extremely common operation, arguably the most important in DSP systems, there are other datapath algorithms that would not benefit from this approach. Moreover, a more generally applicable solution for arbitrary datapath arithmetic is attractive from the angle of eventually incorporating into EDA tools. Therefore, in the next chapter, a more general approach for mitigating timing-errors in arithmetic logic is considered.

Chapter 4. Approximate Timing-Error Correction by Path Delay Shaping

In the previous chapter, error mitigation was achieved by using the timing-error signal to momentarily adapt the pipeline structure to prevent logic errors contributing to the output sample. This is possible with FIR filters because the output sample is the accumulation of many weighted and delayed input samples and hence during the process of accumulation, it is possible to disregard erroneous intermediate results. The product-of-sums form is very popular in DSP datapaths, and is used extensively by commercial synthesis tools for generating arbitrary datapaths [50]. Nonetheless, the approach as applied to the FIR filter in the previous chapter is somewhat opportunistic and will not suit some other important DSP applications. Furthermore, the use of the timing-error signal from the Razor FF in the next cycle places additional timing constraints on the circuit design in order to prevent metastability issues.

In this chapter, the timing-error signal is not used for error mitigation, although it is still used to provide error-rate feedback to control a DVS loop, as before. A novel approach is proposed here to bound the magnitude of intermittent timing-errors at the circuit level. This is achieved by modifying the path delay distribution of the final carry-merge adder in each logic stage. Hence, timing violations lead to weakly correlated logical errors of small magnitude in a mean-squared-error sense. As distinct from the previous chapter, this proposed approach is largely suitable for any non-redundant arithmetic datapath.

This approach is examined in the context of an FIR filter and a 2D DCT implementation, in 32nm CMOS. Power saving compared to a conventional design at iso-frequency is 21 – 23%, at the typical corner, while retaining a voltage guard-band to protect against fast transient changes in switching activity and supply noise. The impact on minimum clock period is small (16 – 20%), as the design approach does not necessitate the use of ripple-carry adders. The impact on design effort is also minimal. The research in this chapter was presented at the IEEE/ACM Design Automation Conference (DAC) [51] and has also been accepted for publication in extended form in the IEEE Transactions on VLSI Systems (TVLSI), to appear in 2012 [52].

4.1 Introduction

Digital signal processing systems that make use of fixed-point number representations are subject to quantisation noise due to either rounding or truncation [59]. During system design, it is necessary to determine minimum word widths in order to trade circuit area and power consumption in the digital datapath for improved dynamic range and Signal-to-Quantisation Noise Ratio (SQNR)[12]. In many cases, the actual dynamic range requirements are subject to coincidental conditions relating to the signal being processed. For example, a wireless receiver

[12] Each additional bit in a fixed-point non-redundant number representation doubles the dynamic range, increasing SQNR by 6dB.

processing a clean modulated signal with no interferers, or a plain white digital image. Approximate DSP [53] was proposed to take advantage of this dynamic variation of signal processing, which is often strongly determined by the input signal. Sign extension detection and trimming is another example [54]. Equally, not every sample requires the full dynamic range. In other words, bit widths are chosen in a worst case fashion, which is often over dimensioned.

In the following work, circuits are designed which recast timing-errors are momentary reductions in number precision. Timing-errors are typically fairly intermittent, even at high average error rates. The reason for this is the path activation effect, which is discussed in a later analysis in this chapter. The intermittent nature of timing-errors and the worst case dimensioning of bit widths then results in a small degradation in SNR that is statistical in nature and related to the average error rate.

4.2 Delay Distribution of Datapath Circuits

A Razor DVS controller will intermittently allow the supply voltage to be scaled to until timing violations are detected. At this sub-critical operating point, the greatest logic path delay exceeds the clock period, and therefore a transition will not register correctly at the capturing flip-flop[13]. Therefore, the distribution of path delay in a given circuit is an explicit illustration of the logic end-points that are most susceptible to errors due to timing violations. To increase the robustness of such a circuit, the path delay distribution is analysed and later modified.

Arithmetic datapath circuits often exhibit relatively deterministic path delay characteristics. For example, carry-save arithmetic datapaths are considered, which allow a single carry-propagation to be shared amongst a number of arithmetic

[13] A simplified description of synchronous timing for illustrative purposes.

operations [55]. An arithmetic datapath pipeline stage would typically consist of a number of operators chained together. Such a stage can be efficiently implemented using carry-save transformations which reduce the number of costly carry propagations to one, which is positioned at the end of the stage before the pipeline register. In such an arrangement, the carry propagate adder dominates the delay imbalance[14] to each flip-flop or bank of flip-flops.

Two extreme cases of carry-propagate circuit topologies are considered, the Ripple-Carry Adder (RCA) and Kogge-Stone Adder (KSA) [56], which are pareto-optimal in delay and area. The KSA has minimum logic depth and fan-out, resulting in high performance and large area, whereas the RCA has minimum area and low performance. The following timing analyses show the path-delay histograms and distributions resulting from extensive Static Timing Analysis (STA) for each individual end-point of all paths in the RCA (Figure 4.1) and KSA (Figure 4.2) topologies from fully placed and routed in a 32nm CMOS process with full extracted parasitic. These results are plotted on identical axis for easy comparison.

The following are some general observations of the path delay distribution:

1. The critical path delay of the RCA (1.49 ns) is over three times that of the KSA (0.45 ns) and has nearly half the mean delay.
2. Both have critical paths in the MSBs; timing violations from sub-critical operation will generate errors of large magnitude, starting with the sign-bit.
3. The RCA has a very wide variation in path length, such that the fastest paths are many times shorter than the critical paths. Path activation can significantly change the critical path length for each pair of input operands.

[14] The difference between the longest and shortest paths in a given logic stage.

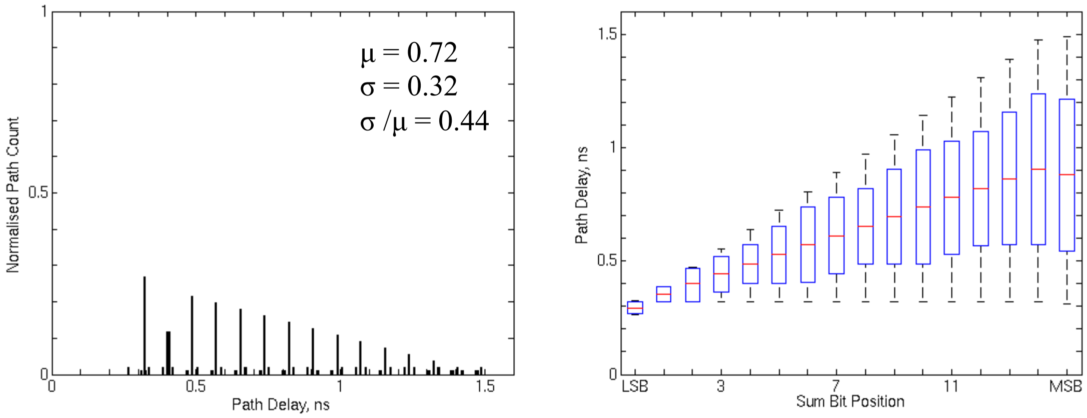


Figure 4.1: RCA path delay histogram (left) and distribution by bit position (right), with 1.49ns critical path.

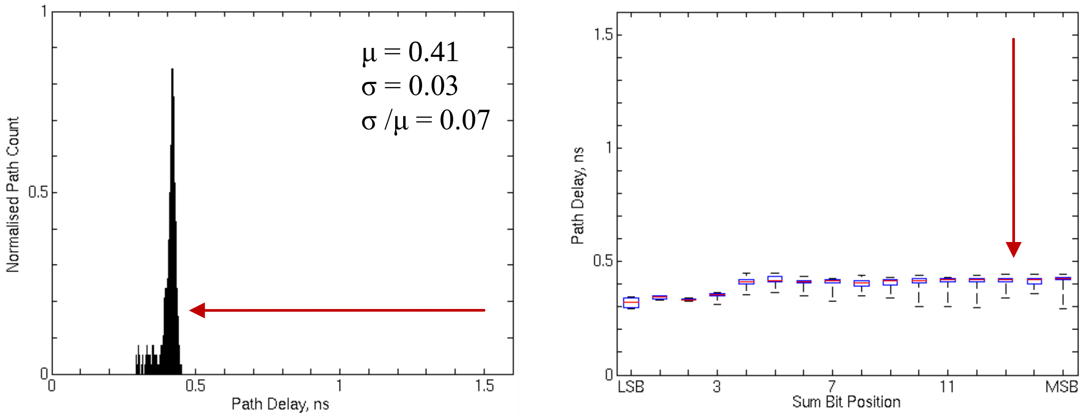


Figure 4.2: KSA path delay histogram (left) and distribution by bit position (right), with 0.45ns critical path. Red arrow indicates timing slack relative to RCA. Scale identical to Figure 4.1 for comparison.

This last point results in strongly data-dependent timing-errors in the RCA, associated with large changes in input signal magnitude and sign. The KSA circuit, however, has many critical paths with low standard deviation and therefore the data-dependency of timing-errors is much less pronounced.

Figure 4.3 shows the variation of path length for a 16-bit carry-propagate adder over a range of performance points achieved by varying both circuit topology and device sizing simultaneously. Clearly, the variation in path length is very small for fast implementations, while slower designs exhibit large variation in path length.

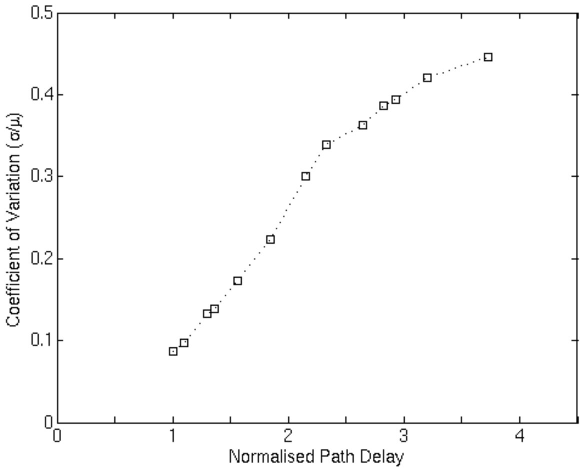


Figure 4.3: Fast arithmetic circuit implementations of a 16-bit adder exhibit low path delay variation.

Hence, with higher performance designs, there is very little signal dependent timing-error correlation because path delays are balanced to within a small range.

4.3 Path Delay Shaping

A novel timing-error mitigation technique is proposed, that is achieved using a simple two-level timing constraint to bound the path delay imbalance. This creates a bimodal path delay histogram, by adding a small tail of critical paths (for purpose of timing-error detection) to an otherwise balanced design. The additional tail contains only paths to registers in the Least Significant Bit (LSB) part of the stage output signal. The result of this is that timing-errors in these positions generate logic errors which are of small magnitude in a mean-squared-error sense. In this manner, a small amount of cycle time is traded for significantly increased robustness at low area overhead. Hence, that timing-error rate driven voltage scaling can be used to track the optimal operating point as environmental conditions vary, without explicit error correction. This technique is referred to as Path-Delay Shaping (PDS).

4.3.1 General Approach

Figure 4.4 shows a conventional combinational logic stage with critical path of td,max. To illustrate PDS, Figure 4.5 shows two path groups created by separating an N bit arithmetic logic stage into one group of M LSBs, which will be considered prone to timing-errors, and the remaining group of $(N - M)$ MSBs, which will be non-critical by design. The LSB group is intended to fail first; however, these end-points are not redundant. Instead, M is chosen such that intermittent timing-errors in this group do not cause an unacceptable reduction in system performance. A timing guard-band between the longest path to the LSB group end-points $(t_{d,max,LSBs})$ and the longest path to the MSB group end-points $(t_{d,max,MSBs})$ is created. In order to detect the timing-errors, RFFs are used to sample the LSB group results.

In this work, the timing guard-band between the two groups is achieved using a modified final-stage carry-merge addition graph, which employs a slower linear-delay segment in the LSB group and traditional fast graph for the MSB group. Tool-based device sizing is also employed, using two setup constraints, one for the critical LSB group and one for the non-critical MSBs.

The PDS approach relies on achieving a small guard-band between $t_{d,max,LSBs}$ and $t_{d,max,MSBs}$ across the design, in order to safely detect the onset of timing-errors. As in the previous section, in the case of arithmetic circuits, the carry-merge adder is responsible for the majority of delay imbalance and therefore only this circuit block is modified in order to adapt the path delay distribution. From an Register Transfer Level (RTL) description, conventional balanced datapath synthesis is used to achieve a high-speed implementation, before a modified carry-merge adder introduces the required degree of delay imbalance, as shown in Figure 4.6.

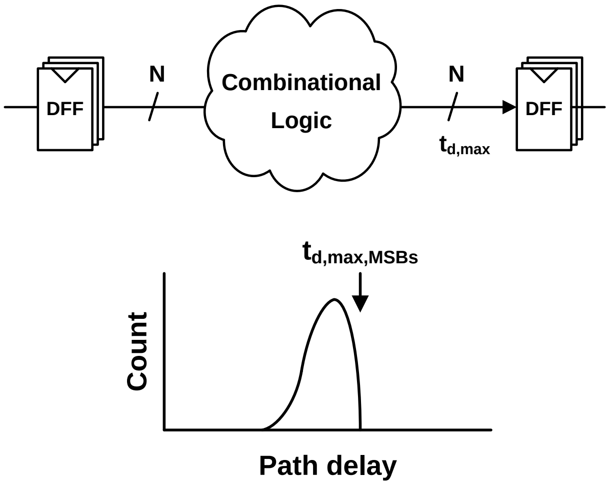


Figure 4.4: Conventional combinational logic stage with critical path length of td,max and associated diagrammatical path delay histogram.

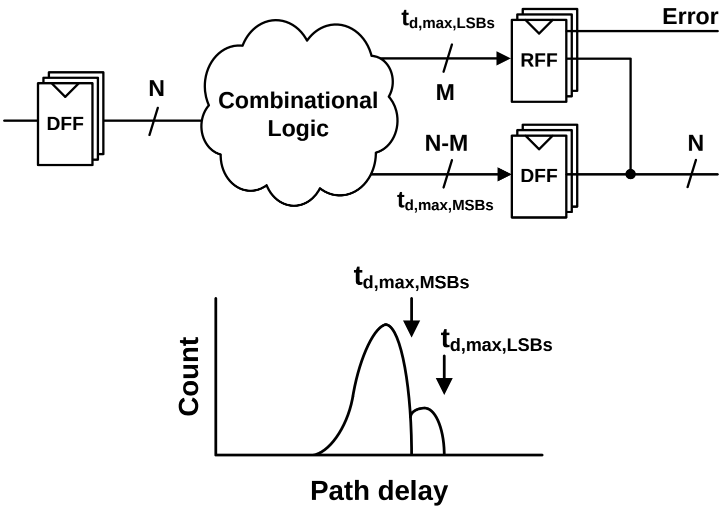


Figure 4.5: Illustration of PDS logic stage and corresponding diagrammatical slack histogram showing bimodal distribution.

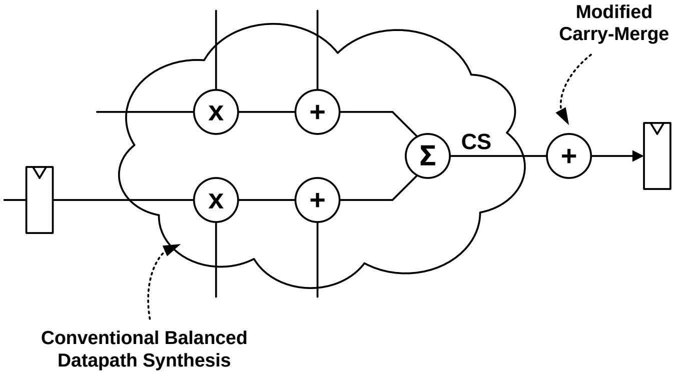


Figure 4.6: Illustration of PDS arithmetic logic stage, with additional path delay imbalance introduced using only a modified carry-merge adder.

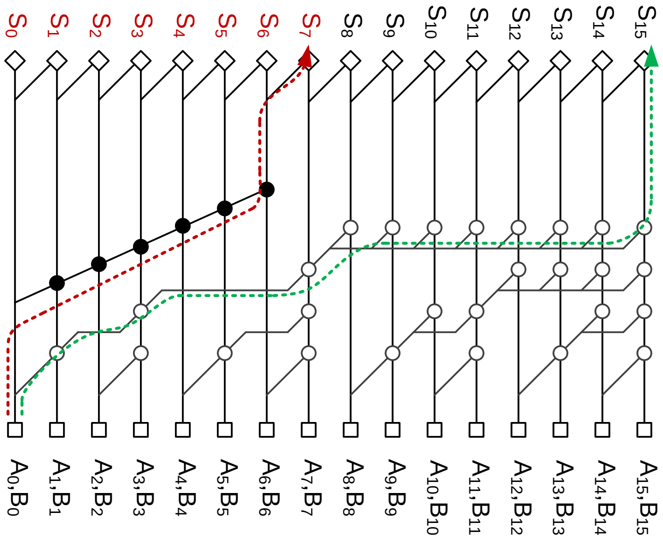


Figure 4.7: A hybrid ripple/Sklansky parallel prefix graph for $N = 16$, $M = 8$. Suitable for even bit arrival profiles.

The effect of timing-errors on well established adder topologies has been previously studied [57] in the context of DSP systems. However, specific optimisation for timing-error tolerance has not been previously considered. Our proposed modified carry-merge adder is based on a novel hybrid parallel prefix graph that combines two topologies in the same prefix network. An $(N - M)$ bit serial-prefix adder is used in the LSB position and has a chain-like structure that evaluates the carry in $\mathcal{O}(M)$ time. In the MSB position, a truncated N bit Sklansky tree is employed with a critical path of $\mathcal{O}(log_2 N)$ time. Combining the two structures such that $M \geq log_2 N$, results in a fast, generally balanced path delay profile with a small tail of critical paths due to the sum paths for the LSBs. Figure 4.7 illustrates the concept, where well-know logical construction is used for propagate-generate (□), dot-operator (●) and sum operator logic (◊) [56].

Where the carry-merge adder follows a multiplication, the input operands (A_i, B_i) are not quite of equal arrival time since the compressor tree following the multiplication is deeper in the centre than at either edge.

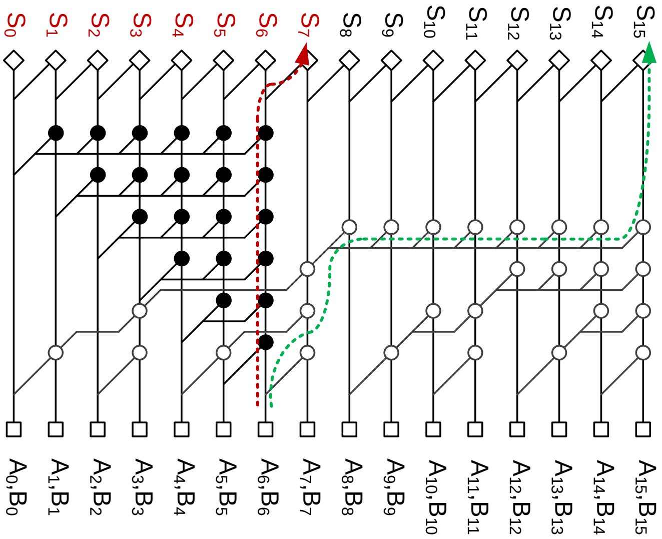


Figure 4.8: An adaptation of Figure 4.7 to show how skewed bit arrival times (often encountered with a partial product compressor tree) can be overcome by using a right-to-left serial-prefix structure in the LSB position.

This can effectively cancel out the effect of the ripple-carry chain. To address this situation, an alternate form of the serial-prefix algorithm can be used, as shown in Figure 4.8. By using a serial-prefix graph that operates from right to left, the critical path for the LSB group is ensured to start near to the centre, as opposed to from (A_0, B_0), which is the case with a conventional ripple-carry. Compared to a conventional Sklansky adder, the modified version requires additional dot-operators. The diagram illustrates the critical paths for the speculative (red arrow, six carry cells) and non-speculative end-points (green arrow, four carry cells).

The topology of Figure 4.7 was implemented in a 32nm CMOS process in order to examine the path delay distribution. The circuit was implemented from a gate-level netlist, along with a simple two-level timing constraint to maintain the intended timing relationship during Automatic Place and Route (APR). Figure 4.9 shows the path delay histogram and per sum-bit delay distribution for the proposed carry-merge topology.

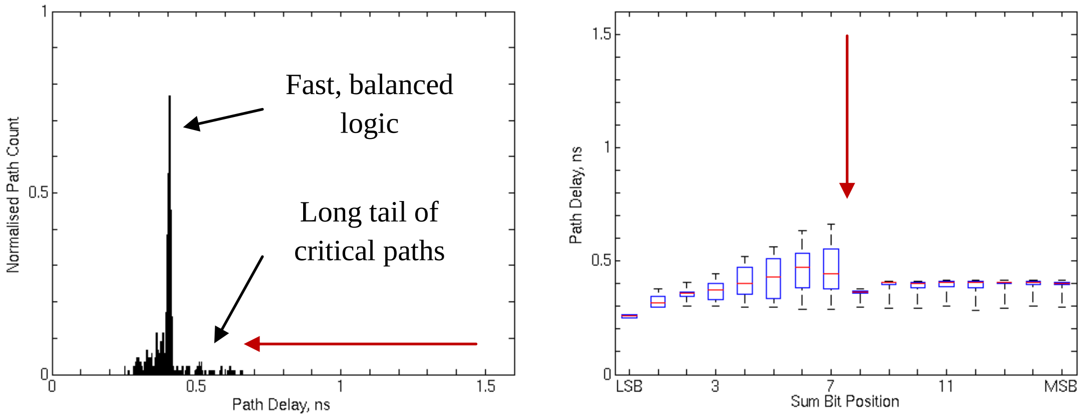


Figure 4.9: Hybrid RCA/Sklansky carry-merge adder path delay histogram (left) and distribution by bit order (right).

The results show a fast, generally balanced path delay profile with a small tail of critical paths due to the sum paths for the LSBs. Thus, the LSB paths start to fail first (with logic errors of bounded magnitude) and provide a timing guard-band over which to detect timing-errors before the MSB paths are compromised. Modern synthesis tools are able to generate similar topologies for an adder automatically given suitable RTL description and modified timing constraints that infer the LSB and MSB end-point groups. In practice, it is necessary to work at the RTL abstraction in this way to enable short design, implementation and verification cycles for VLSI digital systems.

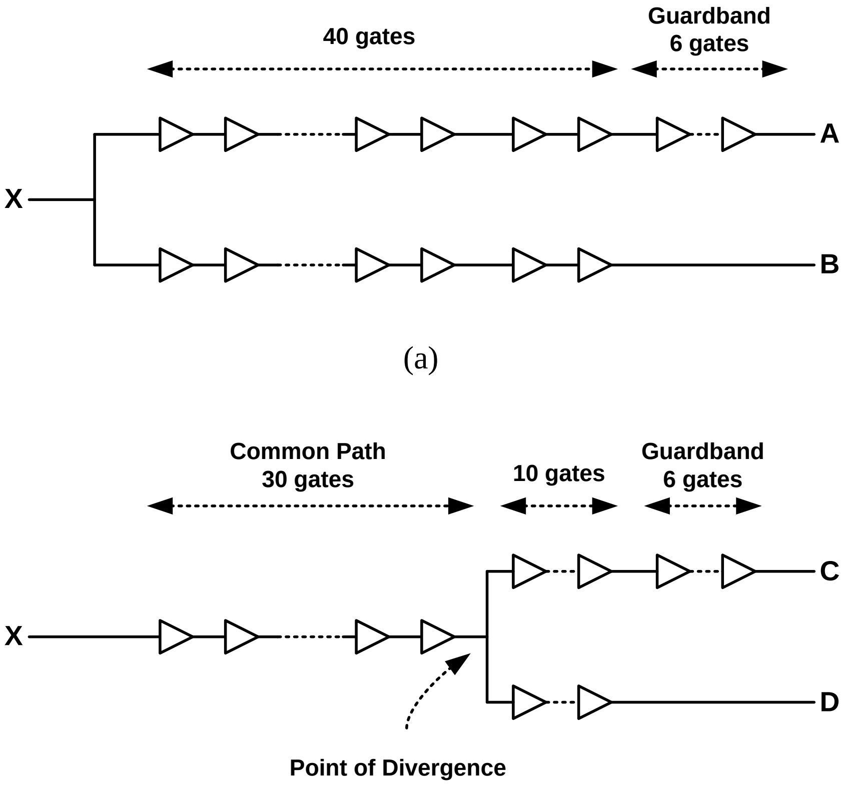
4.3.2 Determination of Guardband

The determination of a safe guardband is an important consideration. If the guardband is too large, the timing overhead will be prohibitive. Conversely, if the guardband is too small, timing violations at extreme variation corners may result in catastrophic logic errors. Fortunately, the guardbands required for PDS are much smaller than those applied globally for PVT tolerance. This is due to two main factors:

1. The guardband is derived from differences in relative on-chip path delays and therefore are not affected by global inter-die process variation, but are vulnerable to intra-die variation, which is substantially smaller, even in scaled process technologies.
2. As the guardband is introduced only in the final carry-merge operation, which is at the end of the timing path, the majority of the critical path is a common path which fans out to both the MSB and LSB groups. Therefore variation on the common segment does not affect the guardband, which is determined only by relative path length. Commercial STA tools are able to account for this using a Common Path Pessimism Removal (CPPR) algorithm [58].

To examine this in more detail, we describe an experiment to quantify worst case intra-die variation on the guardband.

Figure 4.10 shows four logic paths used in the experiment. Path X→B is the reference that represents the nominal critical path. X→A represents a conventional canary path, which is designed to have greater delay than X→B over worst case intra-die PVT conditions. On the other hand, paths X→C and X→D represent the case with PDS, where the majority of the path delay is due to a shared common path. End-points C and D represent the LSB (Razor) and MSB end-points respectively. Using a commercial STA tool, the worst case delay difference between end-points A and B, and C and D was analyzed (Figure 4.11), using four global PVT conditions and 10% On-Chip Variation (OCV). While the global corners vary the gate delay, the relative delay variation is very small (approximately one buffer delay). On the other hand, the effect of OCV on the guardband is rather pronounced, particularly in the case of the guardband for the separate paths (X→A and X→B), which falls below one gate delay in the worst case.



(a)

(b)

Figure 4.10: Paths to A and B (a) have a path length difference of 6 gates; Paths to C and D (b) also have 6 gates difference, but share 30 common gates before the point of divergence.

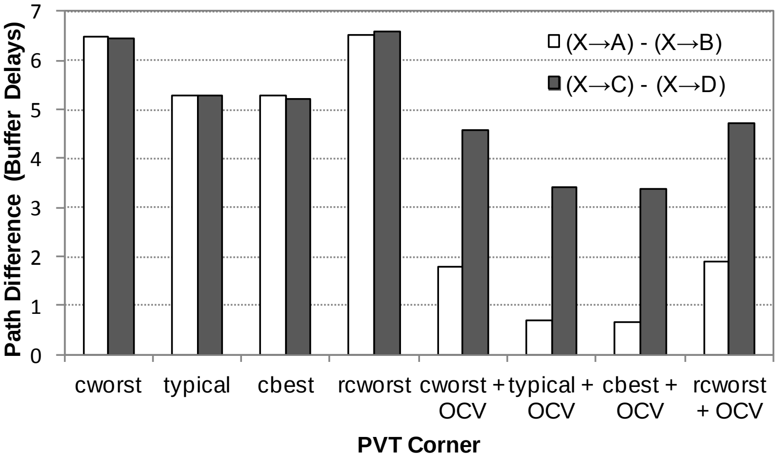


Figure 4.11: Variation in relative path lengths of end-points (A and B) and (C and D) over global PVT corners and considering on-chip variation.

The effect of the common path results in the relative delay between X→C and X→D remains above three buffer delays, which is a conservative margin for uncertainty. Following this simulation methodology, the achieved guardband can be verified at design time for a whole DSP macro. The required guardband is independent of the common path delay and therefore does not necessarily increase with clock period. The LSB paths have very high path activation, much higher than the MSB paths, which actually makes them more suitable for detecting delay variation.

4.4 Analysis of Timing-Errors

One of the key benefits of shaping the path delay profile into two levels, is that the effects of transient bit errors can be easily analysed in a worst-case sense. An N bit arithmetic logic stage with RFF end-points can be analysed for performance in the worst case timing-error conditions by simply assuming all the M speculative end-points have failed to meet setup and/or hold timing and have therefore been latched incorrectly.

4.4.1 Timing-Error Magnitude Bound

To start, the noise contributed by a single stage is analysed. A uniformly distributed N bit integer, x, consisting of the bits $b_0, b_1, \dots, b_{N-1}$, can be represented in signed two's complement form as

$$x = -b_{N-1}2^{N-1} + \sum_{i=0}^{N-2} b_i 2^i, \tag{4.1}$$

where b_{N-1} is the sign bit. In the case of PDS, x consists of M LSBs and $(N - M)$ MSBs, where $M < N$, such that x consists of the bit vector $b_0, b_1, \dots, b_{M-1,} b_{N-M}, \dots, b_{N-1}$, with the representation

$$x = -b_{N-1}2^{N-1} + \sum_{i=M}^{N-2} b_i 2^i + \sum_{i=0}^{M-1} b_i 2^i. \tag{4.2}$$

As previously described, timing-errors are bound using a circuit-level technique to the M LSBs and therefore an error signal, x_e, is declared which is dependent only on the LSB group for magnitude and the (error-free) sign bit,

$$x_e = -b_{N-1}2^{N-1} + \sum_{i=0}^{M-1} b_i 2^i. \tag{4.3}$$

Hence x_e is bound in magnitude,

$$-2^{M-1} \leq x_e < 2^{M-1}. \tag{4.4}$$

Since the sign-bit is in the $(N - M)$ non-speculative timing group, it is not affected by timing violations and hence timing-errors are ideally distributed around a zero mean, i.e.

$$\mu_e = 0. \tag{4.5}$$

4.4.2 Statistical Model

In order to develop a useful statistical model for the timing-error noise characteristics, some additional system variables are introduced to describe the frequency and size of errors. The probability of a finite error, i.e. $x_e \neq 0$, is given by p_e. The target error rate of the DVS loop regulates p_e by controlling the circuit supply voltage. An ideal control loop is assumed, with infinite supply voltage modulation bandwidth, such that p_e determines the probability of sub-critical voltage scaling in a given clock cycle.

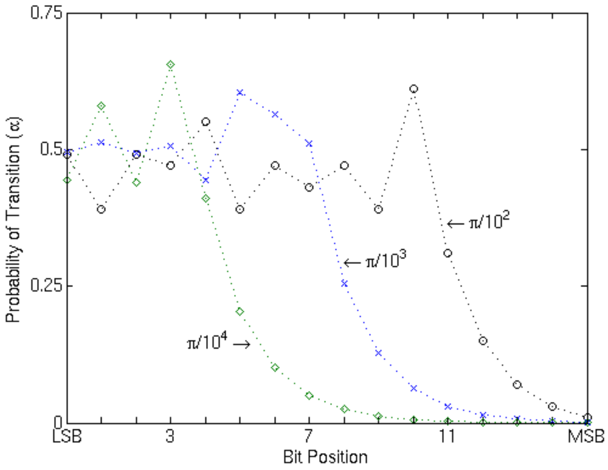


Figure 4.12: Bit transition probabilities for a 16-bit sinewave representation of four frequencies. Normalised frequencies are annotated in radians per second.

The relationship between p_e, V_{dd} and $Tclk$ is non-linear and time-varying due to dynamic PVT effects. The distribution of bit errors in a word determines the average overall error magnitude. The distribution is dependent on both the path activation probability and the path length for each bit position in an N-bit word.

The probability of logic transitions at individual bit positions depends on the underlying signal statistics. The probability of a bit transition between consecutive samples is assumed to be given by a single activity factor, α. Figure 4.12 shows the probability of a bit transition, α, over a 16-bit word between consecutive samples of sine waves of various frequencies. Noticeably, there are two distinct regions, one where toggling tends to $\alpha \rightarrow 1/2$ and one due entirely to sign extension where $\alpha \rightarrow 0$. The cut-off between these regions is determined by the signal bandwidth, where for all but very narrowband applications, or for $M \ll N$, α is roughly independent of signal bandwidth across M LSBs. Hence, the assumption that α is equal for each of M LSBs can be made.

Finally, the influence of the path lengths on the bit error distribution is considered. Although the probability of bit errors is strongly dependent on the path delay statistics, a simplification is introduced that the M^{th} LSB is the only bit that fails. This allows us to accurately model the error noise without needing to know relative delays for all bits (this information is of course not known at the algorithm design stage). Although at very low error rates (the intended operating point) the M^{th} LSB is likely to be the only bit that will fail (as it has by definition greater fan-in than the lower order LSBs), as the error rate increases, other bits in the LSB group will start to fail, which then introduces an error term into the analysis. This is not considered significant as long as the error rate is low enough.

The probability mass function of x_e is given diagrammatically in Figure 4.13, with error variance, σ_e^2, given by

$$\sigma_e^2 = \sum_{i=1}^{n} (x_i - \mu)^2 . p_i = 2^M p_e. \tag{4.6}$$

Assuming the signal is a uniformly distributed integer with variance σ_s^2, the signal to error noise (x_e) ratio, which determines the useful dynamic range, is given by

$$\frac{S}{N_e} = \frac{\sigma_s^2}{\sigma_e^2} = \frac{2^{\mathrm{N}}}{2^{\mathrm{M}} p_e}. \tag{4.7}$$

Figure 4.14 shows S/N_e (7) against p_e for $M = 6$ and $M = 8$, along with simulation results, for a 16-bit adder. Clearly the model is an excellent fit with the simulation results until the MSB group fails at high error rates (well beyond the intended operating point). Simulation results of a conventional 16-bit adder with only a single timing constraint are also plotted to illustrate the proposed approach. Figure 4.15, plotted on a logarithmic axis shows how both curves tend to ~96 dB dynamic range at $p_e = 0$. There are only very few simulation points at low error rates as very long simulation runtime is required to reach low error rates.

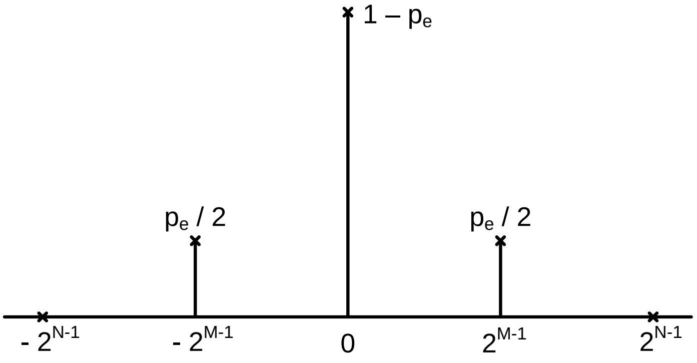


Figure 4.13: Probability mass function of x_e.

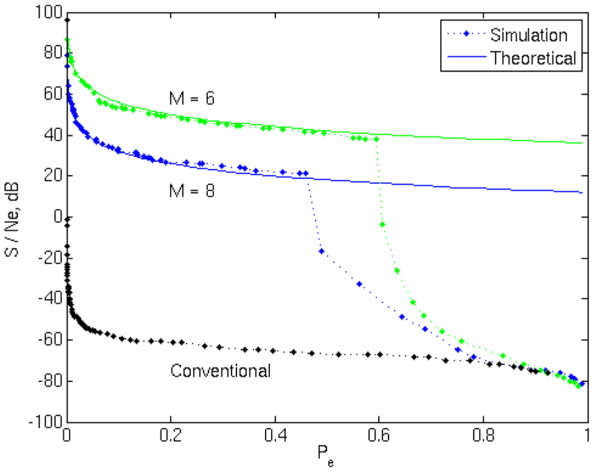


Figure 4.14: Theory vs. simulations for 16-bit PDS and conventional adders.

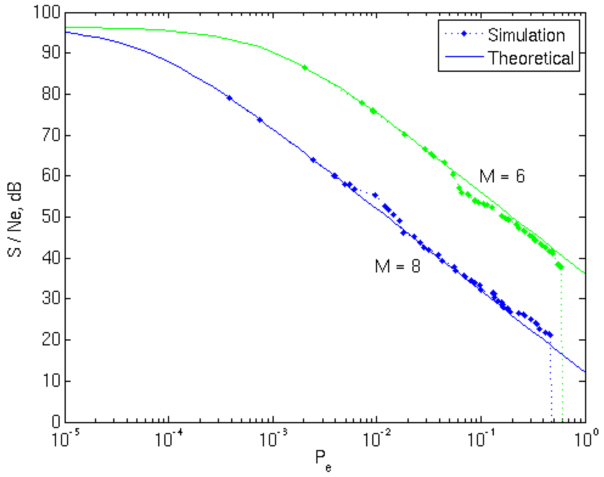


Figure 4.15: Theory vs. simulations for 16-bit PDS adders.

In order to analyze the accumulation of timing-error noise in a system composed of multiple PDS stages, a simple linear-noise model is used in order to ascertain its effect at the output, in a similar fashion to the analysis of rounding errors [59]. Starting with a model of infinite precision, an external error input is added for each register bank that contains RFFs on critical paths. It is assumed that only these end-points are subject to sub-critical timing violations and that sufficient DVS loop bandwidth exists to vary the operating point in response to a non-zero timing-error rate, before setup timing on the remaining non-critical end-points are violated.

Next, our analysis is extended by generalising to a pipeline of repeated identical stages which are considered over N samples. The timing-error noise for the i^{th} datapath stage is given as $e_i[n] = x_e$. The non-linear timing-error noise is modelled in a linear fashion given the following assumptions:

1. $e_i[n]$ is an additive, independent, identically distributed (i.i.d.) white-noise process with assumed zero-mean.
2. $e_i[n]$ is a wide-sense stationary random process, i.e. mean and co-variance are independent of time index n.
3. $e_i[n]$ is assumed to be uncorrelated to all other signals, such as input signals and other noise signals.

Over K datapath stages, the average noise power is

$$\sigma_e^2 = \frac{1}{N}\sum_{n=0}^{N-1}\sum_{i=0}^{K-1} e_i[n] = K2^{\mathrm{M}}p_e + 1, \tag{4.8}$$

and the signal to error noise ratio at the output becomes

$$\frac{S}{N_e} = \frac{\sigma_S}{\sigma_e} = \frac{2^{\mathrm{N}}}{K2^{\mathrm{M}}p_e}. \tag{4.9}$$

4.5 Linear Phase Filter with PDS

This section investigates the proposed approach in the context of a digital filter datapath, which is a common kernel chosen for hardware acceleration in wireless and multimedia SoCs. A programmable coefficient design has been exclusively targeted, as it is more suitable for use as a hardware accelerator in SoC applications. Since the coefficients are not known a-priori, several known algorithm-level optimisations for timing-errors in FIR filters 43 are not directly applicable.

4.5.1 VLSI Design with PDS

The FIR filter operation is a convolution process, defined as:

$$y[n] = \sum_{i=1}^{N-1} h[i]x[n-i], \tag{4.10}$$

where $x[n]$ is the input signal, $y[n]$ is the output and $h[i]$ are the filter coefficients. Figure 4.16 shows the signal flow graph of a transposed direct-form realisation of (10). Timing-error noise sources, $e_i[n]$, have been added for each datapath stage, according to the previously stated linear noise model assumptions. The output is thus given by

$$y[n] = \sum_{i=1}^{N-1} h[i]x[n-i] + \sum_{j=0}^{K-1} e_j\,[n]. \tag{4.11}$$

Each tap is a separate multiply-add datapath stage, i.e. $K = 16$. Since all $e_i[n]$ are assumed to be i.i.d. processes, the maximum timing-error noise magnitude at the output of this structure is $e[n] = 16 \cdot e_i[n]$.

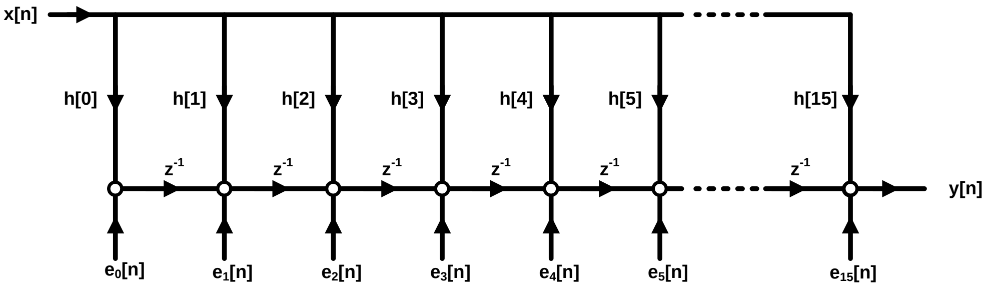


Figure 4.16: Signal flow graph for conventional 16-tap transposed direct form, with timing-error noise sources $e_i[n]$.

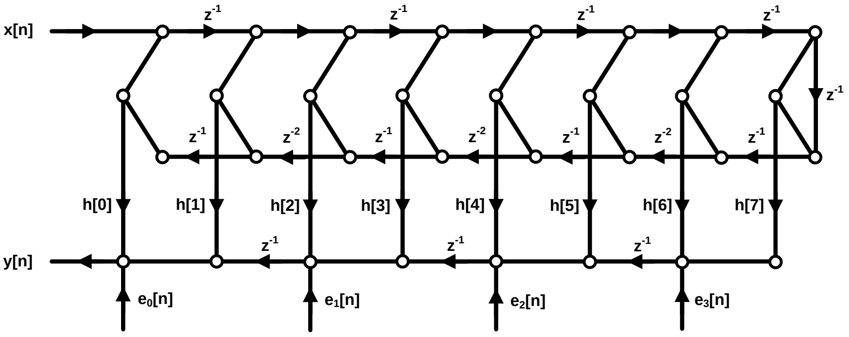


Figure 4.17: 16-tap re-timed symmetrical direct-form FIR reduces the number of i.i.d. noise sources by 75%.

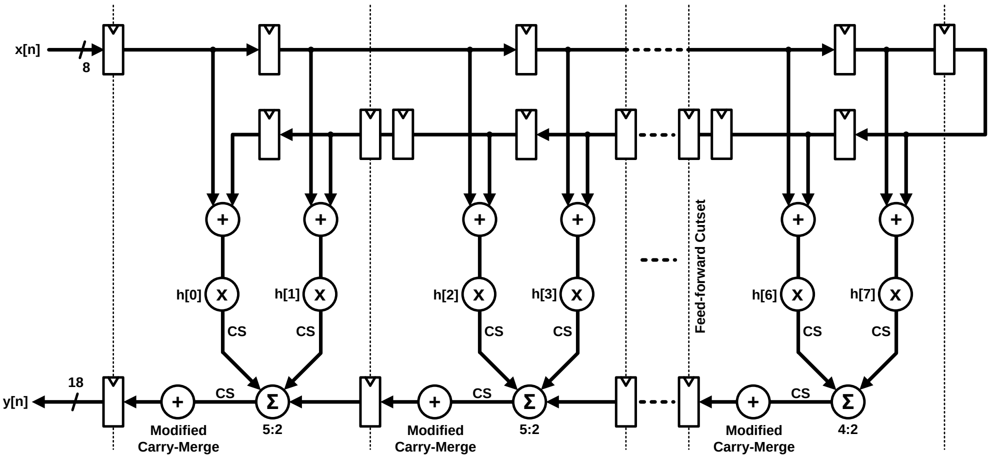


Figure 4.18: VLSI architecture of 16-tap symmetrical retimed direct form FIR. Carry-Save representation for intermediate signals is denoted as CS, all other signals are binary twos complement.

Figure 4.17 uses two techniques to reduce this maximum timing-error. Firstly, the symmetric direct-form is used, which halves the number of timing-error noise sources, while also ensuring phase-linearity is preserved in the presence of timing-errors. Secondly, this structure is retimed along a feed-forward cutset to combine two symmetric taps in each logic stage [60], thereby reducing the maximum timing-error noise contribution by half again, to $e[n] = 4 \cdot e_i[n]$. Figure 4.18 shows the resulting datapath for the 16-tap FIR, which incorporates the modified carry-merge adders and Razor error detecting flops. The implementation employs 8-bit coefficients, 8-bit input data words and an 18-bit adder chain to allow for word growth. The number of bits in the LSB group is set to 8 (i.e. $M = 8$).

4.5.2 Overheads of Proposed Approach for FIR Filters

The proposed PDS approach trades delay for error resilience over a given timing guard-band and therefore increases the minimum clock period. To illustrate this, a tentative comparison to a conventional implementation is made. To make a fair assessment, the frequency and power consumption of this conventional implementation is considered with full worst-case design-margin (i.e. at V_{dd} = 1 V). An FIR implementation with a conventional Sklansky carry-merge adder achieves a minimum delay of 1.1 ns (900 MHz) in a 32nm process technology. The proposed PDS implementation has a conservative timing guard-band of 230ps, which is a 20% delay overhead. The area overhead of the proposed design compared to the conventional at iso-frequency is 22%, due to double-height Razor flip-flops and the larger carry-merge adders. To contrast the delay-efficiency of PDS with the ANT approaches [61], an implementation with a RCA instead of a Sklansky carry-merge adder has also been designed. This resulted in a 72% delay increase compared to the conventional baseline. These findings suggest PDS is well suited for high-performance designs.

4.5.3 Simulation Results and Discussion

The proposed FIR design (layout shown in Figure 4.19) was simulated extensively at the transistor level using Synopsys HSIM with full extracted parasitics, over a range of supply voltage scaling conditions and process/temperature corners. The required simulation runtime for this experiment is significant, but provides accuracy well beyond gate-level simulation. The coefficients used for the simulations are for a symmetric low-pass response with normalised cut-off frequency, $\omega_c = \pi/2$ radians/sample. 1,000 input vectors, consisting of uniform noise samples with full-scale amplitude, were used to exercise the filter amplitude response up to the Nyquist frequency, with approximately worst-case path-activation and power consumption.

The clock period was kept constant at 1.33ns while the supply voltage was scaled down from the process nominal of 1 V, in order to statically infer performance under DVS. The performance of the filter was gauged by calculating the stop-band attenuation, η, as the ratio of pass-band power to stop-band power, both of which are defined as integrals of the power spectral density, Φ(ω);

$$\eta = 10 \cdot log_{10}\left(\frac{\int_0^{\omega_c} \Phi(\omega).\,d\omega}{\int_{\omega_c}^{\pi} \Phi(\omega).\,d\omega}\right). \tag{4.12}$$

This gives an averaged measure of frequency selectivity, which is appropriate for describing digital filter performance.

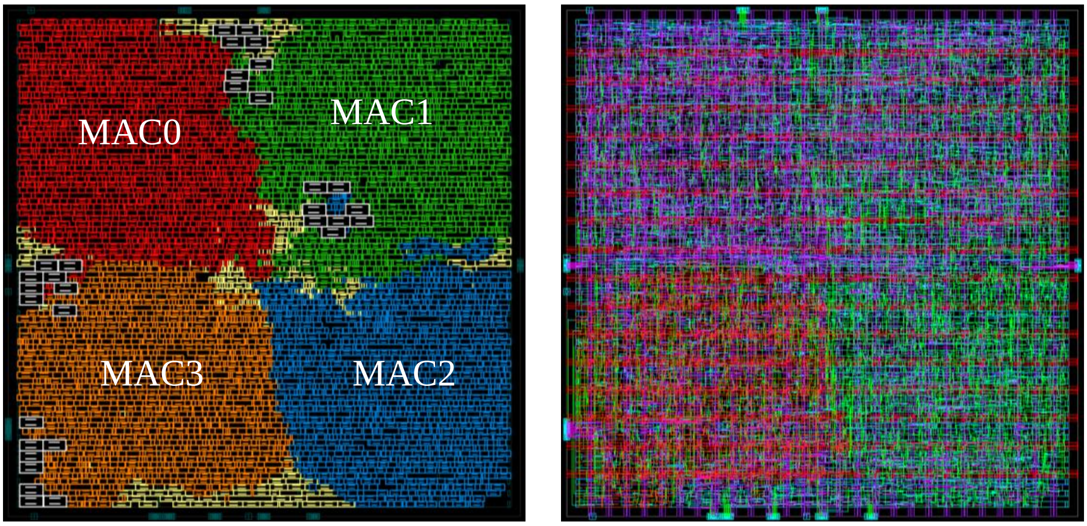


Figure 4.19: FIR standard cell layout (left), with double-height Razor flip-flop cells in white and with full metal stack (right). Each region denoted “MAC” is a 4-tap symmetric multiply-accumulate unit. Layout area is 8,251 um^2.

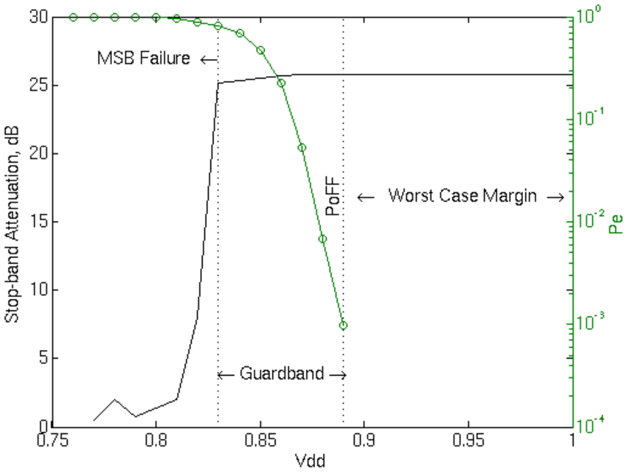


Figure 4.20: Stop-band attenuation vs. supply voltage at typical corner (TT/25°C).

The simulation results in Figure 4.20 show η and p_e as a function of Vdd, starting from the nominal 1 V, which includes full worst-case design margin at the typical corner. Dynamically removing this margin moves Vdd down to 0.89 V, at the point of first failure[15].

[15] In simulation it is hard to reach low error rates as this requires a large number of vectors and fine voltage steps, giving rise to very long runtime.

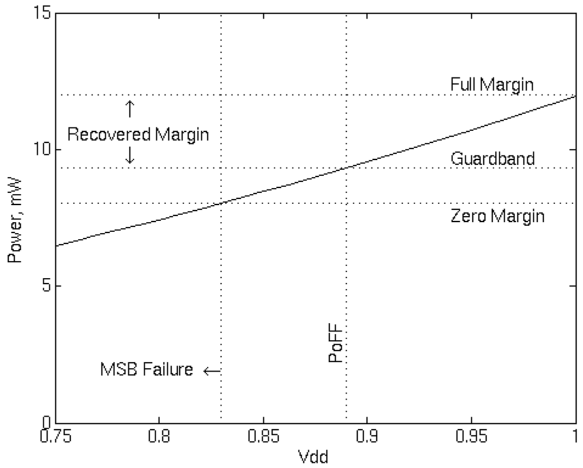


Figure 4.21: Power dissipation vs. supply voltage for proposed and conventional at iso-frequency and typical conditions.

At this point, paths from the LSB group begin to fail intermittently, resulting in a reduction in η (6), albeit of not more than 0.5 dB[16]. Beyond 0.82 V, MSB paths also start to fail, resulting in a rapid decline in η. The resulting timing guard-band provides between 40 mV (FF/125°C) and 70 mV (SS/-40°C) of further headroom. This is an essential buffer to protect the critical MSBs as the finite DVS loop bandwidth may not be sufficient in the presence of fast transients in switching activity and supply voltage noise.

Finally, Figure 4.21 shows power dissipation as a function of supply voltage at the nominal corner. Compared to a fixed-supply baseline with full worst-case design margin at iso-frequency, the reduction in power dissipation at the PoFF is 23%. Further, at the cost of the resilience afforded by the guard-band, the operating point can be maintained at an increased error rate, which leads to power savings of up to 30%.

[16] A reduction by 1.5 dB would allow use of a lower-order response.

4.6 2D Discrete Cosine Transform with PDS

In this section, PDS is applied to a 2D DCT accelerator block. The DCT operation is commonly used in a number of image and audio coding standards.

4.6.1 VLSI Design with PDS

The N point one-dimensional (1D) DCT-II operation 60 [62] can be expressed as the following:

$$X(k) = \frac{w(k)}{2} \sum_{n=0}^{7} x(n) cos \left[\frac{(2n + 1)\pi k}{16} \right], \tag{4.13}$$

where $x(n)$ is the input pixel vector, $X(k)$ is the transformed output and $w(0) = 1/2$ and is otherwise 1. The 2D transform is achieved using two 1D DCT blocks with a transposing memory in between (Figure 4.22). Parameters appropriate for a typical image processing application are assumed, where blocks of 8 x 8 pixels from a bitmap image are transformed at a time.

The optimisation of the DCT has received significant attention in the literature, resulting in algorithms with appreciably reduced numbers of addition and multiplication operations [63] [64]. For this case study, the separable Chen algorithm [63] is employed, which has a computation complexity of $O(NlogN)$, requiring 16 multiplications and 26 additions for an 8-point 1D transform. Chen's algorithm is popular as it is simple, low-complexity, reasonably regular and has good numerical properties. The original 16-multiplier (unscaled) version of Chen's algorithm is used for the 1D DCT. The signal flow graph is given in Figure 4.23, where the coefficients are specified as

$$c[k] = \sin\left(k \frac{\pi}{16}\right). \tag{4.14}$$

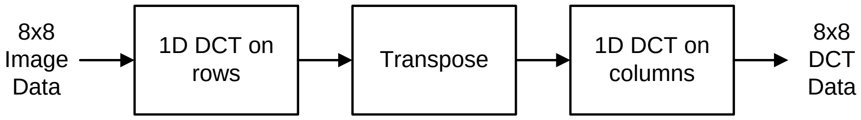


Figure 4.22: Two Dimensional Separable DCT algorithm.

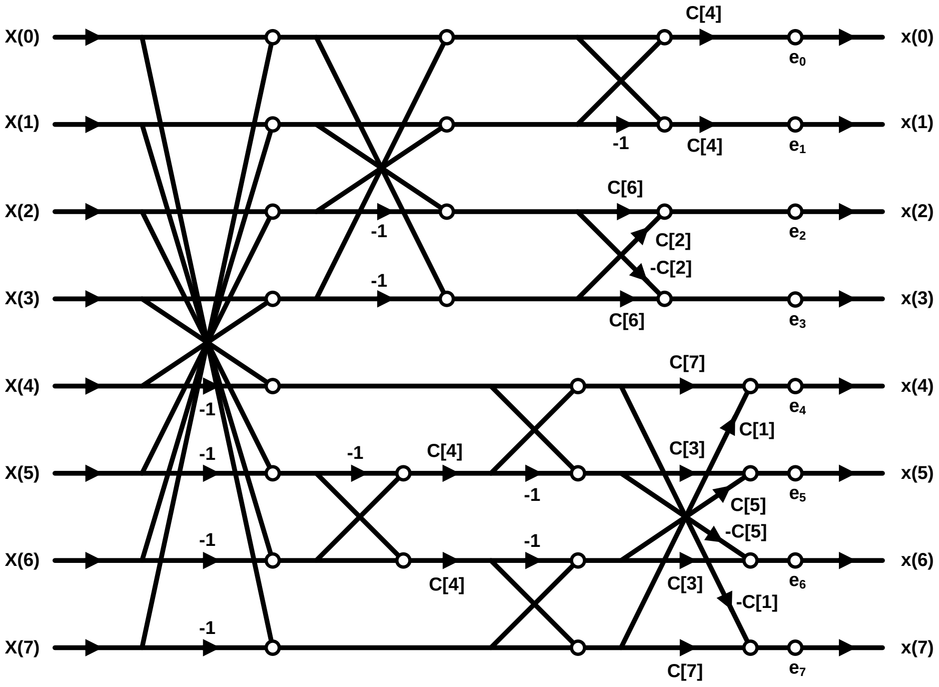


Figure 4.23: 1D Chen DCT signal flow graph with timing-error noise sources, e_i.

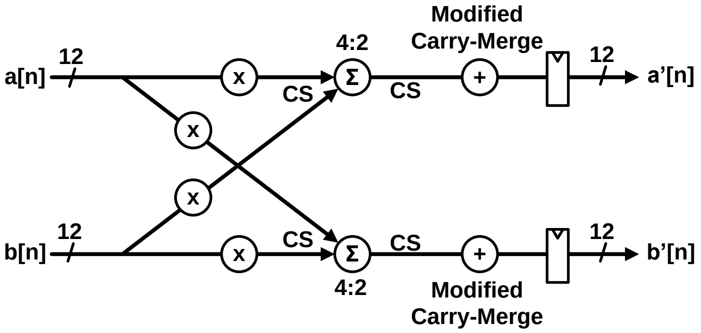


Figure 4.24: Critical final multiply-accumulate butterfly stage section from 1D DCT datapath. "CS" denotes carry-save representation.

This flow graph has been implemented in a single pipeline stage, as shown in Figure 4.23, with additive error sources indicated which represent the scaled noise contributions due to timing-errors. Two 1D stages are used, with a double-buffered transpose block in between.

The transpose block does not contain long paths and thus can easily operate at high speed without risk of generating errors. The two datapath stages employ 8-bit input data, 8-bit coefficients and 12-bit datapaths throughout. Figure 4.24 shows the critical butterfly datapath section with the added modified carry-merge adders ($M = 6$). Simple truncation is used to prevent word growth following multiplications. This scheme achieves 41.4 dB Peak Signal-to-Noise Ratio (PSNR), which represents our baseline performance in the absence of timing-errors. No effort is made to artificially skew delays to different elements of the DCT matrix during physical design [65], although this technique could be incorporated as it is somewhat orthogonal to PDS.

4.6.2 Overheads of Proposed Approach for 2D DCT

A conventional implementation of the 2D DCT in a 32nm process technology was found to achieve a minimum clock period of 1.72ns, using fast Sklansky carry-merge adders. Our PDS implementation with modified timing constraints, merge-adder and Razor FFs has a conservative guard-band of 280ps (which represents a 16% increase in minimum clock period). The area overhead is approximately 14%, due to the double-height RFF cells and the larger carry-merge adders.

In order to make a tentative quantitative comparison with ANT, a 2D DCT with ripple-carry merge adders has also been implemented. In actuality, ANT also requires a number of additional blocks, most significantly a predictor block, as previously described, but since these blocks are generally not expected to increase

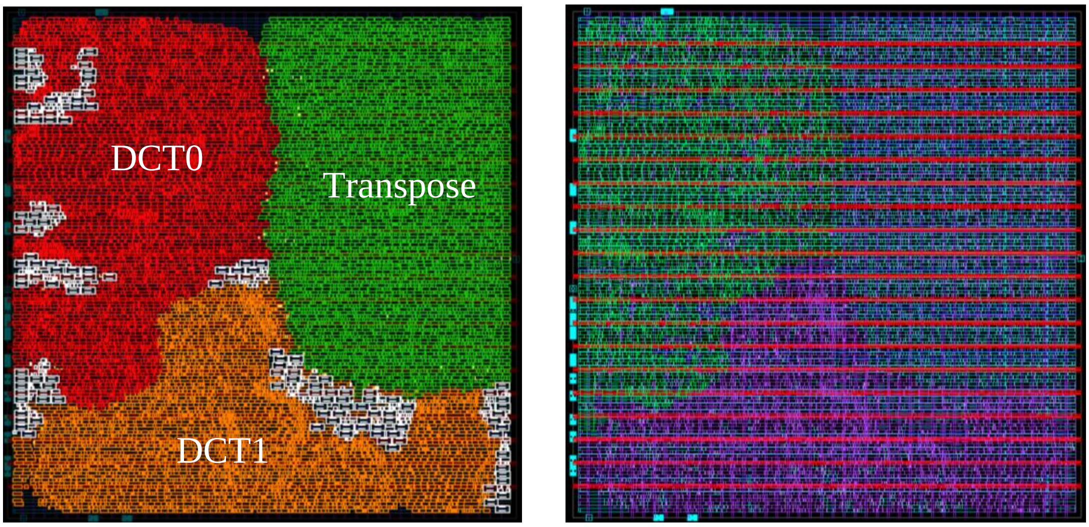


Figure 4.25: Standard cell layout (left), with double-height Razor flip-flop cells in white and with full metal stack (right). Labels indicate the row and column DCTs and the Transpose memory. Layout area is 5,565 um^2.

the minimum clock period, they have been ignored. The delay increase was found to be 69%, compared to the conventional baseline implementation. Again, this confirms the previous observation that our PDS implementation is significantly more delay efficient than ANT implementations. It is important to note that datapaths with smaller word size (N) than those considered here may not show any slow down due to the use of RCAs, since the simpler ripple-carry method often outperforms more complicated schemes for small N [66]. In such cases, ANT datapaths may present minimal clock period overhead.

4.6.3 Simulation Results and Discussion

The proposed DCT implementation (layout given in Figure 4.25) was simulated using Synopsys HSIM. Data from a synthetic random image was used in order to examine performance and power consumption with approximately worst case switching activity for over 1,000 clock cycles. As in the previous section, the clock period was kept constant, while scaling the supply voltage from the process nominal of 1 V, observing p_e, PSNR and power consumption.

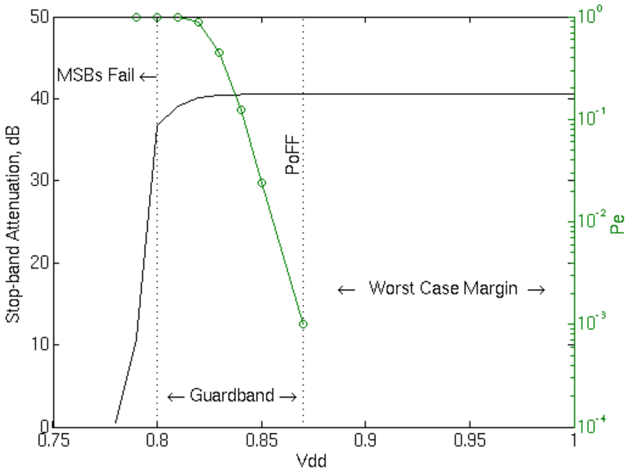


Figure 4.26: Stop-band attenuation vs. supply voltage at typical corner (TT/25°C).

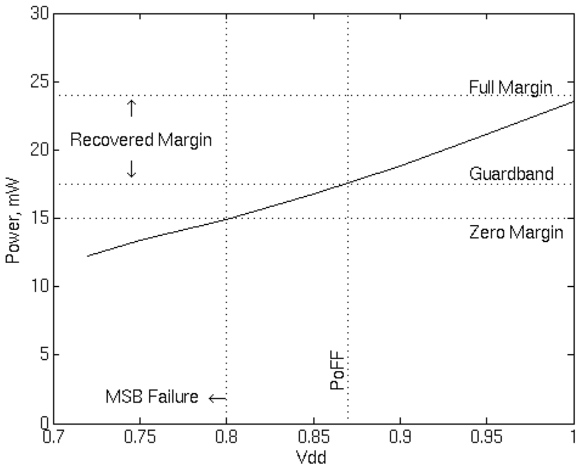
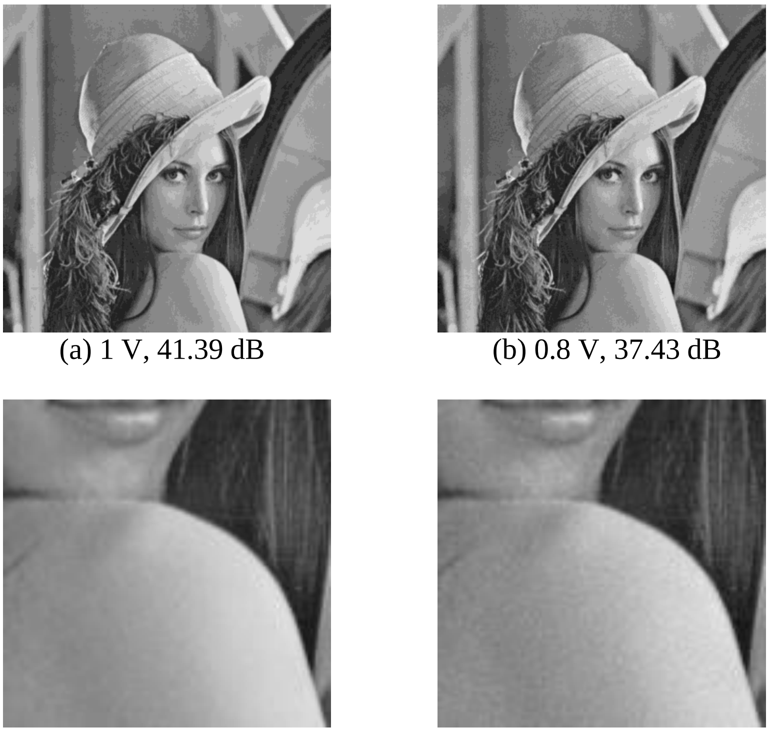


Figure 4.27: Power dissipation vs. supply voltage for proposed and conventional at iso-frequency and typical conditions.

The simulation results in Figure 4.26 show p_e and PSNR at TT/25°C. At this operating point, V_{dd} can be scaled from 1 V to the PoFF at 0.87 V. Beyond this point, the error rate increases until MSB paths fail around 0.8 V. Between the PoFF and the MSB failure point lies the timing guard-band, where PSNR is found to degrade by a maximum of 3.8 dB. The guard-band was found to provide between 50 mV (FF/125°C) and 90 mV (SS/-40°C) of headroom over which errors can be detected safely.



(a) 1 V, 41.39 dB

(b) 0.8 V, 37.43 dB

(c) 1 V, 41.39 dB

(d) 0.8 V, 37.43 dB

Figure 4.28: Test image "Lena" with proposed DCT at full WC margin (a) (c), and PoFF (b) (d), showing Vdd and PSNR. The inverse transform used after the forward DCT is floating-point.

Figure 4.27 shows power consumption as a function of supply voltage. Compared to a fixed-supply baseline with full worst-case design margin at iso-frequency, the reduction in power dissipation at the PoFF is 21%. While it would not be safe to operate the design outside the guard-band, it is noted that the power saving down to the zero margin point is 36%.

Timing-errors in the PDS implementation generate weakly correlated Gaussian noise in the DCT domain output signal. Figure 4.28 shows the visual effect of this additive noise, considering the 512 x 512 pixel "Lena" natural test image. The bitmap in Figure 4.28(a) is the result of transforming the original test image using the proposed DCT operating at nominal supply voltage, before transforming back using a floating point IDCT, in order to avoid introducing additional rounding noise. The image in Figure 4.28(b) was processed in the same way, except with the proposed DCT operating at 0.8 V, resulting in a roughly 4 dB loss in PSNR. The effect of the additive noise is noticeable on plain areas of the image, as shown in the detail crop in Figure 4.28(d). The additive noise does not remove detail [67] and the perceived loss of quality in this case is negligible. This result is in contrast to the masking of DCT coefficients [65], which does result in loss of high frequency detail in the output image. Furthermore, where the DCT is used as part of an image compression system, LSB noise is discarded for all but low-frequency coefficients during the quantisation stage following the DCT operation.

4.7 Comparison to Published Approaches

In order to put the proposed PDS technique into context, a qualitative comparison with established approaches from the literature is presented. Table I contrasts the key features of PDS along with generalisations of two approaches introduced in Chapter 2, both of which have also been studied in numerous DSP applications.

The most established technique is ANT, which is the only one to have been realised in silicon to date [61]. ANT represents an elegant solution that requires only standard logic gates and flip-flops. An implementation of the algorithm, known as the main pipeline, is designed to produce timing-errors in the MSBs, such that they are of large magnitude. This is achieved by explicit use of RCAs, which in our comparisons were found to incur a delay increase of 69–72% in high performance applications. An estimator block is then implemented to provide a low-overhead prediction of the current output sample. An error is identified by the decision block when the main pipeline output diverges from the output of the estimator block by more than a given threshold. If an error is detected, the incorrect sample is replaced with the output of the estimator.

Table 4.1: Qualitative comparison with published approaches.

	Error Detection	Error Mitigation	Circuit Overhead
ANT	Main pipeline output sample compared to estimator output	Replace erroneous output sample with estimator sample	RCAs in main pipeline limit performance; estimator block; decision block
SDC	Analogue PVT sensor and pre-calibrated look-up table	Errors forced into less significant coefficients	PVT sensor; minimal performance loss due to the algorithm/architecture modifications
PDS	Razor flip-flops	Errors forced into less significant bits of datapaths	Razor flops; modified carry-merge adders

The estimator block and the decision block introduce additional circuit overhead, mainly dictated by the implementation of the predictor, for which there are a number of options. The predictor block may also introduce additional limitations, e.g. the linear prediction approach may limit signal bandwidth, while the RPR technique may introduce excessive area overhead [65].

Significance-driven computation is more closely related to PDS, in that it coerces timing-errors to occur first in a particular part of the circuit by affecting the path delay, resulting in a timing guard-band. The key difference is that SDC ensures that computations associated with less significant coefficients are most critical and therefore fail first, while the most important coefficients are engineered with a slack margin. This is achieved in practice through algorithm/architecture transformations that maximise sharing of common sub-expressions for slow paths and minimise sharing for fast paths. These transformations are most applicable when the algorithm coefficients are fixed and know in advance. The DCT design in [65], for instance, defines three path groups with increasing delay for outputs corresponding to higher frequencies in the spatial domain. The result on image quality is a gradual loss of fine detail as the three path groups are progressively compromised. A calibrated analogue PVT sensor is used to detect delay variation in order to zero DCT coefficients that are subject to timing-errors. This constitutes a canary approach and a margin must be included to account for intra-die process variation.

PDS offers an approach derived from applying Razor DVS to DSP circuits. The Razor concept is adapted to DSP accelerators using timing-error detecting flip-flops on critical paths and adapting the error correction replay mechanism with the error mitigation approach proposed. The circuit area, delay and power overheads are low, and the design flow required is realistic and does not require algorithm manipulations. It is emphasised that in this work, that no attempt is made to provide resiliency at very high error rates, but instead are targeting a sufficient error rate tolerance to afford a timing guard band to protect against catastrophic failure due to fast moving delay variation effects, while reducing power consumption from voltage scaling. A significant limitation of PDS is that there is a minimum suitable datapath bit width that allows a large enough timing guard-band to be developed.

As a final remark, it is conceded that all the considered approaches are susceptible to failure due to datapath metastability. While metastability is not addressed directly in this work, it is remarked that metastability is arguably of less concern in the case of a DSP accelerator, since there is little control logic and often very little interaction between datapath and control logic. In addition to this, DSP circuits typically have a given probability of failure anyway since they are often processing noisy signals.

4.8 Conclusions

In this chapter, a new, more generally applicable technique for circuit-level timing-error mitigation was described, along with the design of an FIR filter and 2D DCT transform. The technique is also broadly applicable to other fixed-point datapaths. The proposed approach has a much smaller impact on minimum clock period (16 – 20% reduction compared to conventional), as it does not necessitate the use of ripple-carry adders and has the advantage of requiring minimal additional design effort.

The proposed approach has been investigated in the context of a high-performance programmable digital filter accelerator and a 2D DCT accelerator in a 32nm CMOS process technology. Simulation results show a reduction in power consumption of 21 – 23% through DVS, with a negligible degradation in algorithmic performance in both cases, as compared to a fully margined conventional implementation at nominal supply voltage.

The PDS approach is shown to offer a number of attractive advantages when compared to other published approaches to timing-error tolerance. Nonetheless, in common with the approach of Chapter 3 and indeed many of the published approaches discussed in Chapter 2, timing violations still result in some error, albeit limited and easily modelled. In a commercial VLSI design context, this may still restrict applicability, since many aspects of design verification at both design and manufacturing test stages, require predictable, bit-accurate results. While design verification and manufacturing test are beyond the scope of this work, the next chapter explores an approach that potentially avoids logic errors altogether during sub-critical operation.

Chapter 5. Timing-Error Correction by Selective Time Borrowing

In this chapter, the use of a time borrowing window on critical logic paths is proposed, over which timing-errors can resolve safely without an explicit replay mechanism. Time borrowing is the effect of allowing some flexibility in the sampling instant, such that a late logic transition can still be safely latched. This approach means that timing violations do not result in logic errors of any kind, as distinct from the preceding approaches. It is demonstrated that time borrowing can be incorporated into DSP pipelines without increasing the minimum clock period, while removing the metastability risk associated with many previously published approaches to replay-free timing-error tolerance.

The use of time borrowing presents an extremely low overhead option, which is naturally well suited to high-performance or low-power applications. However, it does place a performance constraint on the control scheme, which is related to fast changes in ambient conditions, such as temperature. To address this, a novel hybrid control approach is used to ensure timing violations do not exceed the safe borrowing window. Implementation and back-end simulation of FIR and FFT pipelines demonstrate a significant power reduction of 21% and 25%, respectively, with no logical errors at the output. Simulation of the hybrid control loop demonstrates robustness of the proposed approach. The research in this chapter has been presented at the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) [68].

5.1 Introduction

In general, algorithm-level approaches are unsuitable for high-performance circuits as there is additional logic in the critical path and carry-propagation must be implemented serially in some cases, both of which increase delay. In addition, there is a risk of metastability if timing-errors are allowed to violate setup and hold times at flip-flop inputs.

In common with the previous chapter, the approach of using time borrowing to correct timing violations does not make explicit use of the timing-error detection signal for correction purposes. The error detection signals are still used to calculate an error rate which is used to drive the supply voltage scaling.

Logically-correct replay-free timing-error tolerance in the context of DSP pipelines, can be achieved using a purely circuit-level approach. This is realised by introducing a transparent phase using a Razor pulse latch (RPL), taking advantage of inherent path delay properties of arithmetic logic circuits. The use of time borrowing can incur hold buffer overhead and is therefore used in a targeted ("selective") fashion. Significantly, this approach does not increase the minimum clock period of the pipeline circuits studied here and therefore is the most delay efficient approach to timing-error tolerance for high performance applications. In addition, our approach is also metastable-safe.

5.2 Delay Imbalance in Arithmetic Operators

Addition and multiplication operators dominate the critical kernels of the majority of common DSP algorithms [69]. In this section, the combinational logic delay properties of addition and multiplication are studied in isolation, in order to analyze the cost of introducing time-borrowing. Both circuit topology and device sizing are considered, which are critical to achieving a balanced implementation.

5.2.1 Carry-Propagation

The well-known carry propagation dependency presents a rigorous limit to achieving fast, balanced digital circuits. The number of operand input pairs that fan into each sum-bit increases linearly with bit order, since every output depends on all inputs of equal or lower magnitude and thus every input influences all outputs of equal or higher magnitude.

Figure 5.1 shows the Sklansky topology for addition of two 16-bit numbers [56]. It is evident that the paths to the eight MSBs end-points have up to four levels ($\log_2 N$) of dot-operator cells, as compared to the maximum 3-levels for the eight LSBs. Thus, the critical paths in this circuit are concentrated in the MSBs, as illustrated by the red arrow. The critical path start-points tend to be in the LSBs, since intermediate carries from these bits fan out to the rest of graph, which leads to slow propagation times. Paths from MSB start-points to MSB end-points tend to be relatively short (illustrated by the green arrow).

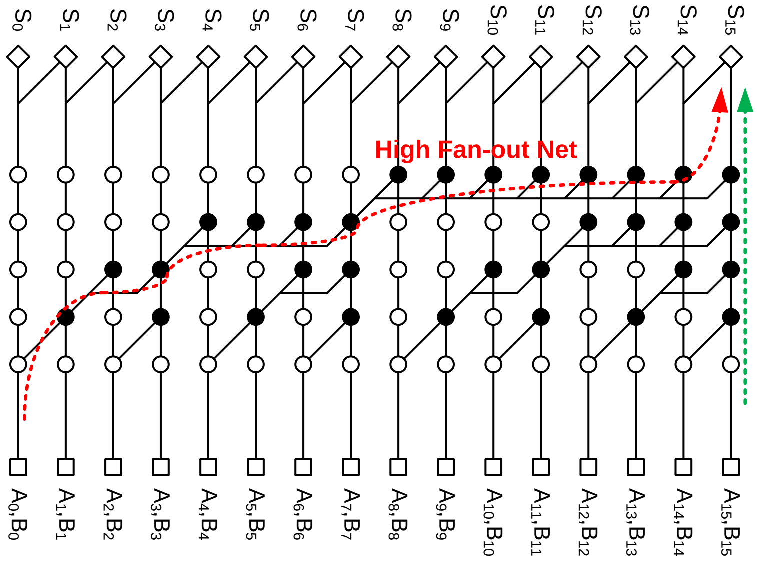


Figure 5.1: Sklansky parallel-prefix graph for addition of two 16-bit numbers.

5.2.2 Partial Product Compression

Multiplication circuits typically consist of three stages: partial product generation, carry-save reduction and final stage vector-merge addition [56]. The vector merge adder typically has similar delay properties to that examined in the previous section (except for optimisations for late-arriving operand bits); however, the delay profile for the multiplier tends to be dominated by the depth of the carry-save reduction tree, varying significantly across its width. Figure 5.2 shows the modified Baugh-Wooley two’s complement binary multiplication matrix for two signed 8-bit operands. As before, the red arrow illustrates the longest path originating in the LSB (of operand Y) and the green arrow shows the longest path originating from the MSB of the same operand. Furthermore, Figure 5.3 shows the logic on the red and green paths in Figure 5.2, showing the LSB start-point ($Y[0]$) path is longer by three full-adder cells compared to the MSB start-point ($Y[7]$), a significant imbalance in a tightly constrained design.

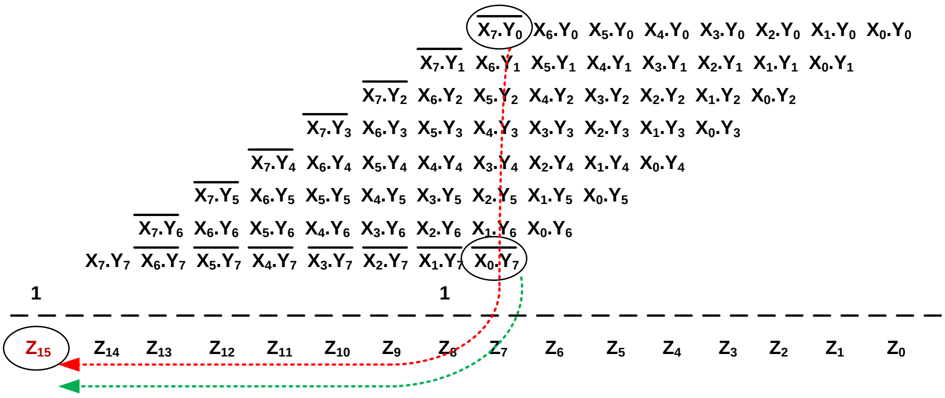

X7.Y0 X6.Y0 X5.Y0 X4.Y0 X3.Y0 X2.Y0 X1.Y0 X0.Y0
X7.Y1 X6.Y1 X5.Y1 X4.Y1 X3.Y1 X2.Y1 X1.Y1 X0.Y1
X7.Y2 X6.Y2 X5.Y2 X4.Y2 X3.Y2 X2.Y2 X1.Y2 X0.Y2
X7.Y3 X6.Y3 X5.Y3 X4.Y3 X3.Y3 X2.Y3 X1.Y3 X0.Y3
X7.Y4 X6.Y4 X5.Y4 X4.Y4 X3.Y4 X2.Y4 X1.Y4 X0.Y4
X7.Y5 X6.Y5 X5.Y5 X4.Y5 X3.Y5 X2.Y5 X1.Y5 X0.Y5
X7.Y6 X6.Y6 X5.Y6 X4.Y6 X3.Y6 X2.Y6 X1.Y6 X0.Y6
X7.Y7 X6.Y7 X5.Y7 X4.Y7 X3.Y7 X2.Y7 X1.Y7 X0.Y7
1
1
Z15 Z14 Z13 Z12 Z11 Z10 Z9 Z8 Z7 Z6 Z5 Z4 Z3 Z2 Z1 Z0

Figure 5.2: Signed multiplication matrix for 8-bit operands, *X* and *Y*. Red arrow illustrates the critical path from the LSB of input operand *B*, green arrow highlights the critical path from the MSB of the same operand.

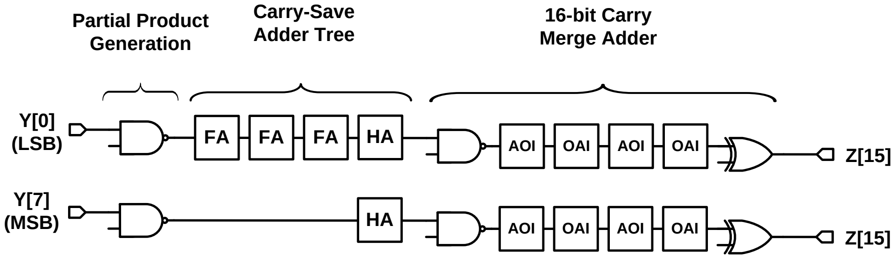


Figure 5.3: Critical paths from LSB and MSB operand inputs for 8-bit multiplication matrix, red and green arrows.

Delay imbalance also exists at the micro-architectural level as well as in the operators themselves, but these aspects are not discussed, as these imbalances can often be overcome by conventional retiming optimisations. This section is concluded with a summary of observations of the timing paths in addition and multiplication circuits:

- Long paths to MSB end-points are unavoidable due to carry propagation, even in minimum depth prefix adders.
- MSBs of input operands have very limited fan-out and therefore tend to be non- critical timing paths.
- Significant hold time slack to MSB end-points, due to regular, high logic-depth topology (cf. Figure 5.1).

- Many common VLSI architectures have significant path-delay imbalance.

5.3 Selective Time Borrowing Approach

In this work, it is proposed to make use of the inherent timing imbalance discussed in the previous section, without increasing the minimum clock period, by using it to resolve the timing-errors that necessarily arise when operating the design in a Razor DVS loop. By assigning RPLs to a group of M critical end-points, a time-borrowing window between stages is introduced. Timing-error detection is performed at these end-points by detecting time borrowing (i.e. any transitions during the transparent phase of the latch). Assigning RPLs only to critical end-points avoids the burden of excessive hold time fixing, which is otherwise necessary to avoid short LSB paths from failing the larger hold time of a RPL. Figure 5.4 illustrates the general concept for an N-bit datapath.

5.3.1 Formulation of Timing Constraints

Suitable timing constraints must be developed to constrain the paths between Razor pulse latches such that sufficient timing slack exists to resolve late transitions at the following start-point.

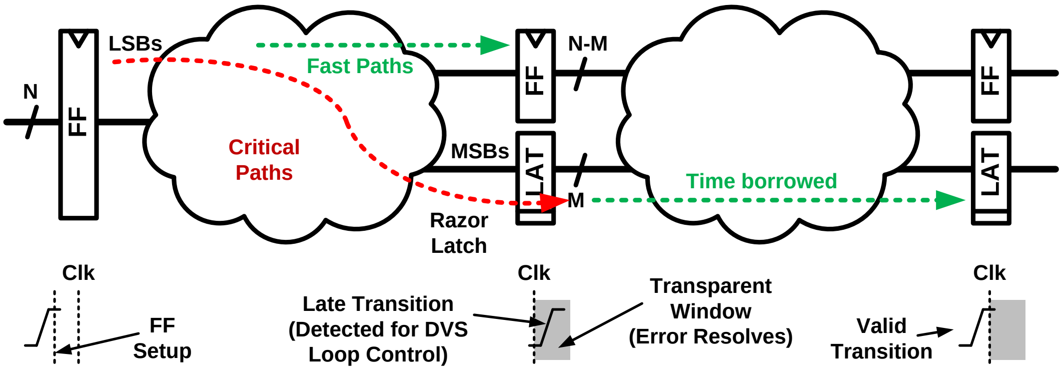


Figure 5.4: Conceptual illustration of selective time borrowing approach.

The necessary timing constraints are described as three separate path groups:

1. FF-to-FF paths: These are non-speculative FF end-points (i.e. cannot incur timing-errors). There should be no long paths in this group as they are LSB-to-LSB paths which generally have few logic levels. Timing violations at FF data pins may cause metastability and so it is necessary to enforce a guardband during automatic place and route to ensure the short paths are not lengthened through the back-end implementation flow.
2. FF-to-RPL paths: These LSB-to-MSB paths are critical by design and will define the minimum clock cycle achievable.
3. RPL-to-RPL paths: Time borrowing is achieved in the MSB-to-MSB paths by launching late transitions at the startpoint, hence, they must be faster than the FF-to-FF paths by an amount equal to the maximum transparency window of the pulse latch.

5.3.2 Hybrid Control Strategy

Selective time-borrowing on critical paths provides a window over which timing-errors can be safely mitigated without risk of metastability. To prevent this window being exceeded, a novel second-order Razor control loop is proposed that incorporates a tuneable canary circuit.

As a sensor of circuit delay change, detection of late transitions at the data pin of a sequential element has a number of issues. Firstly, a transition detector can only detect late transitions when critical paths are activated. In the case of a DSP datapath, this means that if input signal magnitudes are small there will be only very rare critical path activation and hence slow control loop update, except for the case of sign change activity which will sensitise the critical path. Secondly, timing-error detection only indicates when the circuit is sub-critical and cannot detect an increase in slack (which has to be inferred from a zero Razor error rate).

To overcome these issues, a canary circuit is incorporated into the control loop, as shown in Figure 5.5. A canary circuit [10] is designed to detect delay variations such that it fails before the remaining circuitry. In our case, the canary circuit employed is tuneable such that it can be calibrated to match inter- and intra-die PVT effects, removing performance-limiting margin. To this end, the tuneable canary circuit is included in series, such that the detected timing-error rate is used to tune the canary circuit in order to match the longest paths on a given die. The canary circuit tuning loop operates at a reduced rate of F_{CLK}/M, where $M > N$, in order to avoid adapting the canary to local minima due to intermittent periods of low path sensitisation. Furthermore, two delay line taps are incorporated (Figure 5.6), such that either an increase or a decrease in circuit delay can be detected, which allows significantly tighter control of optimal operating point. The truth table in Figure 5.6 describes how the two taps, HI and LO, are used to tune the supply voltage.

The hybrid approach combines the advantages of in-situ timing-error detection, which include robustness to intra-die and fast local variation effects with that of the canary circuit, namely fast response to global variation and sensitivity to positive and negative variations in delay. It is possible to extend the canary approach to multiple circuits distributed within each pipeline stage [10] in order to gain some increased sensitivity to local effects, but this is beyond the scope of this chapter.

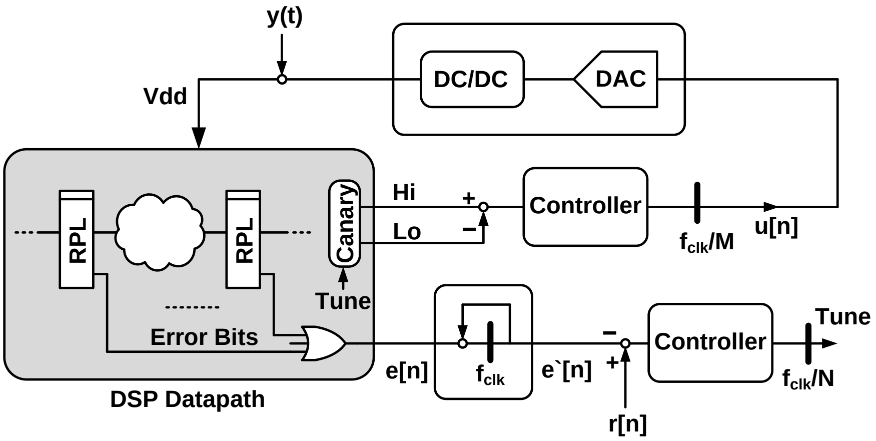
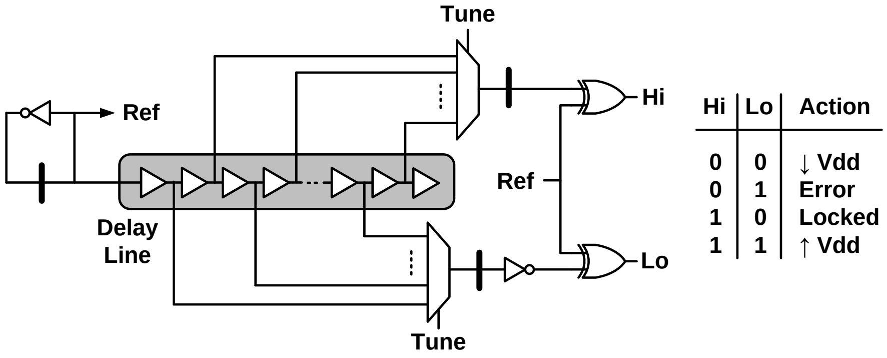


Figure 5.5: Hybrid DVS control loop.



Hi	Lo	Action
0	0	↓ Vdd
0	1	Error
1	0	Locked
1	1	↑ Vdd

Figure 5.6: Two-tap tuneable canary circuit and control truth table.

5.4 FIR and FFT Case Study

In this section, the implementations of two DSP pipelines are described: an FIR filter and a pipeline FFT. These blocks are very common in applications such as wireless communications, audio, video and image processing.

5.4.1 VLSI Architecture

The choice of VLSI architecture needs some consideration with respect to implementation of error resilient circuits. A general goal is to minimise control plane logic, which is difficult to make robust to timing-errors. This is achieved by considering the following guidelines:

1. Avoid non-incrementally addressed RAMs; use only memory structures consisting of Static RAMs (SRAMs) or register files with trivial address generators based on small counters.
2. Avoid critical datapath control signals and feedback paths, such as long feedback paths for operand forwarding.
3. Where possible select maximally systolic architecture, as these generally have the lowest control logic overhead.

The implementation of the 16-tap FIR algorithm makes use of the fully-systolic transposed direct-form architecture [55] shown in Figure 5.7, which has essentially no explicit control logic. The input data samples $x[n]$ and coefficients $h[i]$ are 8-bit signed values, with a 16-bit addition chain. The transposed registers in the accumulation chain are selectively replaced with Razor pulse latches.

The 64-point FFT uses a semi-systolic pipeline, in the form of the well known single-delay feedback [60] architecture (Figure 5.8), as it has significantly reduced area requirement compared to the fully-systolic array and avoids the complex control overhead of an iterative processor style implementation. The design requires a number of First-In First-out (FIFO) buffers of differing depth, which have been implemented as a shift-register here, but can be more efficiently constructed of small SRAM or register-file instances. The datapaths are all 16-bit with a simple fixed scaling scheme to avoid overflow with word growth. Only the registers after the longest paths through the complex multiplier are selectively replaced with Razor pulse latches.

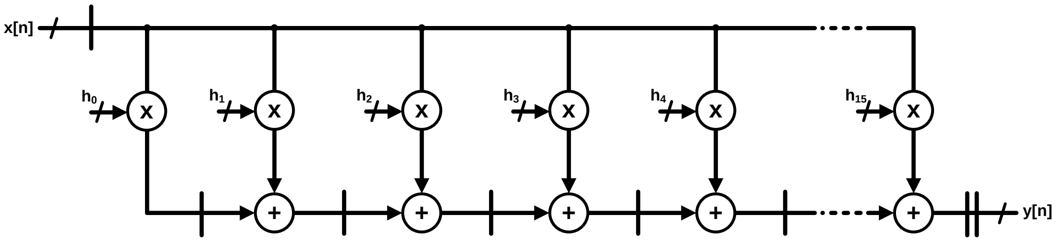


Figure 5.7: Transposed direct-form FIR with 16 coefficients.

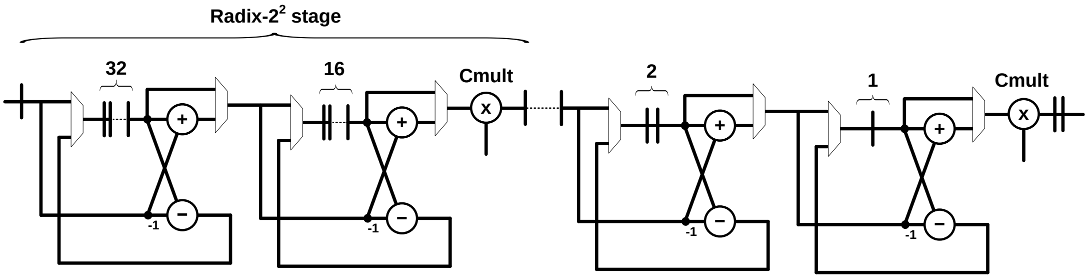


Figure 5.8: 64-pt Radix 2^2 SDF pipeline FFT. Control logic is non-critical and based on a small counter. All datapaths are 16-bit complex words.

5.4.2 Razor Pulse Latch

The RPL shown in Figure 5.9 is similar to that presented in [34] and [70]. This design has a significantly reduced setup time penalty [70] since there is no need to skew the detection window to account for setup time ahead of the rising edge of the clock. The cost of this is an increased hold time requirement. The duty-cycle controlled clock is used to enable a transition detector [34] during the high phase, where the datapath latch is transparent. Compared to a conventional pulse latch, the RPL still suffers somewhat from increased loading of the latch node by the transition detector, however, relative to a Master-Slave Flip-Flop (MSFF), setup time is reduced. Although the datapath latch minimises the chance of metastability on the Q output, the Error pin can still go metastable and therefore, needs a synchroniser before it can be used safely.

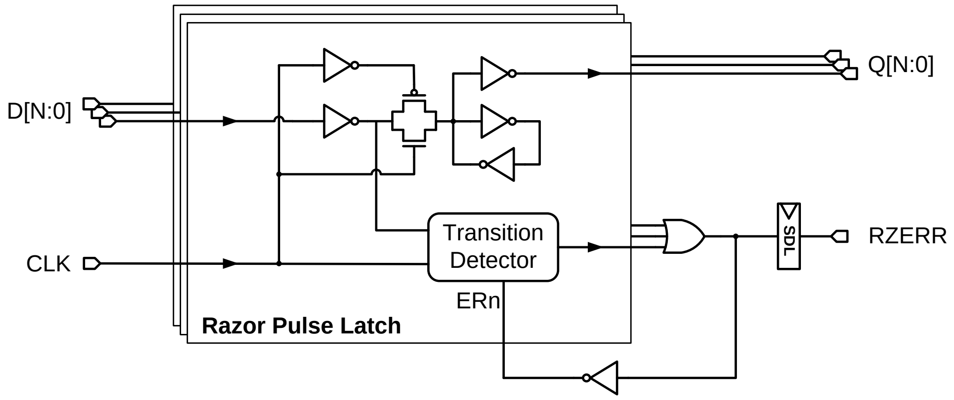


Figure 5.9: Razor pulse latch incorporating self-resetting error detection circuitry and datapath latch. Output error signals for bank are combined and latched with a set-dominant latch.

5.4.3 Implementation Results

The FIR and FFT designs have been implemented in a 32nm LP (low-leakage) CMOS standard cell library, which includes the RPL cell. Both designs were implemented using the proposed technique, for a range of values of M, along with a baseline conventional implementation (referred to as $M = 0$, as it contains no RPLs). A global duty-cycle controlled clock is used to introduce a conservative 200 ps transparent window at RPL sequentials only, all other sequentials are positive edge triggered MSFFs. All circuits were implemented with an industry standard synthesis and automatic place and route flow. Suitable timing constraints, as previously discussed were used to ensure the transparency window on RPL-to-RPL borrow paths. In turn, the transparency window defines the RPL hold time requirement, which is increased relative to a MSFF end-point, but does not lead to significant extra buffering as there are only a few paths to the MSB end-points

The number of MSB RPL end-points, M, should be minimised in order to limit the increase in circuit area due to the additional transition detectors required for a RPL. Figure 5.10 and Figure 5.11 show the area and power impact on the FIR design as M is increased from zero, which is the baseline (conventional design) to 16 (all end-points are RPL sequentials). Clearly from an area and power perspective it is merely desirable to minimise M, however, in terms of timing, a clear trade-off exists. Small values of M are found to result in significant negative setup time slack in non-speculative (MSFF) end-points, as these must meet single-cycle timing as well as an additional setup margin to prevent undetectable timing-errors corrupting state.

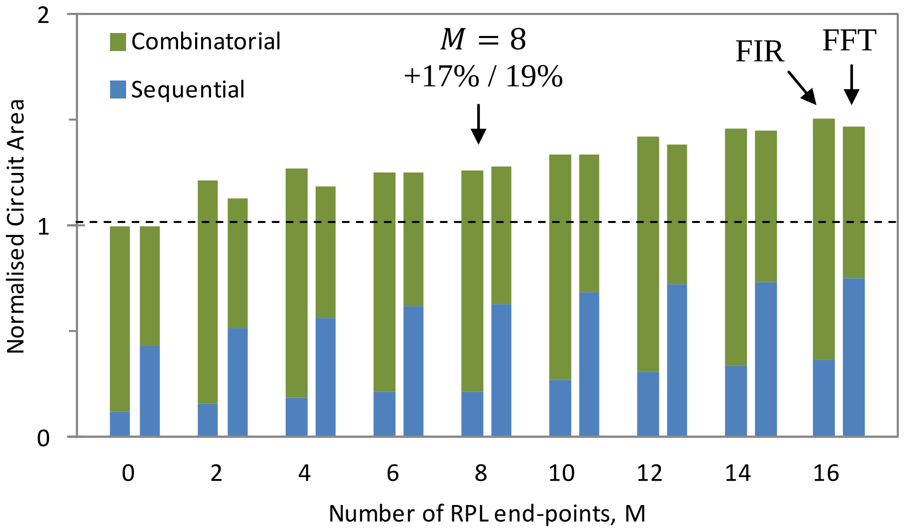


Figure 5.10: Number of RPL sequentials per pipeline stage vs. circuit area for FIR (left) and FFT (right) designs, normalised to $M = 0$ (baseline).

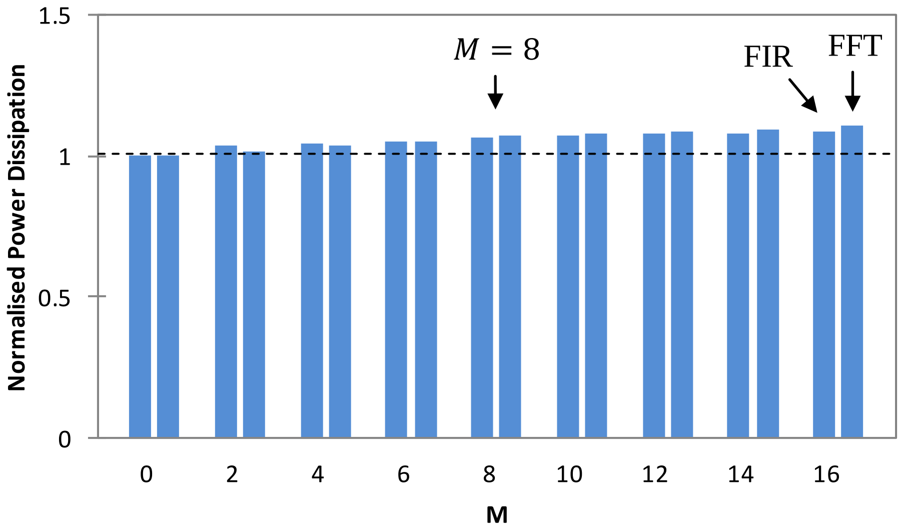


Figure 5.11: Number of RPL sequentials per pipeline stage vs. normalised power dissipation for FIR (left) and FFT (right) designs, normalised to $M = 0$.

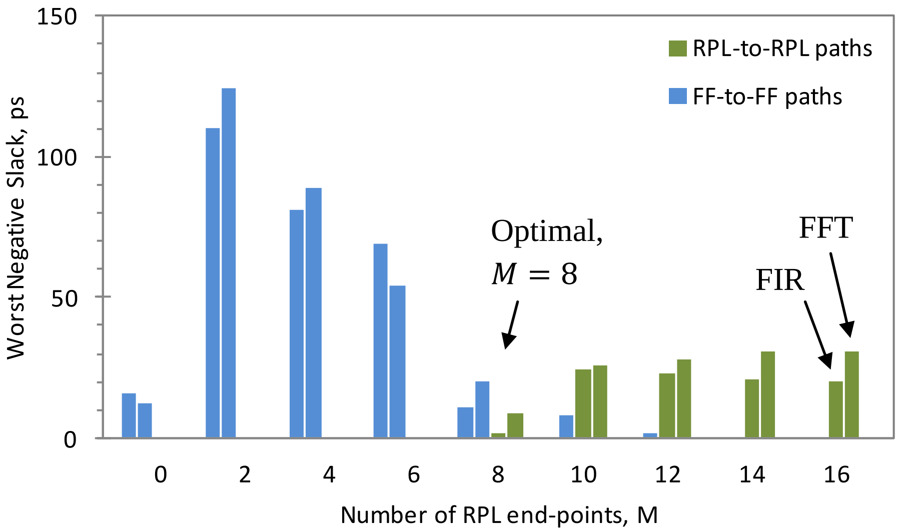


Figure 5.12: Number of RPL sequentials per pipeline stage vs. worst negative timing slack for FIR (left) and FFT (right) designs, normalised to $M = 0$.

Conversely, larger M generates negative slack in the RPL-to-RPL group as longer paths have been introduced that must meet a setup margin to allow for safe time-borrowing. Figure 5.12 shows the worst negative timing slack for implementations of the FIR and FFT designs. The optimal trade-off for speed is $M = 8$, at which point, the area overhead is 17% for FIR and 19% for FFT. There is no negative slack in the FF-RPL group as the propagation time is reduced for a RPL relative to a MSFF. This result demonstrates that the time borrowing approach to timing-error tolerance does not increase critical path length of speed optimised arithmetic pipelines.

5.4.4 Simulation Results

Extensive post-layout simulation work has been completed using HSIM to verify operation and measure the power dissipation of the proposed designs along with baseline conventional implementations. Layouts of the proposed FIR and FFT designs are given in Figure 5.13 and Figure 5.14, respectively. No hierarchy is visible for the FIR layout as the design was implemented “flat” to improve timing.

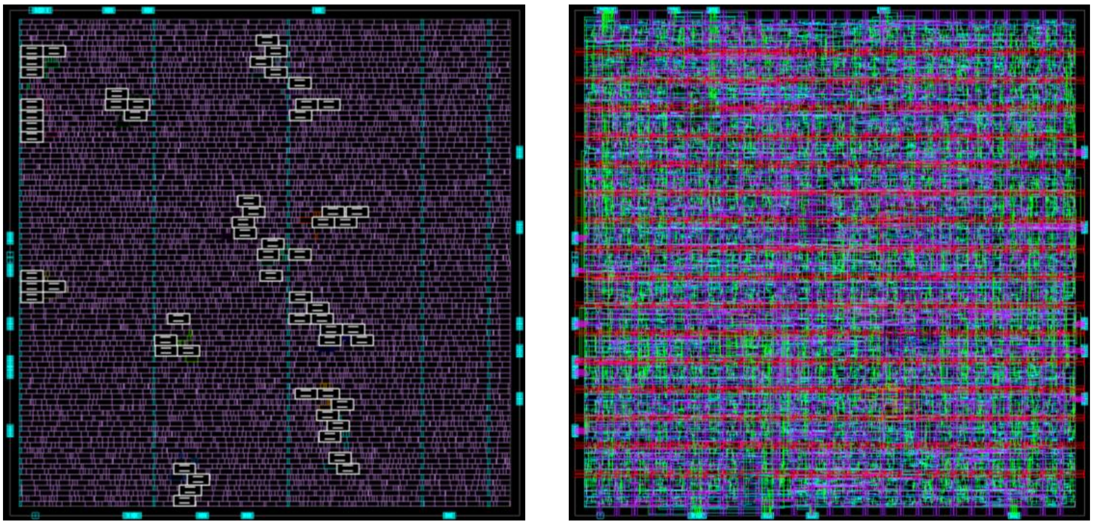


Figure 5.13: FIR standard cell layout (left), with double-height Razor flip-flop cells in white and with full metal stack (right). Layout area is 0.012 mm^2.

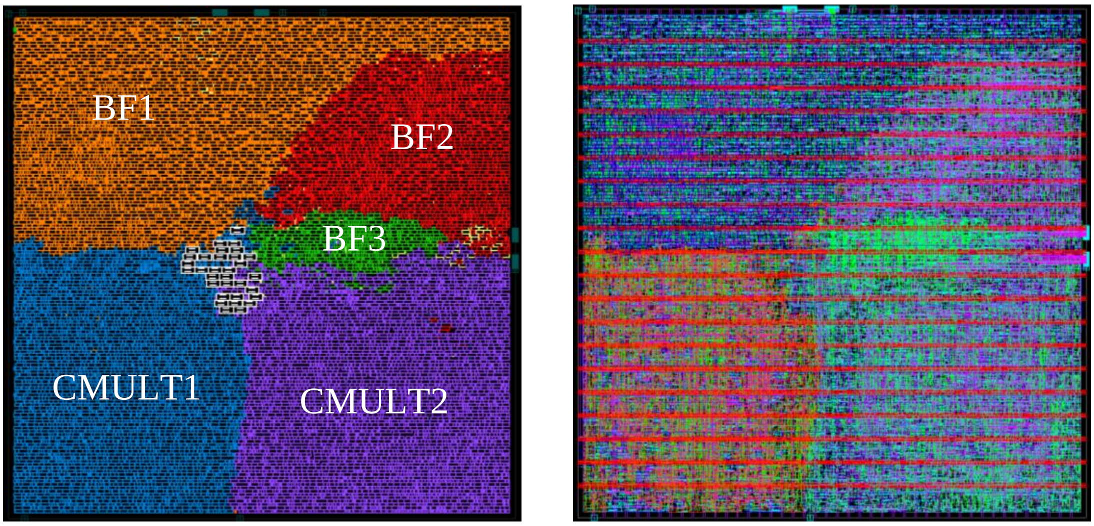


Figure 5.14: FFT standard cell layout (left), with double-height Razor flip-flop cells in white and with full metal stack (right). Layout area is 0.027 mm^2.

The FFT layout shows hierarchy for the three butterfly units ("BF") and the two complex multipliers ("CMULT").

Table I summarises the simulation results completed with TT process corner at 25°C. For these simulations, the supply voltage was kept constant for each operating point test. Due to the additional transition detector circuitry and timing constraints, the area and power dissipation increases compared to the baseline implementation at the nominal supply voltage, which includes full worst-case margin. However, the transition detectors allow us to reduce supply voltage until a low, but non-zero error rate is detected around 860 mV, at which point, the proposed FIR and FFT designs offer a power reduction of 21% and 25%, respectively, with no logical errors at the output. In addition to this power saving, the robustness was investigated by continuing to reduce the supply voltage below the point of first failure, until logic errors were detected at the output, i.e. catastrophic failure. This revealed a margin of 60-80 mV between the zero margin point and failure.

Table 5.1: Simulation Results at TT/25°C.

	Tclk	**Vdd**	**Power**
FIR (M=0)	0.9 ns	1 V	18.21 mW (WC margin)
FIR (M=8)	0.9 ns	1 V	19.43 mW (WC margin)
	0.9 ns	870 mV	14.45 mW (Zero Margin)
	0.9 ns	790 mV	12.56 mW (Failure)
FFT (M=0)	2.8 ns	1 V	14.71 mW (WC margin)
FFT (M=8)	2.8 ns	1 V	15.74 mW (WC margin)
	2.8 ns	860 mV	11.02 mW (Zero Margin)
	2.8 ns	800 mV	9.37 mW (Failure)

5.4.5 Hybrid DVS Control Loop Simulation

In order to verify the selective time borrowing approach in the context of a Razor DVS loop, extensive simulation work was conducted to verify the hybrid control loop and ensure that a sufficient time borrowing window exists for robust operation. A supply noise source, $y(t)$ was incorporated (Figure 5.5), which models fast transient supply noise generated by both the datapath itself and other circuitry sharing the same supply pins. Since $y(t)$ directly modulates the supply voltage, the circuit delays are equally affected. For the sake of brevity, suitable values for parameters N, M, K_C and K_I, were chosen, without discussion.

Simulation of the DVS loop takes a large number of cycles and therefore it is not possible to use fast SPICE simulation as the runtime is prohibitive. Instead, a methodology was used based on back annotated gate-level simulation, using linear delay scaling to approximate the effect of supply voltage scaling and noise. The delay scaling was calibrated at two points using results from fast SPICE simulation.

The simulation traces shown in Figure 5.15 illustrate the action of the conventional Razor control loop, with the FIR design filtering a noisy sine wave. The first two waveforms show the input, $x[n]$, and output, $y[n]$, of the FIR filter. The following two show the timing-error rate, $e`[n]$ and the supply voltage, which includes 60 mV of white noise. Notice that $e`[n]$ is periodic due to zero-crossings in $x[n]$, where sign extension on small numbers activates the critical paths. The control loop tries to respond to the intermittent sensitisation, resulting in transitions outside the time borrowing window and logic errors, which propagate to the primary output, visible as additional noise on the filtered output signal. The timing-errors manifest in the MSBs and hence the resulting logic errors result in large transient noise spikes.

Figure 5.16 shows the proposed hybrid control loop in simulation. Supply voltage scaling is now controlled directly by the canary circuit output bits, HI and LO. The intermittent timing-error rate information is used to calibrate the canary circuit, but does not directly modulate the supply voltage, and therefore no logic errors manifest.

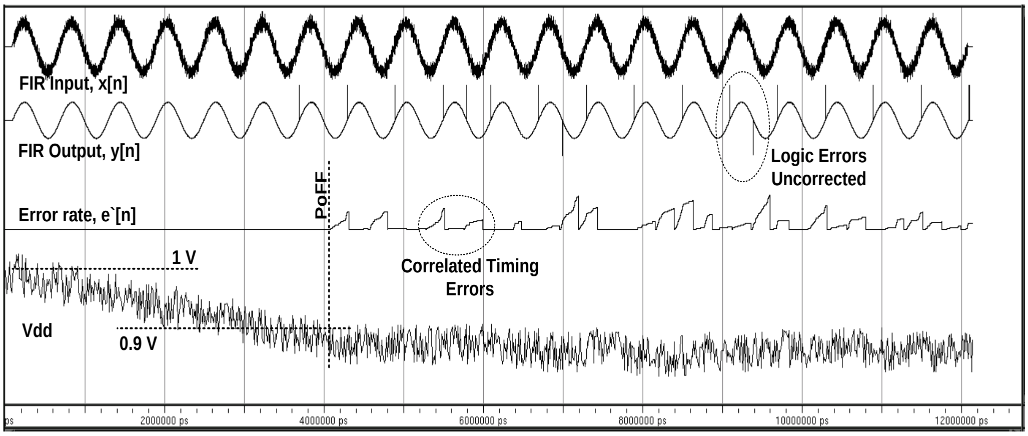


Figure 5.15: Simulation trace of FIR filter design with conventional control.

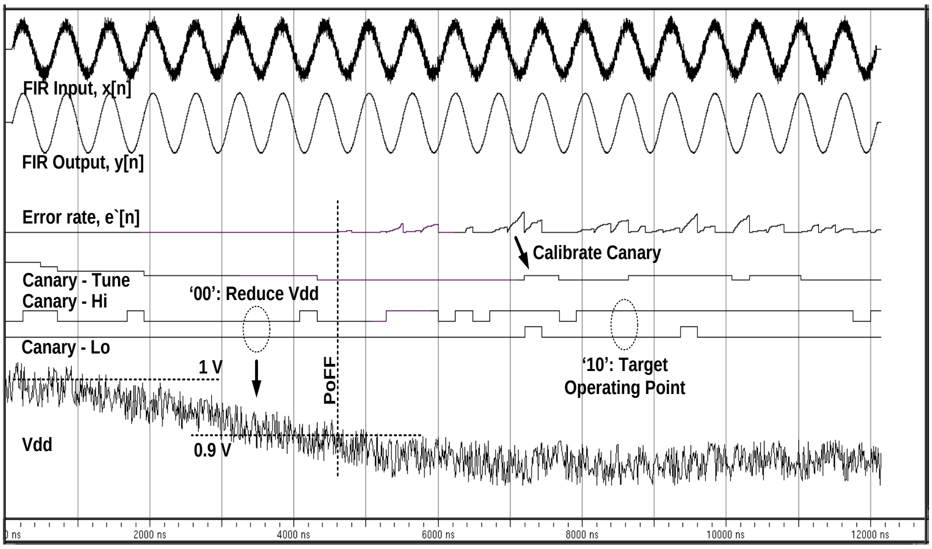


Figure 5.16: Simulation trace of FIR filter design with proposed hybrid control.

Despite the increased robustness of the hybrid controller, the main drawback observed is an increase in the initial loop convergence time while the canary is calibrated by the statistics of the in-situ timing-error rate.

5.5 Conclusions

In this chapter, the use of static time borrowing as a timing-error tolerance technique was demonstrated. It was shown that the path delay properties of fast addition and multiplication circuits exhibit significant imbalance that can be used to introduce time borrowing between stages without increasing the delay of the circuit. Using a Razor pulse latch, a transparent window was introduced only on selective end-points in order to avoid increasing hold time on fast paths. Tight control of supply voltage scaling is achieved using a novel approach of using timing-error detection to calibrate a canary circuit which circumvents the path activation problem.

The proposed approach was verified with FIR and FFT pipelines at high and medium performance points. In both cases selective time borrowing did not increase critical path length, unlike other timing-error tolerance approaches. The drawback is an increase in circuit area due to additional timing constraints on non-speculative FF end-points and also increased implementation effort due to use of a global pulse clock and pulse latches. The hybrid control loop was verified by simulation, demonstrating robustness to intermittent path activation and 60 mV of supply noise.

While the techniques presented thus far (Chapters 3–5) all demonstrate attractive power savings from reducing design margins (largely) at the circuit level, the greatest power savings are often achievable at the algorithm and VLSI architecture levels. To this end, the next chapter will take an exemplary look at the process of algorithm selection and mapping to VLSI architecture for an emerging DSP application in novel spectrally efficient communication systems.

Chapter 6. A Reconfigurable Spectrally Efficient FDM Baseband Transmitter

Future improvements in spectral efficiency will come at the cost of increased DSP workloads (c.f. Chapter 2). In this chapter, a recently developed modulation technique is studied, that seeks to improve spectral efficiency at the expense of an increase in algorithmic complexity. Spectrally Efficient FDM (SEFDM) systems employ non-orthogonal overlapped carriers to improve spectral efficiency for future communication systems. One of the key research challenges for SEFDM systems is to demonstrate efficient hardware implementations for transmitters and receivers and quantify the likely increase in circuit area and power dissipation.

Focusing on transmitters, this chapter explains the SEFDM concept and examines the complexity of published modulation algorithms, with particular consideration to implementation issues. Two new variants of a digital baseband transmitter architecture for SEFDM are then presented, based on a modulation algorithm which employs the Discrete Fourier Transform (DFT) implemented efficiently using the FFT. The algorithm requires multiple FFTs, which can be configured either as parallel transforms, which is optimal for throughput or using a multi-stream FFT architecture, for reduced circuit area. A simplified approach to IFFT pruning for pipeline architectures is proposed, based on a token-flow control style, specifically optimised for the SEFDM application. Reconfigurable implementations for different bandwidth compression ratios, including conventional OFDM, are easily derived from the proposed implementations.

The SEFDM transmitters have been synthesised, placed and routed in a commercial 32 nm CMOS process technology. Circuit area is reported and simulated power dissipation figures, which confirm the feasibility of SEFDM transmitters. The research in this chapter has been presented at the IEEE International Symposium on Circuits and Systems (ISCAS) [71] and was also published in extended form as an invited paper in IEEE Transactions on Circuits and Systems-I (TCAS-I) [52].

6.1 Introduction

In order to accommodate for the ever growing demand for bandwidth, SEFDM emerged as multi carrier communication system promoting higher spectral efficiency than the well known Orthogonal Frequency Division Multiplexing (OFDM). The first systems to appear were Fast OFDM (FOFDM) [72] and M-ary Amplitude Shift Keying (MASK) OFDM [73], both of which halve the spectrum utilisation, but are constrained to one dimensional modulations such as BPSK and MASK. Following this, came SEFDM [74], High Compaction Multicarrier-Communications (HC-MCM) [75], Overlapped OFDM (Ov-OFDM) [76] and Multi-stream Faster than Nyquist Signalling (FTN) [77][78][79] all of which promote variable spectral utilisation savings for two dimensional modulations. All variants of SEFDM systems are basically multicarrier modulation schemes that multiplex non-orthogonal overlapped sub-carriers. In principle, non-orthogonal multicarrier systems achieve spectral savings by either reducing the spacing between the subcarriers in frequency and/or transmission time, thus, communicating information at a faster than Nyquist rate. In theory, such spectral utilisation improvement is supported by the Mazo limit established in [80] stating that signalling at rates beyond the Nyquist can be achieved without performance degradation.

Despite the favourable spectral savings on offer, in practice, the loss of orthogonality complicates both signal generation and detection. For the detection problem, many detectors have been proposed and evaluated in the literature. Maximum likelihood (ML) is suggested for detection as the optimum technique in Additive White Gaussian Noise (AWGN) channels [72]. Nevertheless, ML detection is overly complex, with a computational complexity that grows exponentially with the size of the system. On the other hand, linear detectors, such as Minimum Mean Square Error (MMSE) and Zero Forcing (ZF), constrain the size of the SEFDM system in order to yield competitive Bit Error Rate (BER) performance [81]. Truncated Singular Value Decomposition (TSVD) based detection proposed in [82], has demonstrated improved error performance for systems with relatively large numbers of carriers. Furthermore, iterative detection in the form of Sphere Decoders (SD) proposed in [83] and [84] showed optimum BER performance with a decreased computational complexity which is later extended to fading channels in [85]. However, the variable complexity of the SD algorithms led to the proposal of the Fixed Complexity Sphere Decoder (FSD), where the complexity is tradable with error performance [86] and [87].

As for the generation of SEFDM modulated symbols, recent work has shown in [88] [89] [90] that the SEFDM signal can be realised with a similar complexity to

OFDM system, by utilising standard Inverse Discrete Fourier Transform (IDFT) blocks, judiciously arranged for SEFDM modulation. Minor modifications on the input streams are needed and the designs rely mainly on standard IDFT operations that can be efficiently realised with the Inverse FFT (IFFT) algorithm. However, there are a number of practical implementation challenges for SEFDM systems, most significantly the minimisation of area and power dissipation overheads which are critical in meeting market demands for manufacturing cost and end product battery life.

SEFDM transmitters using Field Programmable Gate Arrays (FPGAs) have been reported recently [91]. Meanwhile, practical VLSI implementation of the closely related FTN signalling scheme has been investigated in both FPGA and 65nm CMOS technology [79]. A first study of SEFDM transmitter VLSI implementation in 65nm CMOS technology was reported by the authors in [71], utilising an IFFT based architecture for a reconfigurable design which enables modification of signal subcarrier spacing and demonstrates the feasibility of ASIC integration. In addition to this prior work targeting wireless applications, there have also been a number of recent demonstrations of practical optical communications systems making use of SEFDM modulation [92][93][94] and reporting substantial increases in system capacity.

In this chapter, the work in [71] is significantly extended by adding novel contributions in three main areas. Firstly, a detailed algorithmic complexity analysis is presented, comparing asymptotic complexity for known SEFDM modulation algorithms over the dimensions of number of sub-carriers and also bandwidth compression ratio. Secondly, a novel VLSI architecture is introduced, based on the multi-stream FFT, which offers substantially reduced circuit area and power consumption compared to the previously published parallel approach. Both the parallel and novel multi-stream architectures resemble conventional OFDM modulators in that they are based on IFFT operations, with the former optimal for highest throughput and the latter offering a significant saving in circuit area and power dissipation. Both architectures can be reconfigurable for differing degrees of sub-carrier overlap, enabling the transmitter to switch from conventional OFDM to a more spectrally efficient FDM system on a symbol-by-symbol basis. Finally, a new implementation technique is reported to address the increase in silicon area and power dissipation required for SEFDM, relative to previous generations of OFDM transmitters [95], [96]. This is achieved by a novel application of token-flow control to perform IFFT pruning [97] of butterfly calculations and FIFO entries. Implementation results are given in 32nm CMOS.

6.2 The SEFDM System

A generic SEFDM system is shown in Figure 6.1. The signal is generated by the superposition of several non-orthogonal carriers each carrying a complex symbol denoted as $s = s_{\mathfrak{R}} + js_{\mathfrak{I}}$ to represent two dimensional modulations. The carriers in SEFDM systems are spaced by a fraction of the inverse of the symbol duration, thereby violating the orthogonality condition of the OFDM system, where the spacing is equal to the inverse of the symbol duration. The distance between the carriers in frequency, denoted by Δf, is given by $\Delta f = \alpha / T$, where α denotes the amount of bandwidth compression and T is the duration of one SEFDM symbol. Equation (6.1) gives the baseband-time domain representation of a single frame of an SEFDM signal denoted by $x(t)$.

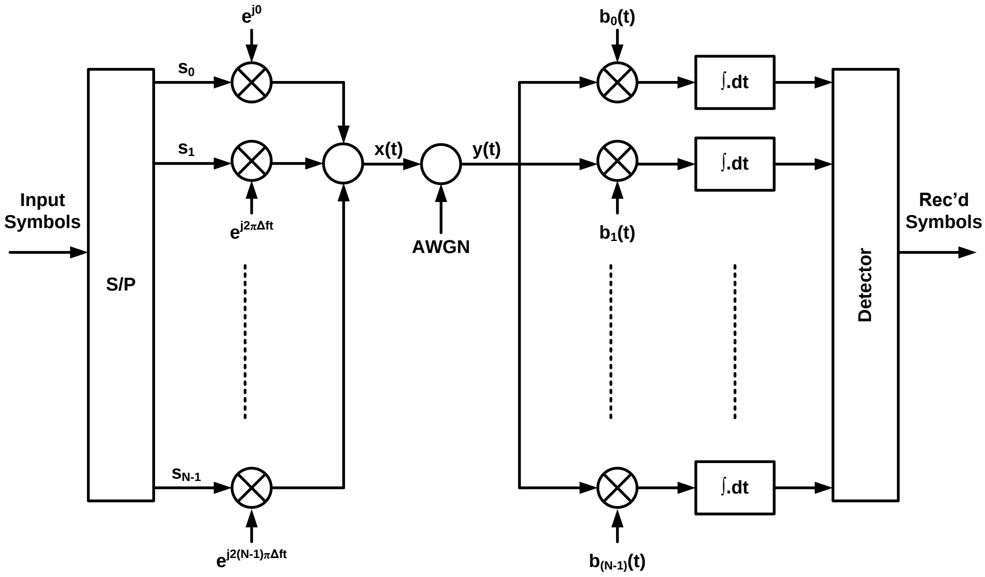


Figure 6.1: SEFDM conceptual block diagram.

A representation similar to that in [95] is followed, where N is the number of subcarriers, s_n denotes a complex valued symbol modulated on the n^{th} subcarrier and windowed by a time limited rectangular function $g(t)$ defined over the period $[0 - T]$.

$$x(t) = \frac{1}{\sqrt{T}}\left[\sum_{n=0}^{N-1} s_n\, e^{\frac{j2\pi n\alpha t}{T}}\right] \times g(t) \tag{6.1}$$

A discrete representation of SEFDM signals can be obtained by sampling each SEFDM frame, shown in (6.1), at a rate N/T. Thus, a single discrete SEFDM will be given by

$$X[k] = \frac{1}{\sqrt{N}}\sum_{n=0}^{N-1} s_n e^{\frac{j2\pi nk\alpha}{N}}, \tag{6.2}$$

where $k = 1, \dots, N$. In the next section it will be shown how the samples of the SEFDM signal as in (6.2) can be generated based on IDFT operations [88].

At the receiver, the SEFDM signal contaminated by AWGN, $w(t)$, is represented by

$$r(t) = x(t) + w(t). \tag{6.3}$$

The SEFDM receiver generates statistics of the incoming signal, $r(t)$, through employing the dual of the transmitter operations [86], [87]. Such statistics are fed to a detector to generate estimates of the transmitted signal [74]. Many techniques have been investigated for the detection of SEFDM signal [74], [76] and it is confirmed that successful detection is achievable for wide range of bandwidth compression levels. As a demonstration, Figure 6.2 is provided to illustrate the BER performance of a received SEFDM signal detected with the modified FSD algorithm [87]. The curves in the figure demonstrate slight error performance degradation for attractive bandwidth savings.

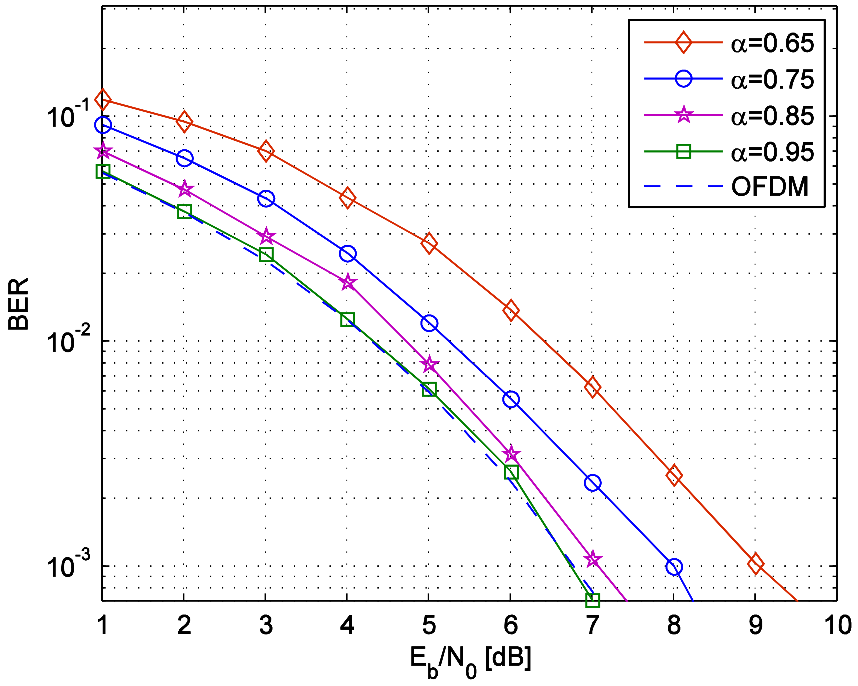


Figure 6.2: BER performance of a 16-subcarrier SEFDM system carrying QPSK symbols for $\alpha = 0.6 - 0.9$ ($\alpha = 1$ corresponds to OFDM).

The preceding analysis in AWGN channels is included here as a general introduction to SEFDM system performance. Notwithstanding, the effects of frequency selective fading are of key significance and transmission over different fading channel conditions is an important area of study for wireless systems. Operation under various frequency selective fading conditions in [85] and [98] has shown the suitability of joint equalisation and detection, leading to the development of bespoke SEFDM channel estimation techniques. Furthermore, recent work on SEFDM has reported lower Peak to Average Power Ratio (PAPR) relative to an equivalent OFDM signal [98]. This is an important advantage, as it relaxes the detrimental effects of analogue front end non-linearities and allows improved efficiency in the RF power amplifier, which can be enhanced further using a PAPR reduction algorithm for SEFDM signals [99]. Additionally, various techniques for signal precoding, optimised for specific values of bandwidth compression and number of carriers, to facilitate simplified reception and decoding, have been published recently [100]. However, the details of signal coding, fading channel and PAPR reduction are beyond the scope of the work presented here, which focuses on transmitter implementation aspects.

6.3 IDFT Based SEFDM Modulation Algorithms

6.3.1 General Description

Equation (6.2) describes the samples of the discrete SEFDM signal. In analogy to OFDM, it is shown that the SEFDM signal can be expressed by IDFT operations [88]. It is shown that there are ways to express the SEFDM signal with an IDFT operation with simple manipulations of the input symbol vectors. These manipulations are merely in the form of zero insertions either at the end of the vector

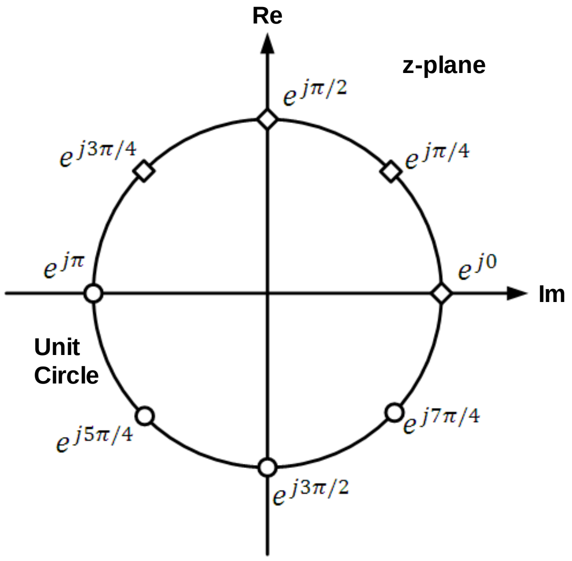


Figure 6.3: Unit circle representation of the relationship between the frequency samples of SEFDM system (diamonds) and IDFT operation (diamonds and circles).

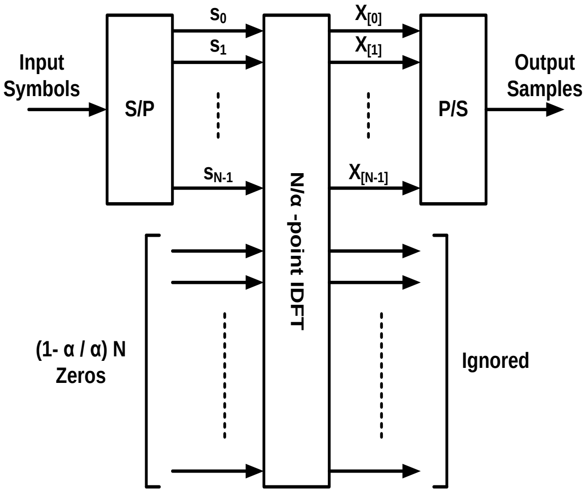


Figure 6.4: Generating SEFDM signal using Type-I algorithm, based on a single IDFT operation.

only, in a manner similar to zero padding and/or between the symbols. The change in length ensures the alignment of the IDFT frequency samples and the SEFDM subcarriers and the zeros suppress the unwanted frequencies. Figure 6.3 illustrates how the frequency samples are related to the IDFT samples, depicting the frequency samples of a 4-carrier SEFDM system for $\alpha = 0.5$ and the frequency samples of an 8-point IDFT operation on the unit circle of the complex z-plane. The figure shows that the SEFDM system is equivalent to the 8-point IDFT of a vector whose last 4 elements are equal to zero.

For integer values of N/α $\left(i.e\ \frac{N}{\alpha} \in \mathbb{Z}\right)$, the work in [88][89][90] shows that a discrete SEFDM signal $X[k]$ can be described as

$$X[k] = \acute{X}[k], \qquad for\ k = 1, \dots, N \tag{6.4}$$

where

$$\acute{X} = F^{N/\alpha}\{\acute{S}\} \tag{6.5}$$

and $F^{N/\alpha}\{\cdot\}$ is the N/α point IDFT of the argument , with $\acute{S}$ being a vector of length N/α ,whose elements $\acute{s}_i$ take the values of either input symbols s_i or zeros as:

$$\acute{S} = \begin{cases} s_i, & 0 < i < N \\ 0, & N \leq i < N/\alpha \end{cases} \tag{6.6}$$

Thus, the SEFDM signal can be realised with a single IDFT block, with a length longer than N, which is referred to as the Type-I modulation algorithm. The SEFDM transmitter in this case is depicted in Figure 6.4.

Furthermore, it is shown in [91] that by expressing the term α as a rational number, that is by taking $\alpha = b/c$, where both b and c are integers and $b < c$, the SEFDM signal can be expressed as

$$X[k] = \frac{1}{\sqrt{N}} \sum_{n=0}^{cN-1} s'_n\, e^{\frac{j2\pi nkb}{cN}}, \tag{6.7}$$

As for the case above, S' is defined to be a vector of length cN whose elements s'_i take the values of either the input symbols $s_{i/b}$ or zeros as:

$$S' = \begin{cases} s_{i/b}, & i \in I \\ 0, & otherwise \end{cases} \tag{6.8}$$

and $I = \{0, b, \dots, b(N-1)\}$. Equation (6.7) can be rearranged as

$$X[k] = \frac{1}{\sqrt{N}} \sum_{i=0}^{c-1} e^{\frac{j2\pi ib}{cN}} \sum_{m=0}^{N-1} s'_{i+mc} \, e^{\frac{j2\pi mk}{N}}, \tag{6.9}$$

by substituting with $n = i + mc$.

Equation (6.9) clearly shows that the samples of the SEFDM signal can be generated using c IDFT operations each of length of N points. The input symbols are padded with $(c-1)N$ zeros and then arranged as a $c \times N$ matrix in column major order. An IDFT operation is then performed on each row. The signal is finally composed by combining rotated versions of the IDFT outputs as depicted in Figure 6.5. This approach using multiple IDFT operations is referred to as the Type-II algorithm.

6.3.2 Algorithm Complexity Analysis

The major advantage of the IDFT based generation of the signal is the reduction in complexity. The computational complexity of the directly generated SEFDM signal as in (6.2) is N^2 complex multiplications and $N(N-1)$ complex additions. In a digital system, this would typically be implemented using Direct Digital Synthesis (DDS) [101], with asymptotic complexity of $\mathcal{O}(N^2)$. On the other

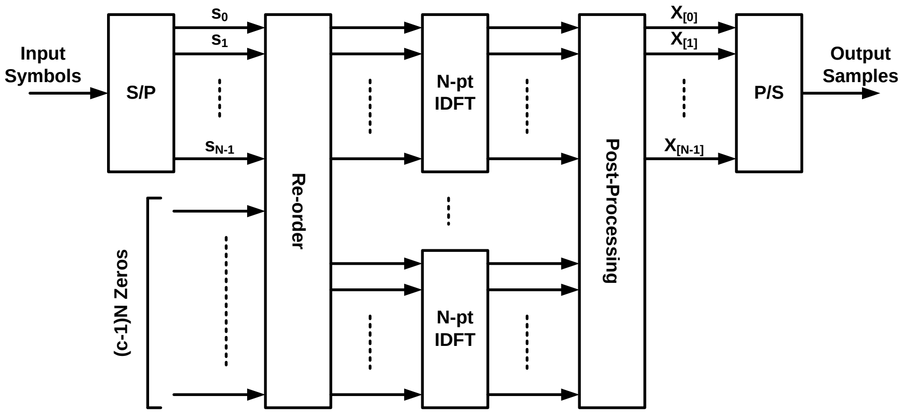


Figure 6.5: SEFDM IDFT based transmitter using Type-II algorithm with multiple IDFT operations.

hand, the IDFT based transmitters can be economically realised by means of the FFT algorithm with complexity of $\mathcal{O}(N \log_2 N)$. The complexity of the Type-I algorithm is given by a single large IFFT with N/α points, thus

$$\mathcal{O}(N/\alpha\ log_2\, N/\alpha). \tag{6.10}$$

By contrast, the complexity of the Type-II transmitter is a combination of the complexity of c IFFT blocks each of length N, giving

$$\mathcal{O}(c.N\ log_2\, N). \tag{6.11}$$

Figure 6.6 illustrates the complexity of the two proposed IFFT SEFDM modulation algorithms (with $\alpha = 2/3$), along with the DDS approach and conventional OFDM, as a function of N. Clearly the Type-I algorithm requires fewer operations than Type-II for the same value of c and N. Both proposed approaches require several orders of magnitude fewer operations than DDS for many combinations of N and c. However, even the Type-I algorithm demands a significant increase in computational power compared to conventional OFDM.

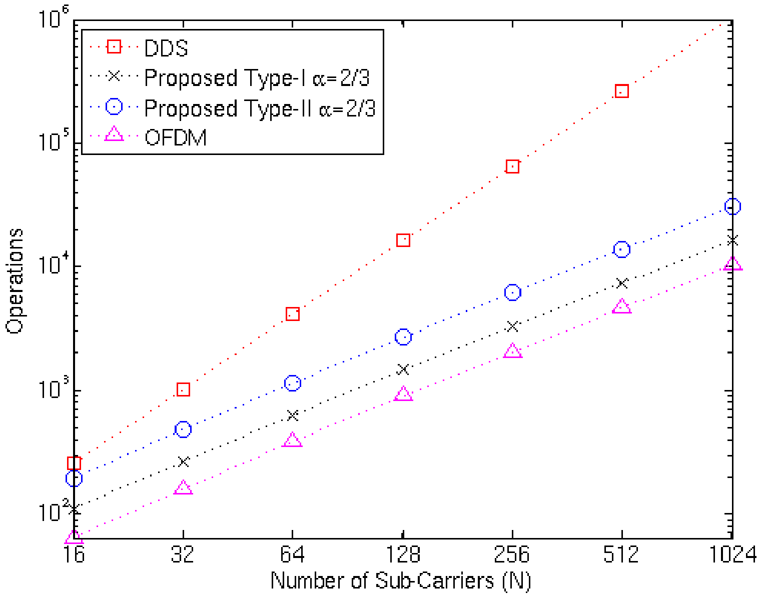


Figure 6.6: Asymptotic complexity of DDS and IDFT based SEFDM modulation algorithms as a function of *N*. Conventional OFDM is included for comparison.

It is important to note that, unlike the DDS approach, the complexity of IFFT-based algorithms varies not only with dimension N, but also α. To this end, Figure 6.7 shows how the complexity of the proposed algorithms varies as a function of α, for $N = 64$. Since the number of IFFT points required by the Type-I algorithm is given by N/α, with large values of α, the complexity is reduced. Conversely, the Type-II algorithm exhibits increasing complexity with α.

Due to the zero padding operations previously described, both IFFT based modulation algorithms require the computation of IFFTs with a number of zero bins. There is thus scope to "prune" the IFFT trellis to remove redundant operations with zero-operands [97][102]. For a transform of size N, with K non-zero inputs, the complexity for a maximally pruned IFFT tends to $\mathcal{O}(N log_2 K)$. Hence, ideally pruned versions are also considered, where all operations with zero operands are skipped. Thus the ideally pruned Type-I modulation algorithm achieves complexity of

$$\mathcal{O}(N/\alpha \; log_2 N), \tag{6.12}$$

and the ideally pruned Type-II is lower bounded by

$$\mathcal{O}\big(c.N \; log_2(N/c)\big). \tag{6.13}$$

These are also plotted in Figure 6.7 for comparison. Generally, the pruned Type-I algorithm shows little benefit, especially for larger bandwidth compression ratios where there are very few zero bins in the single large transform. The number of zero bins in the Type-II algorithm increases with bandwidth compression ratio and hence using a pruned transform gives an increasingly beneficial complexity reduction. In general, it is often difficult to achieve such a complexity reduction in a hardware implementation and hence the asymptotic notation is merely a lower bound in practice, as previously discussed.

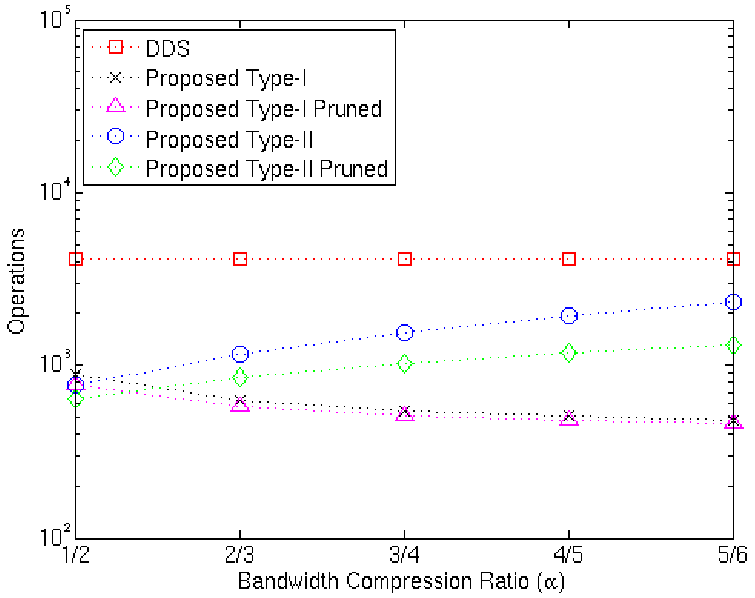


Figure 6.7: Asymptotic complexity of DDS and IDFT based SEFDM modulation algorithms as a function of α, with $N = 64$. Conventional OFDM is included for comparison.

In summary, both IFFT based algorithms show a strong advantage in complexity reduction compared to the directly generated DDS approach. Since they are based on IFFT blocks, there is also excellent compatibility with existing systems for multi-carrier orthogonal signalling. However, the number of IFFT points required for the Type-I algorithm (N/α) often results in non integer and/or non power of 2 values and consequently is only suitable for a small subset of possible parameters, i.e. where $(N/\alpha) \in 2^{|\mathbb{Z}|}$. Hence, although the Type-II algorithm has less attractive complexity, which increases with α, it is better suited to hardware implementation using IFFT blocks. Since the length N IFFT is common to conventional OFDM transmitters, it is possible to re-use this block, retaining backward compatibility with the incumbent OFDM systems. Advantageously, an SEFDM receiver may use the dual of the transmitter algorithm, and thus all the optimisations described in this chapter, while focused on the transmitter, are equally relevant to receiver implementation.

6.4 VLSI Architecture

6.4.1 Parallel Transform Architecture

In this section, a VLSI architecture is described which results from directly implementing the Type-II SEFDM signal generation algorithm previously described. Such an architecture is based on parallel length-N IFFTs which are the key building blocks of current OFDM transmitters and are therefore attractive both for reasons of back-wards compatibility and general familiarity. For the sake of brevity, only aspects that differ from the traditional IFFT-based OFDM transmitter [96] are described. The algorithms previously presented are suitable for the generation of signals with arbitrary values of α, but complexity and power dissipation rise linearly with c, so implementations optimised for $\propto \in \{1, ½, ⅔, ¾\}$ are considered, which are realistic values for practical systems.

A reconfigurable transmitter with adjustable sub-carrier spacing is also attractive for two key reasons. Firstly, it allows us to adapt α in order to maximise the trade-off between receiver complexity, spectral efficiency and prevailing channel conditions. Secondly, supporting $\alpha = 1$ allows us to maintain backward compatibility with the many incumbent OFDM systems. To this end, it is ensured that α can be reconfigured for each FDM symbol. M-ary digital QAM modulation is assumed for sub-carrier symbols, and do not consider mapping of pilot symbols.

Figure 6.8 shows a high-level block diagram of the reconfigurable SEFDM IFFT-based transmitter for $c = 3$, with a pipeline radix-2^2 IFFT implementation [103]. The modulator consists of zero-insertion and re-order, the c parallel IFFTs and post-processing, as discussed individually in the following sections.

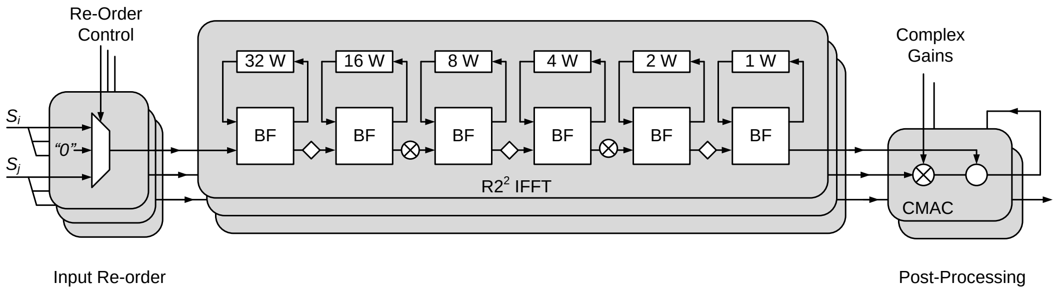


Figure 6.8: Parallel SEFDM transmitter architecture, consisting of input re-order logic, parallel IFFTs and post-processing complex multipliers. Diamonds represent trivial complex multiplications.

$$\begin{bmatrix} s_0 \\ \vdots \\ s_{N-1} \end{bmatrix}_{N\times 1} \Rightarrow \overbrace{\begin{bmatrix} s_0 \\ 0 \\ \vdots \\ s_{b-1} \\ \vdots \\ s_{N-1} \\ 0 \\ \vdots \\ 0 \end{bmatrix}_{cN\times 1}}^{Zero\ insertion} \Rightarrow \overbrace{\begin{bmatrix} S'_0 & \cdots & S'_{cN-1-c} \\ \vdots & \ddots & \vdots \\ S'_{c-1} & \cdots & S'_{cN-1} \end{bmatrix}_{c\times N}}^{Column\ major\ reorder}$$

Figure 6.9: General operation of symbol re-ordering for arbitrary b/c. The resulting matrix arising from the column major reordering of the preceding vector S' (defined in (8)) which is derived from the input symbol vector, and contains cN complex values.

6.4.1.1 Zero Insertion and Reorder

Figure 6.9 illustrates the general symbol re-ordering operation, which consists of padding the input symbols with $(c - 1)N$ zeros before arranging them as a $c \times N$ matrix in column major order. A naive implementation of this operation implies a buffer of cN complex words to hold the sparse complex matrix. However, since each incoming symbol is mapped to only one IFFT input, it is only necessary to use a multiplexer in front of each IFFT to choose either the incoming s_i symbol or $(0 + j0)$ sample.

The control signals required to operate the multiplexers are generated by modulo arithmetic operations on a $\log_2(cN)$-bit counter, which reconfigures for different b/c parameters. In our optimised implementation, this process is replaced with a LUT containing addresses for pre-set values of b/c. To keep the parallel IFFT pipelines fed, $\lceil c/b \rceil$ read ports are required in the preceding symbol buffer. However, since the detection of SEFDM signals of $\alpha < 1/2$ incurs an increasing BER penalty, only $b \geq c/2$ is of generally interest and hence the maximum number of read ports required is restricted to two, in order to provide symbols S_i and S_j in parallel on each clock cycle.

6.4.1.2 Parallel IFFTs

The N-point IDFTs are implemented in this section as c N-point IFFTs, which can be implemented as c parallel IFFT blocks or as a smaller number of time-multiplexed blocks, which is considered in the next section. Using c parallel IFFTs allows the highest throughput and constant latency independent of α, at the cost of linear increase in area and power. 64-point, 16-bit complex IFFT blocks are used, based on the radix-2^2 flowgraph [103]. The IFFTs have an enable signal which when de-asserted gates the internal clock and clears the output registers to zero.

6.4.1.3 Post-Processing

The post-processing operation combines the parallel IFFT outputs after multiplication with a complex exponential in order to produce the discrete-time output samples, $X[k]$. The complexity of the post-processing is a linear function of c, where $(c - 1)$ complex multiply-accumulate (CMAC) operations are required. The hardware required includes the CMACs and LUTs to store pre-calculated rotation coefficients in read-only memory (ROM). A total of $(c - 1)$ LUTs are required for each configuration. Due to inherent symmetry in the rotation coefficients, the storage required can in practice be easily reduced to the range $[0, \pi/2]$ per LUT at the cost of increased complexity in the address generator logic, which is subsequently required to count both up and down the LUT and requires a conditional negation of the output value. For higher performance implementations, the critical paths through the complex multipliers form a feed-forward cutset that can be arbitrarily pipelined to meet throughput requirements at the cost of additional latency.

6.4.2 Multi-Stream Transform Architecture

The previously described parallel architecture is able to maintain iso-throughput for all compression modes. However, this requires an investment in circuit area proportional to $max\{c\}$ over all modes. Such an increase in silicon area is obviously prohibitive for large values of c and also possibly detrimental to power efficiency due to sub-threshold leakage.

An alternative to the systolic implementation is to use m time-multiplexed IFFTs and CMACs, which in the extreme case of $m = 1$, requires only a single IFFT and CMAC with sufficient storage to hold the N intermediate accumulation results. This approach implies a reduction in throughput proportional to m/c, and an increase in latency proportional to c. The reduction in throughput can be compensated by increasing the clock frequency to maintain comparable throughput at significantly lower silicon area. It is acknowledged that this approach has a practical limitation in that providing a derived clock at arbitrary integer multiples of the sample rate is not trivial and may require an additional clock synthesiser.

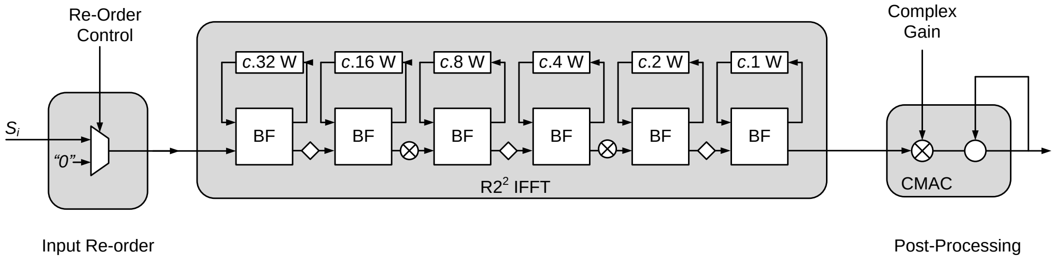


Figure 6.10: Multi-stream implementation of SEFDM transmitter, consisting of input re-order logic, multi-stream IFFT with extended FIFOs and single post-processing complex multiply accumulate stage. Diamonds represent trivial complex multiplications.

To avoid having to store a whole time-domain symbol in the serial implementation, it is possible to instead use a multi-stream IFFT, as illustrated in Figure 6.10. This idea is already well known from Multiple-Input Multiple Output (MIMO) transmitters which require multiple IFFTs to modulate separate data streams for multiple antennas [104]. The multi-stream IFFT accepts alternately interleaved samples from a number of input streams on successive cycles, such that transformed output samples appear at the output, as opposed to transforming the whole symbol at once. This means that it is only necessary to buffer a single sample at the output in order to complete the complex multiply-accumulate. It also significantly reduces the latency. The main drawback with the multi-stream IFFT approach is that it requires an increase in internal storage by a factor of c.

With a multi-stream IFFT, the symbol re-order block is only required to generate a single complex sample per cycle and therefore reduces to a single multiplexer, presuming the modulated sub-carrier symbols are suitably arranged in a preceding buffer. For low throughput systems, it is also possible to replace the CMAC with the COrdinate Rotation Digital Computer (CORDIC) algorithm to reduce further circuit area and power dissipation [105].

6.4.3 Optimised IFFT for Sparse Inputs

The final $c \times N$ re-ordered matrix of Figure 6.9 contains $(c-1)N$ zero symbols, which leads to redundant operations with zero operands in the initial stages of the IFFT algorithm. It is important to take advantage of this to efficiently implement modulators for large ratios of α. In software approaches, it is relatively straightforward to optimise away the redundant butterfly (BF) operations and at the same time reduce the storage requirement [97]. However, in hardware, it is often difficult to implement pruned IFFTs because they lose special regularity in the signal flow graph, which is important to retain for efficient implementation. Hence, instead, s simple approach is proposed to reduce the storage requirement and the number of Butterfly (BF) operations to be calculated. Our analysis focuses on the well known radix-2^2 pipeline architecture, which is particularly popular for OFDM systems, the main advantage is that the same number of multiplications are required as a radix-4 algorithm, but with only simple radix-2 butterflies and a very regular topology.

In order to entirely prune a radix-2 BF operation, both complex inputs need to be zero. When only one complex input to a BF is zero, it cannot be pruned per se, but can be simplified to either a simple mapping to two output nodes or a mapping with negation, as shown in Figure 6.11. In the following sections, two practical approaches to pruning IFFTs for sparse inputs are described. The first allows an entire BF stage to be removed for some ratios of α, while the second is suitable for all α and allows clock gating of BF datapaths for pruned operations, which reduces the energy cost of the redundant operations

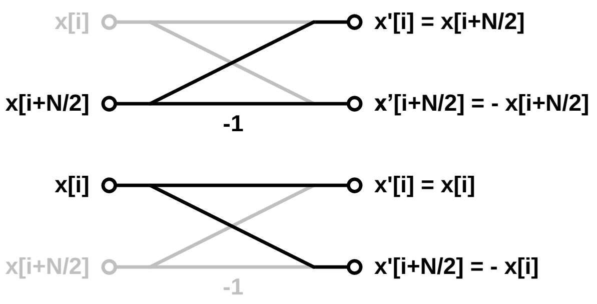


Figure 6.11: Partially-pruned half BFs occur when one of the complex inputs is zero.

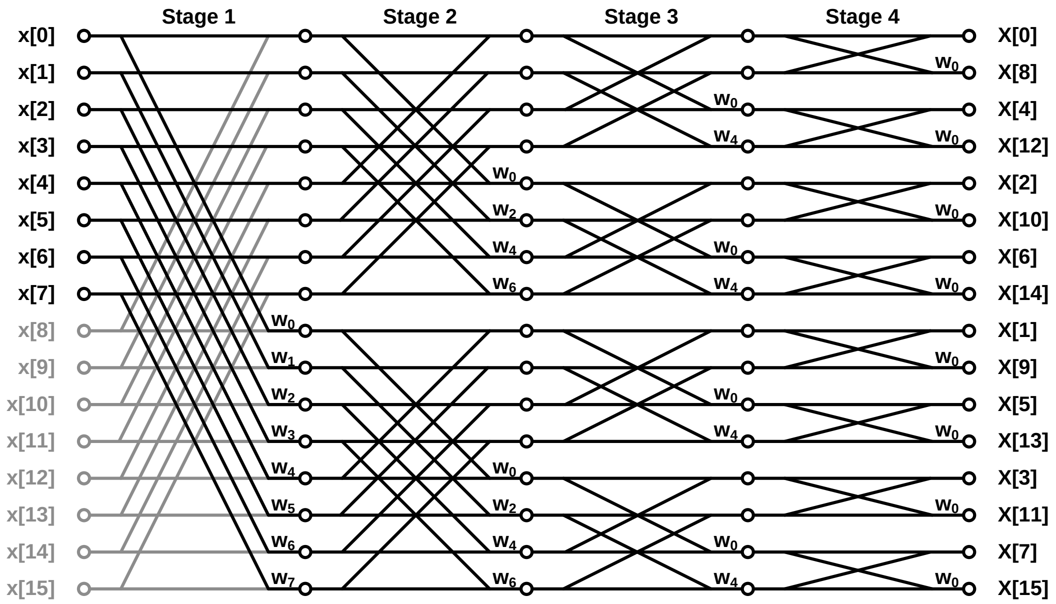


Figure 6.12: IFFT signal flow graph for $\alpha = 1/2, N = 16$. Grey edges of graph are redundant, leading to removal of the first stage by replacing the BF operations with a mapping operation which repeats the first $N/2$ points into the complex multipiers, requiring no additional hardware

6.4.3.1 Whole trellis stage pruning for $\propto \leq 1/2$

In this case, the re-ordered zero bins (c.f. Figure 6.9) are arranged in a compact manner such that non-zero bins are followed by at least $N/2$ contiguous zeros. Hence, the first IFFT trellis stage contains only half BFs and can be pruned entirely up to the input to the first complex multiplier, removing $c(N/2)$ BF operations and $c(N/2)$ complex words of storage. Figure 6.12 shows the IFFT signal flow graph for $\alpha = ½$, showing the grey edges which are redundant.

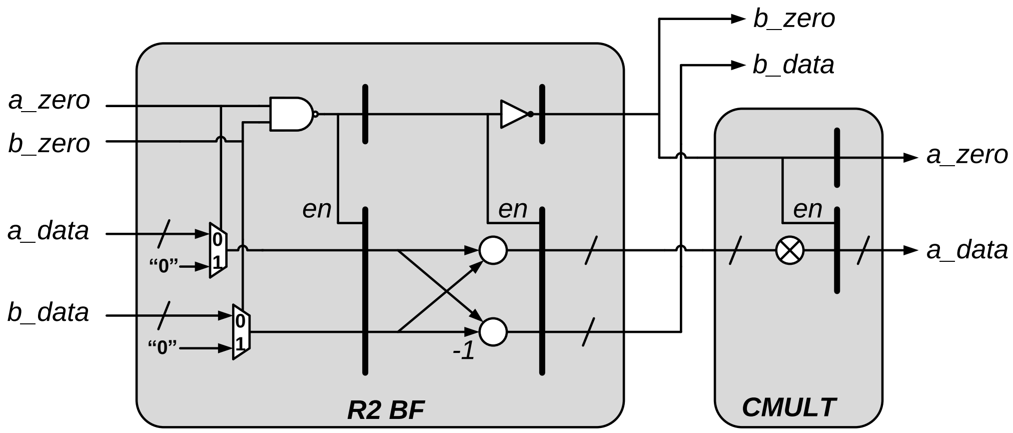


Figure 6.13: Optimised BF and complex multiplier datapaths with clock gating for pruned operations controlled by zero flags which accompany the two complex operands. Both zero flags are cleared if one of the operands is non-zero. All datapath arithmetic

Unfortunately, as previously mentioned, bandwidth compression ratios less than ½ incur a BER penalty and hence this optimisation is only really applicable to $\alpha = ½$, at least in this particular application.

6.4.3.2 BF clock gating for $\propto > 1/2$

For larger values of α, zero bins are less regularly distributed in the trellis and it becomes increasingly difficult to implement a pruned algorithm, especially in the case of a reconfigurable α. Therefore, a sub-optimal pruning approach is implemented, based on token-flow style control which allows us to clock gate BF stages and complex multipliers when the input operands are zero and also use an optimised FIFO which reduces the required storage significantly, using the same mechanism.

Figure 6.13 shows the general approach to reducing power in BFs and complex multipliers with zero input operands. Each 32-bit complex operand a_data and b_data is associated with a 1-bit zero flag a_zero and b_zero, which is initially generated by the input re-ordering logic. The zero flags then follow the datapath and is cleared only when a BF operation is performed on one zero and one non-zero operand. The flag enables simple control of datapath clock gating (illustrated in Figure 6.13 with the en input to the registers), such that register clock pins are isolated from the clock tree when a redundant BF or complex multiplication occurs. Since both the input and output registers are gated in this case, power is saved both in switched datapath capacitance and the clock tree driver load. The area and power overhead of the logic for the zero flag is negligible.

6.4.4 Optimised FIFO storage

It is well-known that FIFO storage in pipeline FFTs consumes significant area and power, a problem which is multiplicatively worse in the case of either a multi-stream transform or equivalent parallel transforms. The FIFOs implement a fixed delay in order to establish the necessary stride between data moving through the trellis. As such, these structures are often implemented using serially connected registers. The power cost of this Shift Register (SR) structure is significant, since all the flip-flops are clocked on every cycle where the module is active, in order to shift every data item to the next register. Because the clock load increases with the FIFO length, the SR structure exhibits poor power efficiency. A dual-port (one read port, one write port) SRAM macro can perform a similar function to the SR with the addition of simple addressing logic, but is not area effective for such a relatively small number of words. Register files consisting of static latches offer low area and power [106], but generally require a semi-custom design approach, so are not considered here.

Instead of moving the data every cycle, a Ring-Buffer (RB) FIFO style is implemented, where instead of moving all data bits on every cycle, a circular pointer is updated to enable only the register that is to be written [107]. All registers except

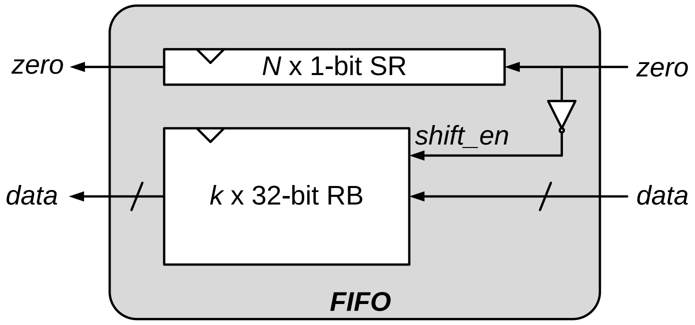


Figure 6.14: Optimised FIFO with clock gated FIFO of k entries and single 1-bit shift register (SR) of length N.

the one to be accessed can be clock gated, which reduces the clock load drastically, while the register that is to be read is addressed by the pointer using a combinatorial read-out path. Unlike the SR, the RB has a clock load which is approximately independent of the number of entries and is therefore well suited to the current design where there are significant numbers of such FIFO arrays.

The zero flag is used to enable a reduction in the internal storage requirement of the IFFTs (both in the multi-stream and parallel architectures), leading to further savings in area and power. It is not necessary to use a full 32-bit complex word to represent the sparse $(0 + j0)$ samples. Instead, zero-samples are compressed in the FIFO buffers by storing only a single bit in a full-length 1-bit FIFO buffer, as illustrated in Figure 6.14. When the $zero$ flag is asserted, the main array is not accessed and the $shift\_en$ bit goes low which is used to gate the clock, reducing switching activity when reading or writing a zero sample. Furthermore, the size of the array itself is reduced to k words, where in the case of the otherwise largest FIFO, at the first stage, k is independent of c and stays fixed at 32 words, instead of $32c$ words, since the number of non-zero bins stays fixed at N (c.f. Figure 6.5).

6.5 Implementation Results

The proposed architectures have been implemented in Verilog and verified using RTL simulation and FPGA prototyping. The designs were implemented in a commercial 32nm low-leakage CMOS cell library using standard-cell logic synthesis, APR and STA tools. Synopsys PrimetimePX was used for power estimation at TT process corner, nominal supply voltage and 25°C temperature. For a baseline comparison, results for a conventional OFDM modulator are also presented, which consists of a single IFFT module. All designs were constrained to an achieved clock period of 10 ns, which was verified at the SS 125°C corner using STA with suitable manufacturing margins.

6.5.1 FIFO Implementation

To illustrate the trade-offs between FIFO implementation styles, the SR and RB FIFOs previously described have been implemented. Figure 6.15 shows circuit area17 and power dissipation from simulation for FIFOs with 32 words down to 8 words from a 64-point pipeline IFFT (smaller buffers are required but have been omitted for clarity). The RB design was found to exhibit a power dissipation reduction of 78 % compared to the traditional SR. The reason for the significantly lower power dissipation is that the SR clocks every flip-flop in the structure on every cycle and hence area and power both increase with number of words. The RB only clocks the flip-flops in a single entry per cycle, which is independent of the number of entries. The RB power dissipation does increase somewhat as the circular address pointer size increases and, more significantly, the multiplexer structure in the read-

[17] Circuit area results are given in equivalent gates, by normalizing to the area of a 2-input NAND cell (NAND2X1) from the employed cell library.

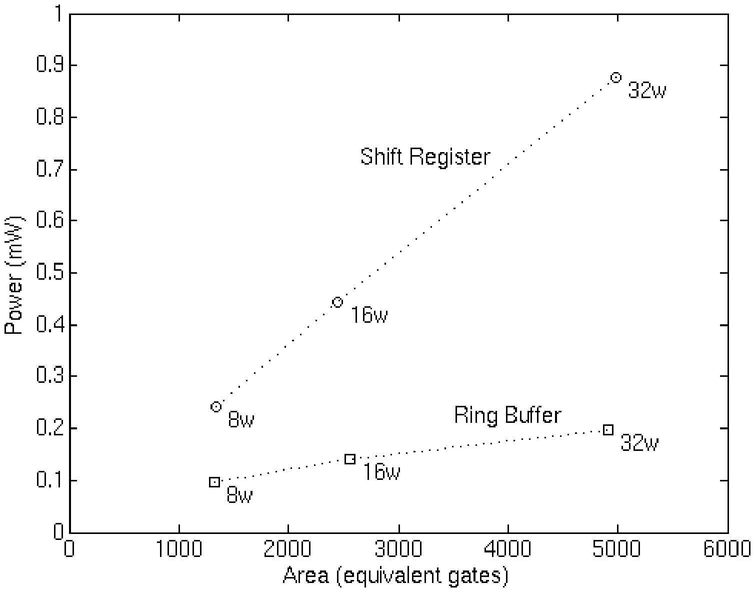


Figure 6.15: Area and simulated power consumption of SR and RB FIFO styles for the larger sizes required for a 64 point Radix-2^2 transform. Complex word size is 32 bits, clock frequency is 100MHz.

out path also increases in size. The RB FIFO is key to addressing power efficiency in multi-stream pipeline IFFTs and is used exclusively in the following implementations.

6.5.2 Parallel and Multi-Stream Architectures

Figure 6.16 shows results for parallel and multi-stream implementations of modulators for bandwidth compression ratios of 1, ½, ⅔ and ¾. The parallel architecture gives a linear area and power cost proportional to c as all the designs operate at the same clock frequency of 100 MHz. The multi-stream architecture requires an increasing clock frequency constraint which tends to require logic gates with larger device sizes leading to a somewhat non-linear increase in circuit area and power dissipation. Generally, the multi-stream architecture is more suited to area constrained designs, while the parallel architecture can reach minimum power consumption. The fully parallel $(m = c)$ and multi-stream $(m = 1)$ are merely

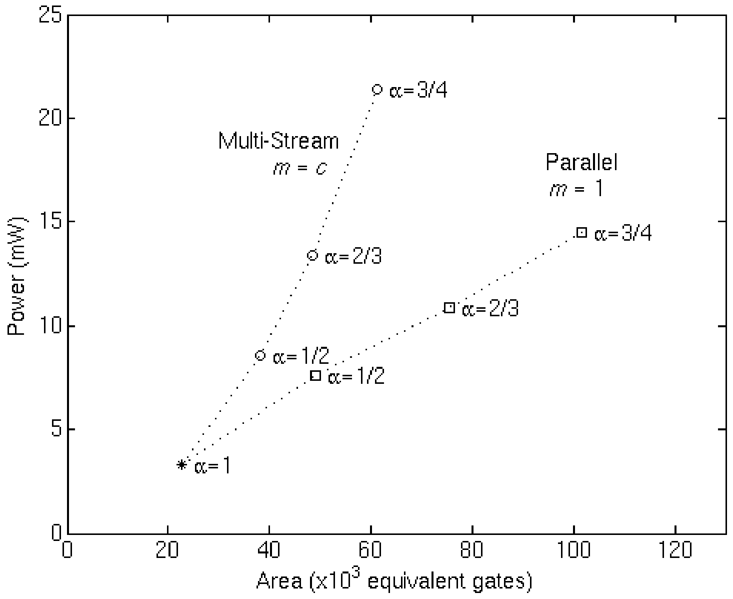


Figure 6.16: Area and simulated power consumption of parallel (squares, $m = c$, $Fclk = 100MHz$) and multi-stream (circles, $m = 1, Fclk = c.100MHz$) SEFDM transmitters.

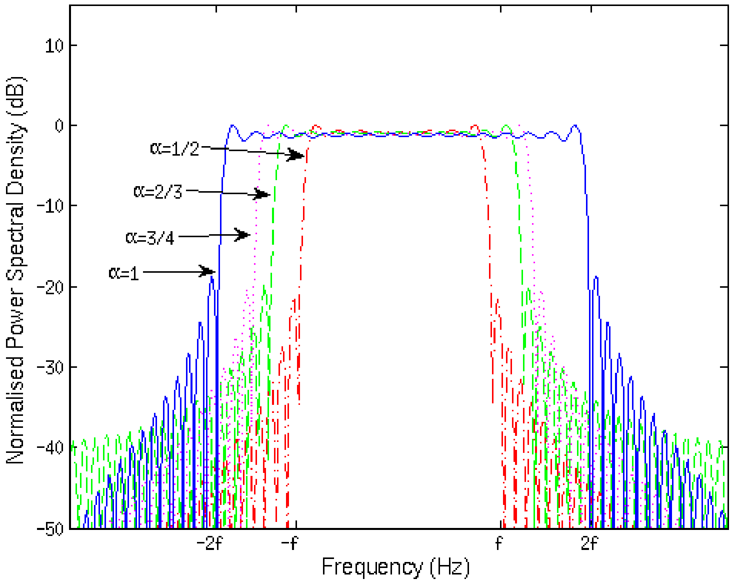


Figure 6.17: Spectra of SEFDM modulated signals for considered bandwidth compression ratios.

the limits of the design space and it is entirely feasible to exploit trade-offs where $1 < m < c$, especially where this can relax otherwise awkward requirements for integer-multiple clock frequencies. At this design point, the raw (uncoded) throughput is 17.4 Mbps with QPSK modulation, up to 52.2 Mbps with 64QAM modulation. Figure 6.17 shows the SEFDM signal spectrum for the considered bandwidth compression ratios, with 64 QPSK modulated subcarriers.

6.5.3 Optimised Architecture

The pruning techniques previously described have also been implemented, leading to reductions in circuit area and power dissipation. The first stage of BFs have been entirely pruned for $\alpha = ½$, while the token flow clock gating and FIFO reduction approaches have been applied for $\alpha = ⅔$ and $\alpha = ¾$. Figure 6.18 shows area and power dissipation for these optimised designs. In the case of the parallel implementation, the clock gating effectively addresses the power consumption increase with α, such that as the number of IFFT computed increases, the number of BFs and FIFO accesses does not increase significantly. The area increase is still proportional to c, although the absolute numbers are reduced due to the optimised storage. For $\alpha = ¾$, the area saving is around 25%, with a 13% power reduction. The multi-stream case shows a more marked improvement in absolute numbers, since the increased clock frequency requirement makes the design more sensitive to optimisation. In this case, the saving in area at $\alpha = ¾$ is 42%, while power dissipation is reduced by 33%.

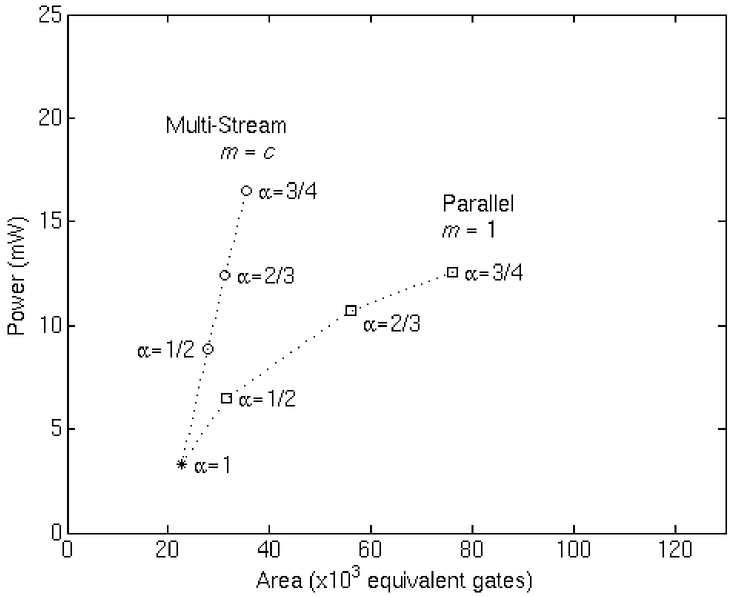


Figure 6.18: Optimised SEFDM modulators with pruned IFFT and FIFOs in parallel (squares, $m = c, Fclk = 100MHz$) and multi-stream (circles, $m = 1, Fclk = c.100MHz$) implementations.

Compared to the baseline OFDM implementation, the optimised architectures were found to give viable results. The multi-stream architecture requires only a 60% increase in silicon area and fourfold increase in power dissipation when comparing $\alpha = ¾$ SEFDM with OFDM. The parallel architecture, while offering higher performance, requires a 140% increase in area with a 180% increase in power dissipation.

6.5.4 Reconfigurable Architecture

It is envisaged that a key feature of future spectrally efficient systems will be the ability to adapt the trade-off between spectral occupancy and BER based on observed channel conditions, much as is currently achieved with adaptive modulation and coding. To this end, SEFDM transmitter implementations with reconfigurable bandwidth compression ratio are easily derived from the presented parallel and multi-stream architectures and can be similarly extended for further

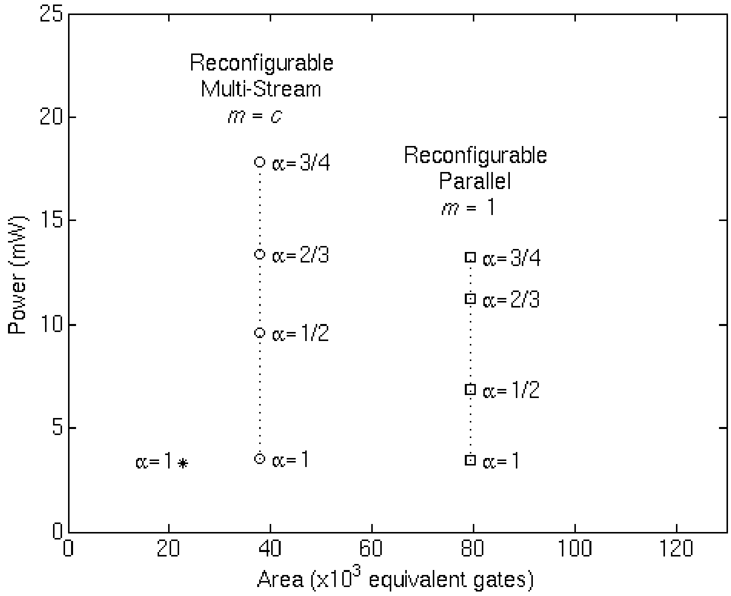


Figure 6.19: Reconfigurable parallel (squares, m = c, Fclk = 100MHz) and multi-stream (circles, m = 1, Fclk = c x 100MHz) SEFDM modulators.

bandwidth compression ratios. In the case of the parallel architecture of Figure 6.8, it is merely necessary to adapt the symbol mapping control logic, the complex gains in the post-processing block and to clock gate un-used IFFT blocks. For the multi-stream version of Figure 6.9, it is also necessary to adapt the clock frequency and FIFO buffer lengths based on the number of transforms required.

Figure 6.19 shows area and power dissipation results for parallel and multi-stream reconfigurable SEFDM transmitters. The reconfigurable designs have around 8% circuit area increase, compared to the design for $\alpha = $ ¾ and no more than 5% increase in power dissipation. Compared to a single-mode OFDM modulator, the reconfigurable SEFDM transmitter has a factor of four increase in circuit area (for the multi-stream architecture) and around 70% increase is power dissipation (for the parallel architecture).

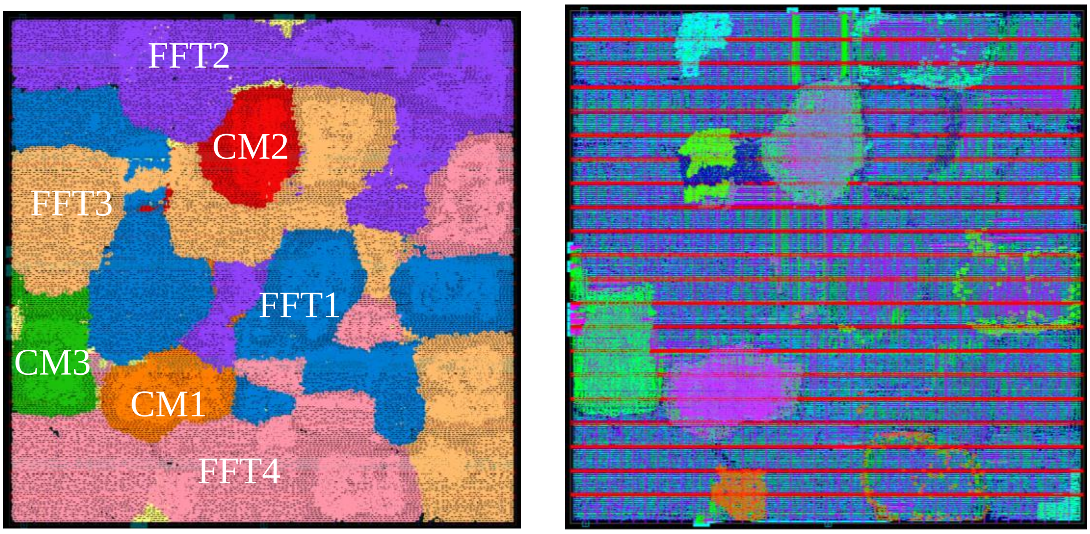


Figure 6.20: Reconfigurable parallel modulator standard cell layout (left), and with full metal stack (right). Layout area is 0.079 mm^2.

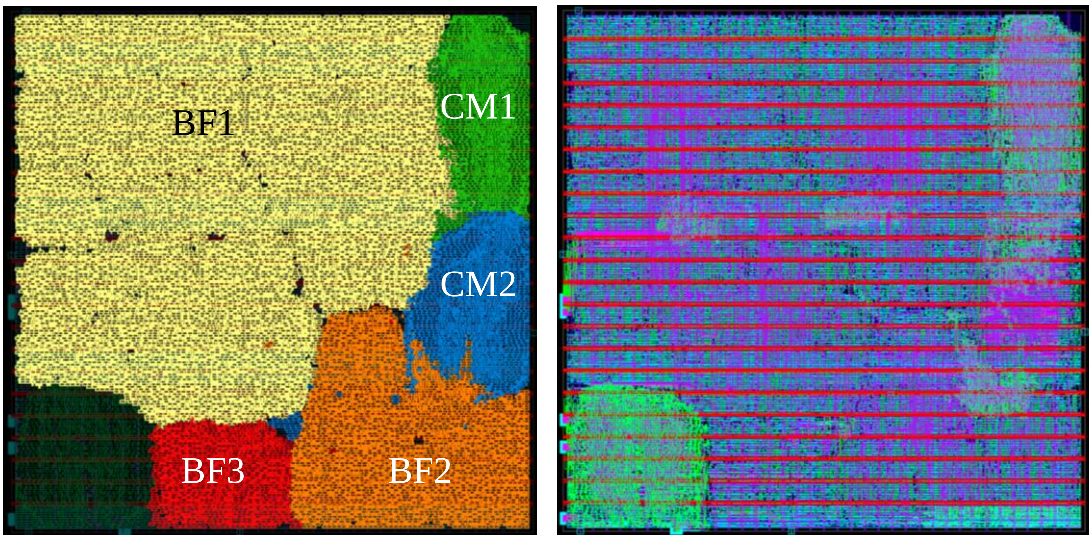


Figure 6.21: Reconfigurable multi-stream modulator standard cell layout (left), and with full metal stack (right). Layout area is 0.048 mm^2.

Due to the clock tree gating in the design, dynamic power dissipation scales well with different values of α, and in fact, for $\alpha = 1$ has a comparable power dissipation to the OFDM baseline, although with a greater leakage power contribution due to the significantly increased circuit area. It is also important to consider that, in context, successfully achieving reduced spectral occupancy may well lead to considerable improvements in power efficiency at the system level if it allows a reduction in transmission power at equal throughput. Layouts for the Reconfigurable parallel and multi-stream SEFDM modulators are given in Figure 6.20 and Figure 6.21, respectively.

6.6 Conclusions

The newly developed SEFDM system is described. After reviewing the practicality of proposed modulation algorithms for signal generation, a recently proposed algorithm is considered, which employs multiple IFFTs, for reasons of low complexity and general suitability to hardware implementation. The algorithm is mapped to two variants of a VLSI architecture, one with parallel IFFTs and one where the concept of the multi-stream FFT is applied to realise the multiple transforms at minimal circuit area overhead. A number of optimisations due to transforms on sparse input vectors are described to further reduce the number of arithmetic operations and FIFO sizes using a novel token flow approach. The designs are detailed in the context of optimised ASIC implementations for $\alpha \in (1, ½, ⅔, ¾)$ and also considering the requirement for a reconfigurable transmitter.

Using a commercial 32nm cell library, circuit area is reported, along with simulated power dissipation figures for the proposed architectures along with a baseline OFDM transmitter for comparison. Analysis of the multi-stream architecture shows a 60% increase in area, along with power dissipation that scales with α up to a factor of four with $\alpha = ¾$, as compared to the baseline OFDM implementation. These results demonstrate that SEFDM transmitters can be realistically implemented with a viable increase in circuit area and power dissipation when compared to conventional OFDM. The work presented here clearly shows the feasibility and limitations of SEFDM signal generation and aims to serve as a first study of implementation in a modern integrated circuit manufacturing technology. It also demonstrated that detailed analysis and good design choices at the algorithm and architecture levels deliver more efficient designs in terms of both power consumption and circuit area.

Chapter 7. Conclusions

This thesis has addressed aspects of power efficiency in DSP ICs as an enabler for continuing trends towards ever increasing spectral efficiency demands. Evolving trends in IC process technology have led to increasing safety margins to account for PVT variation and parametric yield goals. Reducing these design margins is strongly motivated, but is difficult to achieve due to the interdependence of requirements for clock frequency, power consumption and robustness. The Razor DVS approach, first reported in 2004 [6], offers a way to break out of these limitations by using closed-loop adaptive tuning of supply voltage to balance clock frequency and power consumption while separating out robustness as a separate concern. The major aspect of this thesis addresses achieving this robustness to logic errors for DSP applications, utilising the strengths of DSP algorithms which are well suited to tolerating noise.

As a starting point, consideration was given to some of the key trends in parametric variability emerging from process technology research, focussing on the most important aspects from the designer’s point of view. Clear trends of escalating process spread, coupled with concerns over increasing supply voltage noise due to

dI_{dd}/dt limitations are likely to lead to excessive safety margins, detrimental to power efficiency. These issues have not gone unnoticed in the research community and a number of approaches exist for adapting to prevalent conditions, instead of margining for the worst case. The key contributions from the literature were reviewed, including Razor and a number of variants of the ANT approach.

In Chapter 3, a novel FIR filter architecture is presented, incorporating error detection aspects from Razor and use the error information to adapt the filter order to ignore coefficients that are found to have caused timing violations. The FIR filter is an excellent vehicle for experimentation, as it is a fundamental algorithm for so many DSP systems and can be optimised for high performance, allowing for a fair comparison of the proposed scheme against a conventional baseline with a worst case margin. The proposed filter was implemented in a 90nm CMOS process and simulated using SPICE, assuming typical conditions (TT process, 25°C). Power dissipation was found to scale with supply voltage from 28.6 mW at 1 V (nominal) to 13.4 mW at the point of first failure at 730 mV. This is a power saving of 53%, with an undetectable reduction in algorithmic performance. The area and power overhead at nominal supply voltage compared to the transposed direct form is conservatively estimated to be 26% and 24%, respectively. A limitation of this approach is that it is only applicable to algorithms that can be implemented in a sum-of-products structure, as it relies on bypassing in an accumulation structure.

In order to move beyond the sum-of-products kernel, a more generally applicable solution is explored for mitigating timing-errors in arbitrary datapath arithmetic. The use of a two-level timing constraint is proposed, introduced using a novel carry-merge adder with a shaped path-delay distribution, which allows operation in the presence of timing-errors. Timing-errors effectively result in intermittent errors only in LSB bits, which results in noise characteristics similar to quantisation noise. A statistical model is given for this noise source that connects to system SNR. The approach implemented with an FIR filter a 2D DCT in a 32nm CMOS process technology. Simulation results show a reduction in power consumption of 21 – 23%, with a negligible degradation in algorithmic performance in both cases, as compared to a fully margined conventional implementation at nominal supply voltage. The main limitation of this approach is that for small datapath widths (e.g. less than 16-bits), it may be difficult to generate sufficient path length variation between LSB and MSB groups.

The approaches of Chapter 3 and 4, and indeed, many of the published approaches, timing-errors still result in some error, albeit limited and easily modelled. In a commercial VLSI design context, this limits applicability, since many aspects of design verification at both design and manufacturing test stages, require predictable, bit-accurate results. Hence, in Chapter 5, the use of static time borrowing is explored as a timing-error tolerance technique. Analysing the path delay properties of fast addition and multiplication circuits, a significant imbalance is observed, that can be used to introduce time borrowing between stages without increasing the delay of the circuit. Using a Razor pulse latch, a transparent window is introduced only on selective end-points in order to avoid increasing hold time on fast paths. The proposed approach was verified with FIR and FFT pipelines at high and medium performance points. In both cases, selective time borrowing did not increase critical path length, unlike other timing-error tolerance approaches. The drawback is an increase in circuit area due to additional timing constraints on non-speculative FF end-points and also increased implementation effort due to use of a global pulse clock and pulse latches. The hybrid control loop was verified by simulation, demonstrating robustness to intermittent path activation and 60 mV of supply noise. Tighter control of supply voltage scaling is achieved using a novel approach of using timing-error detection to calibrate a canary circuit which circumvents the path activation problem.

Chapter 6 explores the circuit area and power consumption implications of increased DSP workloads due to demand for improved spectral efficiency. Our vehicle for this investigation is the recently SEFDM system. The background and theoretical aspects of the modulation scheme are described, before analysing algorithm and architecture decisions. The concept of the multi-stream FFT is applied, along with a number of optimisations due to transforms on sparse input vectors which reduce the number of arithmetic operations and FIFO sizes. The designs are detailed in the context of optimised ASIC implementations for $\alpha \in (1, ½, ⅔, ¾)$ and also considering the requirement for a reconfigurable transmitter. Using a commercial 32nm cell library, circuit area and simulated power dissipation figures are reported, along with a baseline OFDM transmitter for comparison. Analysis of the multi-stream architecture shows a 60% increase in area, along with power dissipation that scales with α up to a factor of four with α = ¾, as compared to the baseline OFDM implementation. These results demonstrate that SEFDM transmitters can be realistically implemented with a viable increase in circuit area and power dissipation when compared to conventional OFDM. The work presented here clearly shows the feasibility and limitations of SEFDM signal generation and aims to serve as a first study of implementation in a modern integrated circuit manufacturing technology.

The application of timing-error detection techniques to DSP datapaths has been shown to attractively exploit inherent error tolerance of DSP algorithms, resulting in increases in power efficiency and resiliency. Looking at emerging modulation techniques for increased spectral efficiency, such as SEFDM, we have seen that while the workload seems demanding at first, attention at the algorithm and VLSI architecture levels can yield significant savings in circuit area and power consumption. As future DSP workloads increase, it is hoped that these advances may help to close the gap between increasing power consumption and decreasing benefit from process scaling.

7.1 Future Work

Timing-error tolerance for DSP systems remains an open research topic and many important considerations must be addressed if the approach is to become a commercial reality. The following is a suggestion for future work in this area.

- **Analysis of timing-error tolerance techniques in recursive architectures.** This thesis covers non-recursive filters and transforms. These systems have state, but do not have feedback loops. There is no reason why any of the techniques proposed could not be easily extended to non-recursive algorithms. For instance, the analysis of statistical SNR degradation given for the technique in Chapter 4 could be extended to consider, for example recursive filters, following the analysis used for rounding and truncation errors in IIR filters [59]. In the context of the Viterbi algorithm, it was shown that retiming and lookahead techniques [60] can be used to relax the impact of logical errors in recursive loops [41].
- **Analysis and design of timing-error tolerant DSP systems.** Research to date on timing-error tolerant DSP has been limited to investigations of individual algorithms. Of course, such blocks rarely operate in isolation, so it is important to consider system-level implications. Analysis of noise

contributions of each DSP block is required to determine the bounds on noise derived from timing-errors. A number of techniques at the algorithmic level are proposed in [48] to improve SNR of systems with randomised errors, such as over-sampling and filtering. These techniques are directly applicable at the system-level. Another area to explore is opportunities between blocks in the system to tolerate noise of a certain characteristic. An example in the case of image compression was previously outlined to in Chapter 4; it was alluded that a DCT block which generates LSB noise is readily tolerated in a system context, since the DCT is followed by a quantisation stage, which discards the LSBs for many frequency components anyway [67]. Another example in the context of communications systems relates to the fact that there already exist a number of layers mechanisms to cope with varying levels of signal noise, such as channel equalisation, Forward Error Correction (FEC) and Automatic Repeat reQuest (ARQ) techniques [2]. It is conceivable that these system-level techniques could be extended to help with tolerating timing-errors from DSP circuits along with the usual noise sources arising from the communications channel itself. An interesting extension of Chapter 6 would be to apply the voltage scaling techniques of the preceding chapters to the SEFDM baseband transmitter in order to analyse the power savings in this context.

- **Verification and manufacturing test methodologies for timing-error tolerant VLSI.** Verification at design time is an increasingly critical consideration, mainly due to the dramatic increase in design complexity. There is no doubt that the introduction of Razor-like schemes adds a significant burden to the verification challenge and is likely to require significant methodology changes. One of the historical strengths of digital circuits is the ability to perform manufacturing test quickly, cheaply and accurately using scan test patterns and built-in self test (BIST) [12]. In general, testing timing-error tolerance techniques is a very difficult challenge. There is additional circuitry to test and there may be new timing related constraints that are very difficult to reliably test post-silicon. Extensive research is required across the disciplines of design, EDA and test in order to tackle these issues.

- **Hardware prototyping of timing-error tolerant DSP systems.** Very few timing-error tolerant DSP implementations have been reported in silicon to date [38]. This is an important step, as it allows insight into real-world gains in throughput and/or power consumption. It also allows experimental investigation into realistic variations in environmental conditions, which is an important factor to consider when designing adaptive supply voltage control schemes, such as those considered in Chapter 5.

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