New Strategies for Low Noise, Agile PLL Frequency Synthesis

by

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I, Hongyu Wang, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis and acknowlegements.

Hongyu Wang

To my Parents and Rui.

Abstract

Phase-Locked Loop based frequency synthesis is an essential technique employed in wireless communication systems for local oscillator generation. The ultimate goal in any design of frequency synthesisers is to generate precise and stable output frequencies with fast switching and minimal spurious and phase noise. The conflict between high resolution and fast switching leads to two separate integer synthesisers to satisfy critical system requirments.

This thesis concerns a new sigma-delta fractional-*N* synthesiser design which is able to be directly modulated at high data rates while simultanously achieving good noise performance. Measured results from a prototype indicate that fast switching, low noise and spurious free spectra are acheved for most covered frequencies. The phase noise of the unmodulated synthesiser was measured −113 dBc/Hz at 100 kHz offset from the carrier.

The intermodulation effect in synthesisers is capable of producing a family of spurious components of identical form to fractional spurs caused in quantisation process. This effect directly introduces high spurs on some channels of the synthesiser output. Numerical and analytic results describing this effect are presented and amplitude and distribution of the resulting fractional spurs are predicted and validated against simulated and measured results. Finally an experimental arrangement, based on a phase compensation technique, is presented demonstrating significant suppression of intermodulation-borne spurs.

A new technique, pre-distortion noise shaping, is proposed to dramatically reduce the impact of fractional spurs in fractional-*N* synthesisers. The key innovation is the introduction in the bitstream generation process of carefully-chosen set of components at identical offset frequencies and amplitudes and in anti-phase with the principal fractional spurs. These signals are used to modify the Σ-Δ noise shaping, so that fractional spurs are effectively cancelled. This approach can be highly effective in improving spectral purity and reduction of spurious components caused by the Σ-Δ modulator, quantisation noise, intermodulation effects and any other circuit factors. The spur cancellation is achieved in the digital part of the synthesiser without introducing additional circuitry. This technique has been convincingly demonstrated by simulated and experimental results.

Acknowledgements

The work presented in this thesis could not have happened without the help and support of many people. First of all, I would like to express my appreciation of my supervisor, Professor Paul V. Brennan, for bringing this interesting and useful problem to me, for making available his valuable time on a regular basis to discuss the progress of the project and also for his professional guidance and very useful suggestions through out the project. He also provided help in technical writing style and presentation style, and I found it to be extremely valuable. The skills that I learned from him will be of much use to me in my whole life and thus I am in gratitude for his supervision.

I would like to give a special thanks to Dr. Dai Jiang for his guidance and friendship during my time here. He introduced me to a lot of useful theories. His expert suggestions on both electronic circuits and radio frequency system design directed me a short way.

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Table of Contents

List of Figures

List of Principal Symbols

SYMBOL	DEFINITION	UNIT
$\Delta\phi$	Phase Error	rad
$\Delta\phi_{in}$	Input phase jitter	rad
$\Delta\omega_H$	Hold-in limit	rad/s
$\Delta\omega_L$	Lock-in limit	rad/s
$\Delta\omega_P$	Pull-in limit	rad/s
Δt	Timing jitter	s
Δt_n	Timing jitter	s
Φ	Phase	Deg
α	Fractional part of division ratio	-
θ_e	Phase error	rad
θ_i	Input phase	rad
ϕ	Generic phase value	Deg
$\tau_1,\ \tau_2,\ \tau_3$	Generic loop filter time constants	s
ω	Angular frequency	rad/s
ω_c	Cut-off frequency	rad/s
ω_n	Loop natural frequency	rad/s
ω_o	Angular output frequency	rad/s
a	Generic phase term used in trigonometric identity	rad
B	Bandwidth	Hz
B_n	Noise bandwidth	Hz
b	Generic phase term used in trigonometric identity	rad
$C(s)$	Generic Laplace output signal	-
C_1, C_2, C_3	Loop filter capacitor values	F
D	Division ratio	-
$E(z)$	Error signal introduced by quantizers	-
F	Noise factor	-
$F(s)$	Loop filter Laplace transfer function	-
f	Fourier frequency (sideband, offset, baseband)	Hz

f_c	Cut-off frequency	Hz
f_d	PFD Frequency	Hz
f_i	Input frequency	Hz
f_o	Output frequency	Hz
f_s	Sampling frequency	Hz
$G(s)$	Open loop forward gain of PLL	Rad/s
$H(s)$	Feedback gain	Rad/s
K	Collective gain of all PLL frequency independent constants	mA/V
K_{VCO}	VCO gain	Hz/V
k	Boltzmann's constant, $(1{\cdot}38\times10^{-23})$	J/K
$L(f_m)$	Single side band phase noise at offset frequency f_m	dBc/Hz
$L(\omega_m)$	Single sideband signal to carrier ratio at offset frequency ω_m	dBc/Hz
L	Binary word length	-
M	The binary equivalent of the DDS input word	-
m	Multiplier of radio frequency	-
N	Generic n-divider division value	-
n	Multiplier of local oscillator frequency	-
P	Dual modulus prescaler division value	-
Q	Quality factor	-
$Q_i(\omega)$	Quantisation noise power	W
R	Generic R-divider value	-
R_1, R_2, R_3	Loop filter resistor values	Ω
$S\phi_{in}(f_m)$	Input double-sided spectral density of phase fluctuations	rad^2/Hz
$S\phi_{out}(f_m)$	Output double-sided spectral density of phase fluctuations	rad^2/Hz
s	Laplace operator	-
ζ	Damping factor	-
T	Absolute temperature	K
T_L	Lock-in time	s
T_P	Pull-in time	s
T_{ref}	Reference cycle period	s
T_S	Sampling cycle period into phase frequency detector	s
t	Time	s
$v(s)$	Voltage signal, Laplace domain	V
$v(t)$	Voltage signal, time domain	V

List of Abbreviations

SYMBOL	DEFINITION
3G	Third Generation
3GPP	3rd Generation Partnership Project
ADC	Analogue to Digital Converter
ADS	Advanced Design System
AFC	Automatic Frequency Control
AM	Amplitude Modulation
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
CPLD	Complex Programmable Logic Device
DAC	Digital to Analogue Converter
DC	Direct Current
DCI	Digital Controlled Impedance
DCS	Digital Cellular System
DDFS	Direct Digital Frequency Synthesiser
DDS	Direct Digital Synthesis
EDGE	Enhanced Data rates for GSM Evolution
FM	Frequency Modulation
FOM	Figure Of Merit
FPGA	Field-Programmable Gate Array
FSK	Frequency-Shift Keying
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications, (formally known as Groupe Speciale Mobile)
HSCSD	High Speed Circuit Switched Data
IC	Integrated Circuit
LO	Local Oscillator
LSB	Least Significant Bit
MMIC	Monolithic Microwave Integrated Circuit
MSB	Most Significant Bit
OCXO	Oven Controlled Crystal Oscillator

PCB	Printed Circuit Board
PECL	Positive Emitter-Coupled Logic
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PM	Phase Modulated
PSD	Power Spectral Density, (single side-band phase noise)
ROM	Read Only Memory
RF	Radio Frequency
RMS	Root Mean Square
SNR	Signal to Noise Ratio
SSB	Single Side-Band
TCXO	Temperature Controlled Crystal Oscillator
TDMA	Time Division Multiple Access
VCO	Voltage Controlled Oscillator
WCDMA	Wide-band Code Division Multiple Access

Chapter 1

Introduction

1.1 The Issue of Frequency Synthesis

Wireless personal communications have been growing inexorable due to ever emerging new applications and falling prices. The applications of wireless communication devices include cordless phones, cellular phones, global positioning systems, wireless local area networks and radio frequency identification devices, conveying voice, video and other kinds of data. Signal purity of these radio frequency systems determines the effective usability of the radio spectrum. The need for spectrally clean frequency sources has been an almost timeless pursuit for nearly the entire history of humanity. Common to all systems and standards competing for radio space are specifications defining the allowable amount of frequency drift and spurious emissions that each system can impact on its neighbours.

The Phase-Locked Loop (PLL) method of frequency synthesis is now the most commonly used for producing high frequency local oscillators in modern communications equipment. Most modern amateur or commercial transceivers employ at least one if not several, PLL systems, to generate stable high frequency oscillations. PLLs are widely used in a variety of applications, which include line synchronisation and colour sub-carrier recovery in TV receivers, synthesised local oscillators and FM demodulators in radio receivers and frequency synthesisers in transceivers and signal generators, to name but a few [1]. As an essential part of these applications, designers have been exploring new advanced PLL techniques about PLL system with lower noise and better performance.

Modern communication products, from TV sets to mobile phones, universally use a circuit known as a frequency synthesiser to generate a selected range of frequencies to allow the product to tune to different channels and frequencies. In many applications, particularly cellular communications, these synthesisers need to produce fairly pure

signals and simultaneously be able to switch between channels rapidly. Conventional integer-*N* synthesisers [2-4] are very difficult to satisfy the need of fine channel resolution, fast settling and low in-band noise simultaneously. More recently, a technique known as fractional-*N* synthesis, especially PLL based sigma-delta (Σ-Δ) fractional-*N* synthesis [5-9] has been developed to satisfy this requirement of modern wireless communications.

Fractional-*N* synthesisers based on PLL techniques have threatened to challenge the dominance of integer-*N* synthesisers. These synthesisers offer many advantages of significant improvement in finer resolution, lower phase noise, faster lock-in and less spurious spectra. The classical approach to fractional-*N* synthesiser design utilises dithering and phase interpolation. An accumulator carry out signal is used to dither the control input to a dual-modulus divider such that a fractional average divide value is obtained from a divider which supports integer values. In fractional-*N* synthesis, the spurious performance is improved through modulation of the divider control.

In order to suppress fractional spurs in fractional-*N* synthesisers, the Σ-Δ modulator replaces a simple accumulator to control the frequency division due to its high-pass characteristic – noise shaping. Σ-Δ modulators have been applied widely in analogue-to-digital converters (ADC) [10-12] and fractional-*N* frequency synthesisers. The dual advantages of Σ-Δ modulators are their high precision average output value and noise shaping, which can increase the channel resolution and reduce the in-band phase noise of the frequency synthesiser respectively. In order to obtain sufficient randomisation to reduce spurs to negligible levels, Σ-Δ modulators of order two or higher (normally with LSB dithering) are often employed, necessitating a higher order loop filter to counteract the increased noise slope. The shaped quantisation noise can easily dominate at high offset frequencies, introducing a noise-bandwidth tradeoff which translates to low closed loop bandwidth for low phase-noise synthesisers. The quantisation noise introduced by dithering the divide value is whitened and shaped to high frequencies, so that it is substantially filtered by the synthesiser dynamics.

Although fractional-*N* synthesisers can generate the desired signals by Σ-Δ modulation, the noise performance, especially out-of-band noise levels, is not as good as integer-*N* synthesisers because of the wider bandwidth in fractional-*N* architectures. Furthermore, quantisation noise characteristics vary by channel, meaning that on some channels the

Σ-Δ randomisation causes limit cycle repetition. This phenomenon will generate some discrete spurs and degrade the spectral purity. Some other mechanisms, due to the nonlinearity of the feedback system and potential frequency multiplexing, may also lead to unpredictable effects and cause many concerns. Many new techniques and architectures of fractional-*N* synthesisers have emerged in the last decade to change this situation. However, the complexity of the new architectures demands much higher fabrication cost and power consumption.

1.2 Thesis Scope and Contributions

The primary intention of this work is to produce a single-loop synthesiser capable of meeting the specifications of a GSM-1900/DCS-1800/GSM-900 base station application. Table 1.1 summarises some GSM-900 base station requirments. In addition, Figure 1.1 displays the specification masks for the phase noise and spurs at the output of a GSM transceiver. It is very difficult to achieve the purpose by using exist fractional-*N* synthesiser designs because of their high phase noise introduced by wide bandwidth and low reference frequency. This challenge requires that each element of the system is pushed to the edge of its performance envelope, within the confines of current technology. More importantly, several new techniques on refining the quantisation noise are invented to suppress the noise floor of the PLL. If quantisation noise can be reduced significantly, it is possible that it will not have a noticeable impact on overall phase noise performance, and that intrinsic noise sources should become the area of design focus for continued bandwidth extension.

Table 1.1 Specifications for GSM-900 base stations.

Frequency Band	890 – 960 MHz
Channel Spacing	200 kHz
Timeslot Length	577 μs
Switching Time	30.5 μs

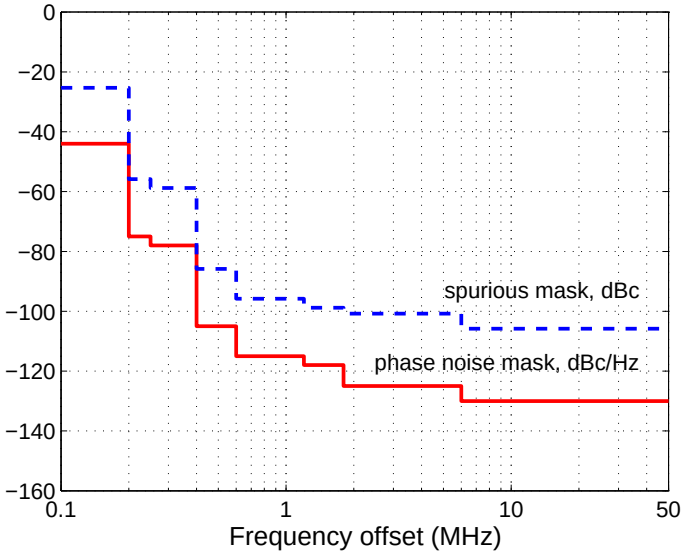


Figure 1.1 GSM specification masks.

This thesis presents a comprehensive description of the work to develop a low noise fractional-*N* synthesiser as an alternative solution of the 'ping-pong' synthesiser used in mobile base stations. The principal contributions of this work are mainly focused on three aspects:

1) An extremely low phase noise fractional-*N* synthesiser is developed, which is capable of satisfying the requirements of phase noise and settling time of base stations in cellular communication systems. This synthesiser is based on an FPGA implemented digital control block using the stored-sequence approach. Benefiting from this advanced architecture, the reference frequency of the synthesiser is increased to 110 MHz and leads to lower phase noise than exist designs. This synthesiser covers all 125 channels of a GSM-900 system and can be extended to DCS-1800 and GSM-1900 bands. Most channels of the synthesiser present clean spectra without significant spurious tones.
2) The intermodulation effect may cause some discrete spurs on some channels of a fractional-*N* synthesiser. An experimental setup has been successfully built first time, which validates the analytic model for a number of synthesiser configurations. The modelled and measured results show good general agreement. A phase compensation technique is then investigated to suppress at least part of these coupling and intermodulation-induced spurs – in particular the most dominant sidebands. The measured results demonstrate that the proposed technique can

effectively suppress close-in sideband spurs and is therefore capable of enhancing spectral purity.

3) An advanced technique, pre-distortion noise shaping, is then proposed to dramatically reduce the impact of discrete spurious components in fractional-*N* synthesisers. This new technique allows optimised noise shaping to be implemented by an FPGA. The key innovation is the introduction in the bitstream generation process of a carefully-chosen set of sinusoidal components at identical offset frequencies and amplitudes and in anti-phase with the principal fractional spurs. These signals are used to modify the Σ-Δ noise shaping, so that fractional spurs are effectively cancelled. This approach can be highly effective in improving spectral purity and reduction of spurious components caused by the Σ-Δ modulator, quantisation noise, intermodulation effects and any other circuit factors.

1.3 Thesis Outline

The primary intention of this work is to investigate intermodulation effects on the performance of the fractional-*N* synthesiser, especially the in-band noise level. A low noise fractional-*N* synthesiser model is necessary and the implementation process is presented and explained in this thesis. Chapter 2 introduces fundamental theories of PLLs and fractional-*N* frequency synthesis. Major loop components are analysed in detail. The closed loop performance is discussed in both time and frequency domains. A comparison of integer and fractional synthesis theories leads to a discussion of the merits for exploring agile fractional-*N* frequency synthesisers.

Chapter 3 covers the theory and architecture of Σ-Δ modulators, which are used to control the divider of the fractional-*N* frequency synthesiser. Third order single-stage and third and fourth order MASH modulators are analysed, which contain their stable input and output range, signal and noise transfer functions, noise shaping and stability analysis. Both simulated and measured results are presented and found to match fairly well at high sampling frequencies. The results are compared analysed for the purpose of being used in fractional-*N* frequency synthesisers to shape the noise characteristic.

Chapter 4 presents the design procedure and measured results of fractional-*N* synthesiser prototypes. Several Σ-Δ modulators are successfully implemented by an FPGA, which can work at high frequencies by employing a stored-sequence technique. The two implemented prototypes, working at different reference frequencies, demonstrate the fundamental theory of fractional-*N* frequency synthesis. An extra low in-band noise fractional-*N* synthesiser is successfully developed, to provide a valid solution in cellular base stations replacing exist high cost integer-*N* applications.

Chapter 5 introduces the intermodulation effect in PLL fractional-*N* synthesisers. An analytic and numerical model shows prediction of possible intermodulation-borne spurious components. This prediction is then validated by measured results. To eliminate this effect in the synthesiser system, a phase compensation technique is proposed, which can partially remove the spurious tones. A series of measured results demonstrate that it can effectively suppress the dominant spurs.

In chapter 6, a novel technique is presented for enhancing the spectral purity of fractional-*N* synthesisers. The proposed pre-distortion technique is able to optimise the noise shaping of a Σ-Δ modulator, and it can eliminate the disadvantage of insufficient randomisation in single-stage Σ-Δ modulators with 1-bit quantizers. Modelled and measured results are compared and analysed and show that it is feasible in practice to generate improved spectra as an efficient solution.

Finally, chapter 7 concludes with a summary of the work, followed by a series of discussion of further work.

1.4 Author's Publications

1. H. Wang and P. V. Brennan, "Pre-Distortion Sigma-Delta Noise Shaping in Fractional-N Frequency Synthesizers," submitted to *IEEE trans. Microwave Theory and Techniques*, Nov. 2008.

2. P. V. Brennan, H. Wang, D. Jiang and P. M. Radmore, "A New Mechanism Producing Discrete Spurious Components in Fractional-N Frequency

Synthesizers," *IEEE trans. Circuits and Systems*, vol. 55, Issue 5, pp. 1279-1288, June 2008.

3. P. V. Brennan, D. Jiang and H. Wang, "Memory-controlled frequency divider in fractional-N synthesisers," *IET Electronics Letters*, vol. 42, pp. 1202-1203, 12 Oct. 2006.

4. H. Wang and P. V. Brennan, "A new spurious component suppressing technique in fractional-N frequency Synthesizers," *IEEE Proc. Frequency Control,* IFCS'08, pp. 753-757, May 2008.

5. H. Wang, P. V. Brennan and D. Jiang, "A Low Noise Fractional-N Frequency Synthesiser Using A Very Fast Noise Shaper," *IEEE Proc. Electronics, Circuits and Systems*, ICECS'07, pp. 1388-1391, Dec. 2007.

6. H. Wang, P. V. Brennan and D. Jiang, "FPGA Implementation of Sigma-Delta Modulators in Fractional-N Frequency Synthesis," *IEEE Proc. Signals, Circuits and Systems*, ISSCS'07, vol. 1, pp. 1-4, July 2007.

7. H. Wang, P. V. Brennan and D. Jiang, "A Generic Multi-Modulus Divider Architecture for Fractional-N Frequency Synthesisers," *IEEE Proc. Frequency Control,* TIMENAV'07, pp. 261-265, May 2007.

8. H. Wang, P. V. Brennan and D. Jiang, "A comparison of Sigma-Delta Modulator techniques in fractional-N frequency synthesis," *IEEE Proc. Circuits and Systems*, MWSCAS'06, vol. 1, pp. 659-663, Aug. 2006.

9. D. Jiang, P. V. Brennan and H. Wang, "Strategies for reducing noise-coupling effects in fractional-N frequency synthesisers," *IEEE Proc. Frequency Control,* IFCS'06, pp. 65-69, June 2006.

Chapter 2

Phase-Locked Loop Fundamentals

2.1 Introduction to Phase-Locked Loops

The basic phase-locked loop concept has been known and widely utilised since first being published by Bellescize [13] in 1932 and treated as the synchronous reception of radio signals. The first widespread use of phase lock theory was in television receivers. The start of each line and the start of each interlaced half-frame of a television picture are signalled by a pulse transmitted with the video information [1]. The popularity of PLLs also originates from its use as a signal detector, i.e. the detection of a low-level signal carrying information in its phase or frequency, embedded in noise [14]. Furthermore, PLL circuits are used for frequency control. They can be configured as frequency multipliers, demodulators, tracking generators or clock recovery circuits. Each of these applications demands different characteristics but they all use the same basic circuit concept.

PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth. Techniques and systems frequently involved in these applications are quite complex, requiring a high degree of sophistication. Many of the PLL applications have been used at radio frequencies, complex phase shifters, signal splitters, modulation, and demodulation schemes such as bi-phase and quadra-phase. Because of low noise requirements in some dedicated microwave applications, most components of these PLL systems are made from discrete as opposed to integrated circuits. The capacitance of the loop filter occupies significant die area in integrated circuits. However, in other communications system applications such as Frequency-Shift Keying (FSK) and FM and AM demodulation where frequencies are below approximately 100 MHz, monolithic PLLs have found wide application because of their low cost versus high performance [15, 16].

One obvious application of phase lock is in automatic frequency control (AFC). Good frequency control performance can be achieved with this method, whereas conventional, non-coherent AFC techniques necessarily entail some frequency error [1]. To maintain the control voltage needed for locking it is generally necessary to have a nonzero output from the phase detector. Consequently, the loop operates with some phase error present [17, 18]. This error tends to be small in a well-designed PLL. Frequency synthesis is another area where the phase-locked technique is widely employed as a basis and accurate method to generate high stable frequencies. A typical frequency synthesiser comprises all analogue elements, exactly as a basic PLL, except for the divider. A dual or multi modulus divider often replaces a constant phase/frequency divider in the PLL in conjunction with digital control part of the synthesiser.

A PLL is a feedback control loop consisting of four fundamental components, as shown in Figure 2.1. As labelled, they are a phase detector, a loop filter, a VCO and a frequency divider. The PLL achieves its functionality by firstly dividing the output frequency of the VCO and then comparing its phase with the phase of the input signal. The phase comparison operation is performed through the use of a phase detector which also acts as a frequency discriminator when the PLL is out of lock. Practical implementations of the phase detector are non-ideal, and lead to the introduction of high frequency components in the error signal. To solve this drawback, these components must be attenuated before feeding the error signal into the VCO input. This task is accomplished by the loop filter which uses the error signal to steer the VCO input voltage which changes the frequency in the direction and even reduces the phase difference. The feedback action of the PLL accurately sets the VCO output frequency. The phase detector output voltage is dependent on the difference in phase of the two applied inputs and is used to adjust the VCO until this phase difference is zero. The loop is then in a steady state (i. e. dynamic equilibrium) so that the VCO frequency and phase are locked to the input signal frequency and phase respectively:

$$f_o = Nf_i \tag{2.1}$$

In the locked state, the phase error between the output signal and input signal is zero or very small. If a phase error builds up, a control mechanism redirects the output signal as to minimise the phase difference with the input signal. Thus the circuit behaves as a

phase multiplier and also a frequency multiplier because frequency is the time derivative of phase.

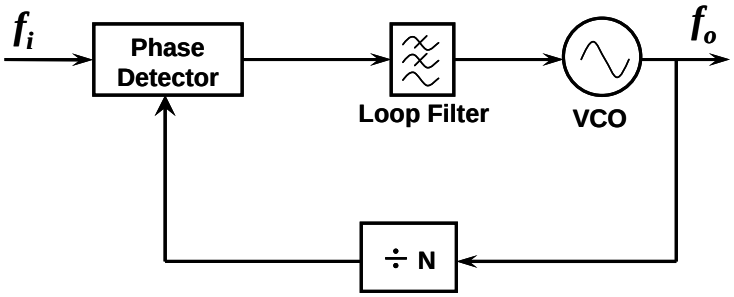


Figure 2.1 A block diagram of the basic arrangement of a Phase-Locked Loop.

The active characteristics of PLLs are governed by the design of loop filters. The loop bandwidth may be made very narrow so that the loop can extract signals from the white noise and still track their frequency variations over a wide range [19, 20]. On the other hand, a wide bandwidth is needed in applications requiring high operating speed, such as agile frequency synthesisers and there are also certain practical constraints on the loop characteristics.

2.2 Phase-Locked Loop Elements

2.2.1 Phase/Frequency Detector

As the engine of the PLL, the phase detector transfers the phase information (including noise) from reference source and divider to the VCO output. The phase detector is a form of comparator providing a DC output signal proportional to the difference in phase between two input signals. This may be written as [1]:

$$V_P = K_P(\phi_1 - \phi_2) \tag{2.2}$$

where V_P is the phase detector output voltage, ϕ_1 and ϕ_2 are phases of the input signals and K_P is the phase detector gain in units of Volts per radian. There are two basic types of phase detector, multiplier and sequential. The Phase/Frequency Detector (PFD), as shown in Figure 2.2 [21], is a sequential phase detector widely used in various integer-*N*

and fractional-*N* frequency synthesisers. The PFD compares the phase or frequency difference from a reference signal and a VCO feedback signal which has already been divided by a frequency divider. The arrival of the rising edge of the reference signal triggers the upper flip-flop to switch *UP* to logic-1, then the arrival of the rising edge of the VCO/*N* signal triggers the lower flip-flop to switch *UP* to logic-0. The PFD outputs are differential square waveforms whose duty cycle varies according to the input phase or frequency difference. The difference of the output pulse streams provides a control voltage proportional to input phase or frequency difference. Its output voltage versus phase difference is shown in Figure 2.3.

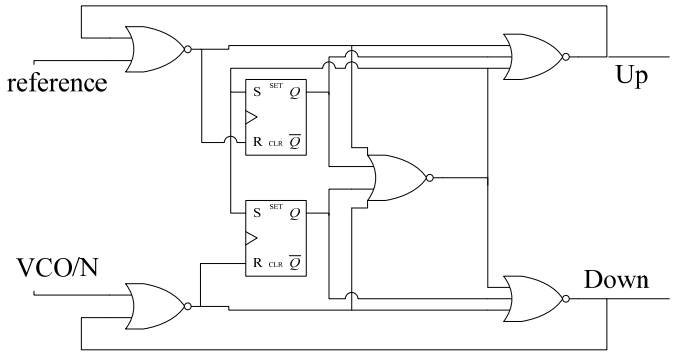


Figure 2.2 Functional diagram of a phase/frequency detector.

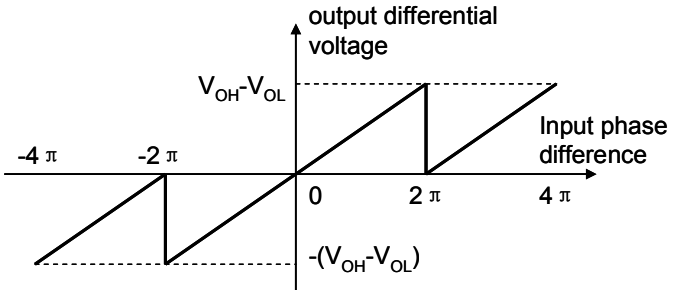
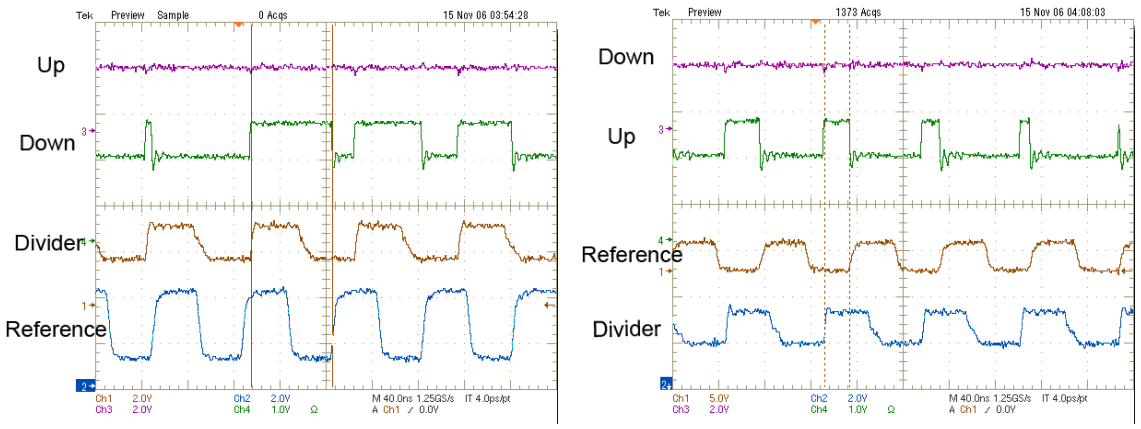


Figure 2.3 The PFD output voltage versus phase difference.

When two inputs of the PFD are at the same phase and frequency, its outputs produce a stream of minimum duration pulses that occur at the rising edges of the input waveforms. This is the lock condition of the system. If either input starts to lead the other in phase, the width of pulses on the corresponding output increases in proportion to the phase difference. In a PLL implementation, these outputs direct the system VCO to increase or decrease its frequency to maintain the lock condition. The minimum

output pulse duration is an important parameter for the design of the signal processing functions, which follow the phase detector.

When the phase error of the input signals is fairly small, there are problems with the PFD responding to it correctly. The phase detector is often modelled under ideal conditions, but the components used to implement the PFD suffer nonlinear and delay problems. If the delay is significant enough, the differential output of the PFD is unable to generate the narrow pulses needed to revise the output frequency of the VCO. This area of operation where the phase error is of the order of the component delays in the phase detector is often referred to as the dead zone [22]. Many PLLs have dead zone elimination circuitry to ensure that the PFD always comes on for some amount of time to avoid operating in this manner. When controlling a charge-pump integrator, a detector may produce a dead-zone characteristic at the lock condition if the minimum pulse width is too short. However, it can be eliminated by providing a well-defined minimum output pulse width [23, 24]. The minimum short pulse duration can completely eliminate the minimum phase difference requirements during the lock condition in theory and maximise loop jitter performance.



(a) (b)

Figure 2.4 Measured waveforms of the Phase/Frequency Detector. (a) Divider output lags reference signal. (b) Reference signal lags divider output.

To demonstrate the behaviour of a typical PFD, Figure 2.4 presents the measured input and output relationship. The PFD under test is a MAX9383 which can work up to 400 MHz without cycle slips. The input frequency is 12.8 MHz and the PFD generates pulses with different widths. If the divider output signal lags the reference signal, the

output *DOWN* channel generates phase difference pulses and the *UP* channel is a DC signal as shown in Figure 2.4(a). The output channels change characteristic in the other case as shown in Figure 2.4(b).

2.2.2 Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) is an analogue component of the PLL which converts a voltage to a frequency. VCOs are made to change frequency by changing the value of one of the frequency determining circuits. In the VCOs the frequency-determining component is made to change electrically, and the output frequency is dependent on the value of an applied tuning voltage. They are realised in many forms from RC multivibrators at low frequencies to resonators and Yttrium Iron Garnet (YIG) tuned oscillators at higher frequencies; crystal oscillators (VCXOs) are used as high stability oscillators. Some of specifications of VCOs as follows:

1) Phase and temperature stability (Spectral purity).
2) Linearity of frequency versus control voltage.
3) Gain factor.
4) Modulation bandwidth.
5) Cost and required PCB area.

As far as the loop filter design is concerned, the most important property of VCOs is their tuning characteristic. The slope of this characteristic, the VCO gain K_V, is a further factor to be included in the loop equations, in addition to the phase detector gain, and divider ratio, 1/*N*. The VCO gain is defined as [1]:

$$K_v = \frac{d\omega_o}{dV_t} rad/s/V \tag{2.3}$$

where ω_o is the output frequency and V_t is the tuning voltage. In many cases the LC-tank VCO frequency initially increases sharply and then increases with a flatter slope with the increasing tuning voltage. The VCO gain therefore often decreases as the operating frequency is increased. This is because the non-linearity of the active element. A typical LC-tank low-noise VCO CLV1025E [25] manufactured by Z-Communications is measured with tuning characteristic shown in Figure 2.5.

Figure 2.6 shows the circuit of a typical LC-tank VCO. The variable capacitors lead to LC oscillation covering a frequency range. Each individual transistor in the pair is essentially a common-source amplifier with a complex, tuned load comprised of a lossy inductor in parallel with a variable capacitor. An LC-tank VCO basically is a feedback network consisting of a resonator and a non-linear active amplifier [26]. If the VCO has a resonator filter of at least an order of two, a sinusoidal output results, since the light harmonic content due to the weakly non-linear amplification is filtered by the resonator [27].

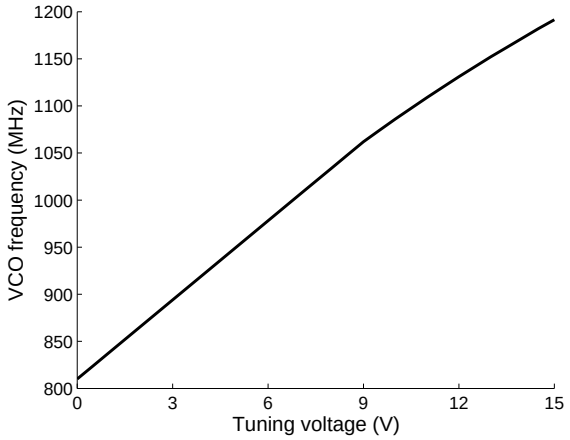


Figure 2.5 Measured tuning characteristic of a low-noise VCO Z-COMM CLV1025E.

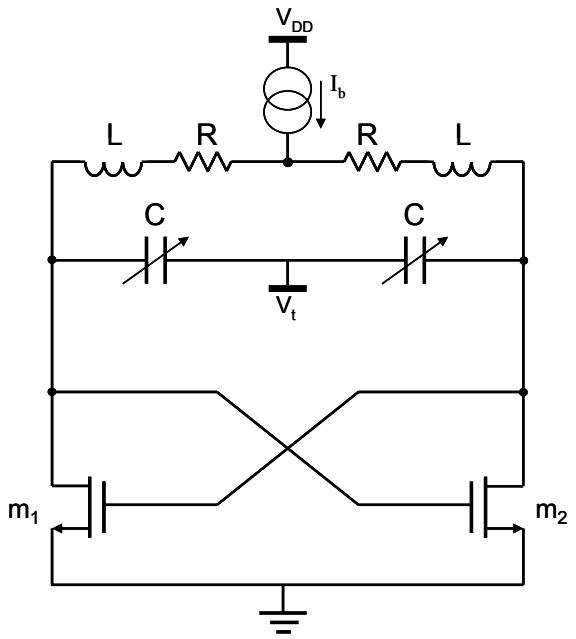
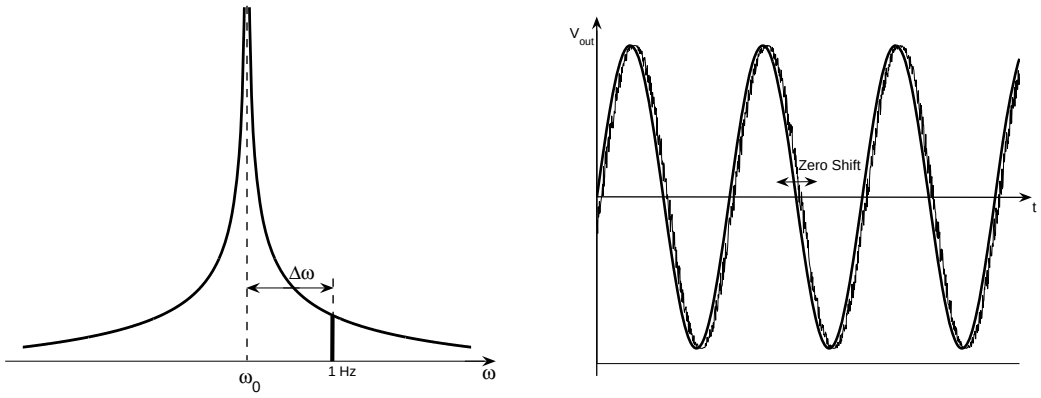


Figure 2.6 Circuit diagram of an LC-tank VCO.

The VCO performance is directly related to its noise level, with a quantity known as phase noise which is a frequency domain view of the noise spectrum of the oscillator signal. In time domain, the phase noise is related to jitters which represent time accuracy of the oscillator period. Phase noise is typically expressed in units of dBc/Hz at various offsets from the carrier frequency. The output of an ideal oscillator is a perfect sinusoidal wave and it corresponds to a Dirac impulse in the frequency domain. In a real oscillator, noise generates fluctuation on the phase and the amplitude of the signal. The output spectrum is no longer a Dirac impulse, but exhibits sidebands close to the oscillator frequency, as shown in Figure 2.7. To quantify phase noise, the noise power in a unit bandwidth at a certain offset frequency $\Delta\omega$ from ω_0 is considered and derived by the carrier power. The results is a single sided spectral noise density [16]:

$$L(\Delta\omega) = 10\log\left(\frac{P_n}{P_c}\right) \quad \text{(dBc/Hz)} \tag{2.4}$$

where P_n is the noise power in a 1 Hz band at $\omega_0 + \Delta\omega$ offset frequency; P_c is the carrier power.



(a) (b)

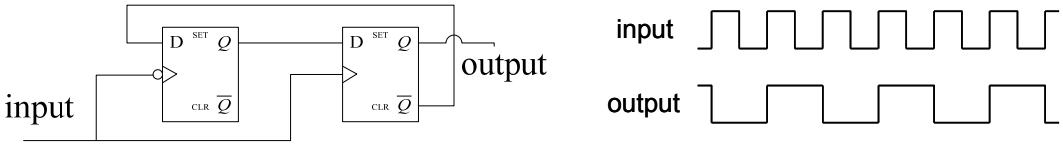
Figure 2.7 The frequency (a) and time (b) representation of phase noise in an oscillator.

2.2.3 Frequency Divider

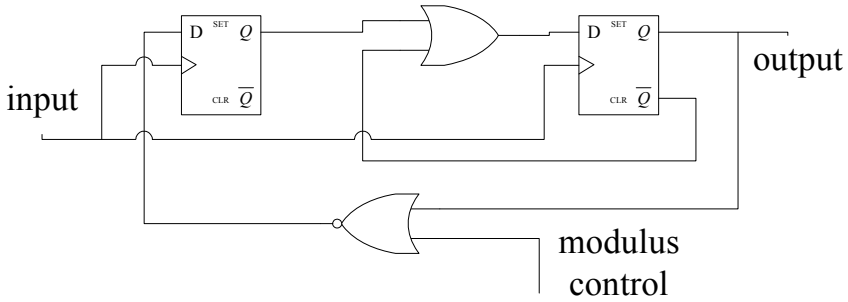
One of the most common uses of PLLs is in frequency synthesisers, where a range of output frequencies are generated from a single stable frequency reference. This requires the use of a variable ratio divider in the feedback path. There are other applications where fixed dividers are sufficient, such as in phase modulators or demodulators where a deviation beyond the range of the phase detector is needed, or in microwave frequency multiplier loops. It should be noted that frequency dividers act equally as phase dividers, therefore a factor of $1/N$ must be allowed for in the loop equations.

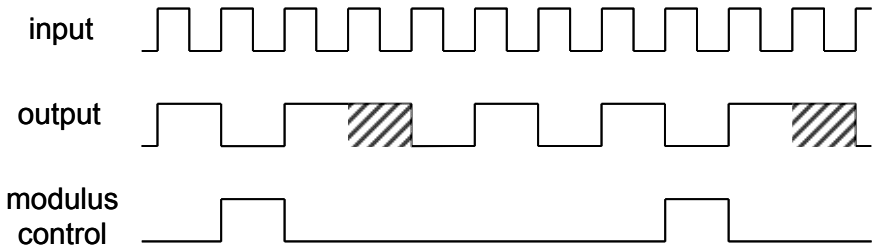
Together with the oscillator, the frequency divider is the only part of the PLL that operates at high frequencies. It converts the high oscillator output frequency to a lower frequency. In integer-*N* frequency synthesisers, the frequency divider is a counter, whose output state changes after it has counted a pre-defined number of input periods. As fractional-*N* frequency synthesisers draw a lot of attention, dual and multi-modulus frequency dividers controlled by Σ-Δ modulators play a key role to overcome the bottleneck of channel resolution and settling time. This technique permits narrow output frequency step sizes compared to the reference frequency and fast settling time while improving the phase noise performance of the PLL frequency synthesiser. The output frequency of the divider in fractional-*N* synthesisers is much higher than integer architectures, which means the division ratio is lower. Furthermore, the dual or multi modulus divider needs to keep switching division ratio all the time, dithering between integers with a constant average value.

Figure 2.8 shows a fixed divide-by-2 Johnson counter and a divide-by-2/3 circuit implemented by logic gates and D-type flip-flops. Both of them are fairly simple and are widely used in synthesisers.



(a)





(b)

Figure 2.8 Functional diagrams of (a) A divide-by-2 Johnson counters. (b) A divide-by-2/3 circuit implemented by logic gates and D-type flip-flops.

2.3 Integer-N Synthesisers

Figure 2.9 displays a classical indirect frequency synthesiser based on a PLL architecture consisting of a VCO, a phase detector, a loop filter, a divider and a reference source. Accurate control of the phase, and thus frequency, of the VCO is achieved by using an error signal to adjust the VCO control voltage. The phase/frequency detector produces a pair of voltage signals corresponding to the phase difference of the divided VCO output and a reference source, which are then smoothed by the loop filter and fed into the VCO input.

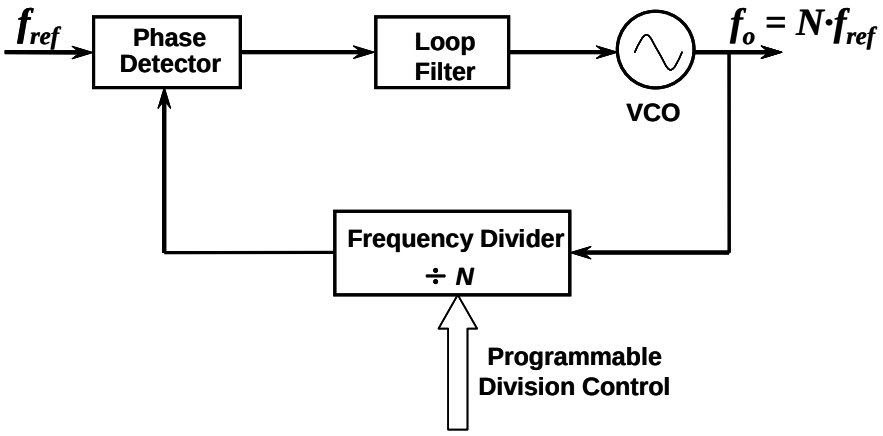


Figure 2.9 A general arrangement of an integer-*N* synthesiser.

Physical implementation of the divider within the synthesiser is easily accomplished using digital circuit techniques so long as the division ratio *N* is contrained to be an integer, hence this kind of synthesiser is named integer-*N* synthesiser, to be different from later emerged fractional-*N* technique. The divider is set to a stable division ratio on a specific channel, in order to generate an expected frequency. A programmable multi-bit control signal is in charge of switching output frequencies channel by channel.

The frequency/channel resolution of the synthesiser is restricted to the value of the reference frequency, so that high resolution requires the choice of low reference frequency. In order to prevent large spurious noise levels, a low reference frequency must be accompanied by a small PLL bandwidth, which leads to slow dynamics. This is because that the loop filter provides limit suppression on reference spurs at low

frequency offsets. In GSM base station applications, two separate integer-*N* synthesisers are merged to act as a carrier generator. The reference frequency is equal to GSM channel resolution, 200 kHz, and the bandwidth of these synthesisers are set to 20 kHz, so that the closest reference spurs at 200 kHz offset can be suppressed without affecting the signal to noise ratio of other channels. However, the low pass response of a second order loop is −20 dB and a third order loop is −40 dB, which means the first reference spur at 200 kHz offset may still have significant level and easily exceed the system requirment. To break the tradeoff between loop bandwidth and channel resolution which is equal to the reference frequency in integer-*N* synthesisers, the fractional-*N* synthesis technique was introduced.

2.4 Loop Filter

Operation of the PLL of Figure 2.1 may be represented by a signal flow graph shown in Figure 2.10. Here the filter transfer function is illustrated, using Laplace notation, by $G(s)$ and a $1/s$ term is included to translate the VCO output frequency, ω_o, into phase, ϕ_o. The closed-loop transfer function is given as:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{\dfrac{K_P K_V G(s)}{s}}{1 + \dfrac{K_P K_V G(s)}{Ns}} \tag{2.5}$$

The order of the loop is defined by the highest power of (s) in the denominator of the closed-loop transfer function shown above and the type of loop is defined by the number of perfect integrators within the loop [28, 29]. If $G(s)$ has $n - 1$ poles in the form of $\frac{1}{s^{n-1}}$, $\frac{\phi_o(s)}{\phi_i(s)}$ will have poles in form of $\frac{1}{s^n}$, which is the n^{th} order of PLL. All loops are at least type I because of the integrating action of the VCO [1]. Because each integrator contributes one pole to the transfer function, so that the order can never be less than the type. But additional non-integrated filtering is often present, contributing additional poles and increasing the order, with no effect on the type [30].

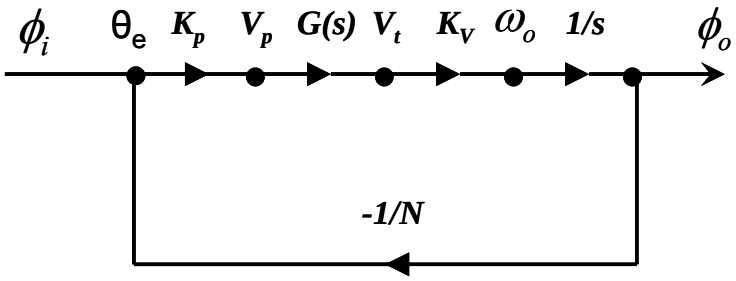


Figure 2.10 Signal flow graph representation of a PLL.

Various inputs can be applied to a system. Typically, these include step position, velocity, and acceleration. Supposing $\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem allows determination of the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.

If the system is stable, the steady-state error for a step input $\theta_i(t)$ can be obtained from the final value theorem [4]:

$$\lim_{t\to 0}[\theta_i(t)] = \lim_{s\to 0}[s\theta_e(s)] \tag{2.6}$$

where

$$\theta_e(s) = \frac{1}{1+\dfrac{K_P K_V G(s)}{Ns}}\theta_i(s) \tag{2.7}$$

If there is a constant-amplitude change in the input frequency of A rad/s,

$$\theta_i(s) = \frac{A}{s^2} \tag{2.8}$$

then

$$\lim_{t\to 0}[\theta_i(t)] = \lim_{s\to 0}\frac{AN}{K_P K_V G(s)} = \frac{AN}{K_P K_V G(s)} \tag{2.9}$$

If $G(s) = 1$, the steady-state phase error will be inversely proportional to the loop gain $K_P K_V/N$, recalling that the closed-loop bandwidth and loop response increases with loop gain. To increase the response speed and reduce the tracking error, the loop gain should be as large as possible. If $G(0)$ is finite, there will be a finite steady-state phase error. The frequency error,

$$f_i(t) = \frac{d}{dt}\theta_i(t) \tag{2.10}$$

will be zero in the steady state. That is, the input and VCO frequencies will be equal ($f_i = f_o$).

The two loop filter topologies used in PLLs are passive and active loop filters. The choice of the two topologies depends upon the type of the phase detector employed in the system. The active filter is directly driven by the output voltage signals of the PFD, and charge pump is unnecessary in this kind of filters. Its function is to control the VCO by changing the high frequency PFD output signals into a low frequency and relatively stable control voltage. Active loop filters convert the PFD differential voltage output signals to the VCO control voltage. The conversion process is completed by using an active component such as op-amp. As a result of the phase difference information, the voltage output pulses of the PFD are smoothed, and are converted to a relatively stable modulation signal to control the VCO. High order Σ-Δ modulators are commonly used in fractional-*N* frequency synthesisers to push the quantisation noise to high frequencies, and higher order loop filters are mandatory to suppress close-in quantisation noise. Normally higher order active filters provide a better overall compromise in loop performance, and they are more suitable in high order loops. However, stability issues limit their practical usage in some real synthesiser designs.

The passive RC filter normally cooperates with the charge pump phase detection system. The input signal to this filter is a pulse width modulated current sequence, referred to as a current driven loop filter. The passive loop filter converts current pulses from the PFD into the steady state voltage by employing a simple combination of only resistors

and capacitors. Passive loop filters are widely used in integrated PLLs and frequency synthesisers benefiting from its simple topology, small area occupation and low power dissipation. In addition, they have better performance in high speed loops where active elements with non-linear behaviour or parasitic delays, such as track lengths, may introduce unwanted phase shifts around the loop, resulting in instability [1].

2.4.1 First Order type I Loops

The PLL without a loop filter, $G(s) = 1$, is called a first order type I loop because it has only one integrator – the VCO, and the highest power (s) in the denominator of the system transfer function is 1. The PLL transfer function is:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{N}{\frac{N}{K_P K_V}s + 1} = N\frac{\frac{K_P K_V}{N}}{s + \frac{K_P K_V}{N}} = N\frac{\omega_o}{s + \omega_o} \tag{2.11}$$

where $\omega_o = \frac{K_P K_V}{N}$ and $f_o = \frac{K_P K_V}{2\pi N}$,

This is clearly a first order type I loop and the loop transfer function is simply a first order low pass response with a time constant of $N/(K_P K_V)$. This loop is of very limited practical use due to no filtering of the phase detector output. An improvement can be obtained by using a passive low-pass filter, so that the system becomes a second order type I loop. However, this system also has practical limitations such as there being a finite phase offset necessary to support a steady-state VCO tuning voltage and possible acquisition and tracking problems. More useful loop filters fulfill a combination of low-pass and integrator properties, the latter function requiring the use of an active device such as an op-amp [1].

2.4.2 Second Order Type II Loops

One of the most useful and popular designs of loop filters, producing a second order type II response, is shown in Figure 2.11. It functions as an integrator at low frequencies with a DC gain equal to that of the op-amp. Since this gain is fairly high, it

may be regarded as a perfect integrator at DC, for which the filter transfer function is given as:

$$G(s) = \frac{-\left(R_2 + \frac{1}{sC}\right)}{R_1} = -\frac{1}{s}\frac{\tau_2 s + 1}{\tau_1} \tag{2.12}$$

where $\tau_1 = R_1 C$, $\tau_2 = R_2 C$.

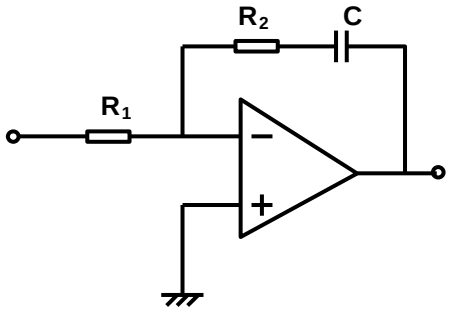


Figure 2.11 Single input second order type II loop filter.

The multiplier 1/*s* indicates a second integrator (in addition to the VCO), which is generated by the active amplifier. Since the type of the loop has been added an active element in the filter, the tracking behaviour of the loop is also altered. The steady-state error after a phase change is still zero. This means that the loop can track phase and frequency steps with zero error. The magnitude of the transfer function is:

$$|G(j\omega)| = \frac{1}{R_1 C\omega}\sqrt{1 + (\omega R_2 C)^2} \tag{2.13}$$

And the phase is

$$\theta = \arctan(\omega\tau_2) - 90° \tag{2.14}$$

Substituting this into equation (2.5) is the closed-loop transfer function shown as:

$$\frac{\phi_o(s)}{\phi_i(s)} = \left[\frac{K_P K_V R_2}{R_1}\right] \frac{s + \frac{1}{sC}}{s^2 + \frac{K_P K_V R_2}{NR_1} s + \frac{K_P K_V}{NR_1 C}} \tag{2.15}$$

which may be written in a form compatible with standard control terminology,

$$\frac{\phi_o(s)}{N\phi_i(s)} = \frac{2\zeta\omega_n s + \omega_n{}^2}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \tag{2.16}$$

where the loop natural frequency, ω_n, and damping factor, ζ, are given by

$$\omega_n = \sqrt{\frac{K_P K_V}{NR_1 C}} \text{ and } \zeta = \frac{R_2}{2}\sqrt{\frac{K_P K_V C}{NR_1}} = \frac{\omega_n R_2 C}{2} \tag{2.17}$$

The 3-dB bandwidth of the type II second-order loop is [4]

$$B_{3dB} = \frac{\omega_n}{2\pi}\sqrt{2\zeta^2 + 1 + \sqrt{\left(2\zeta^2 + 1\right)^2 + 1}} \tag{2.18}$$

And the noise bandwidth is [4]

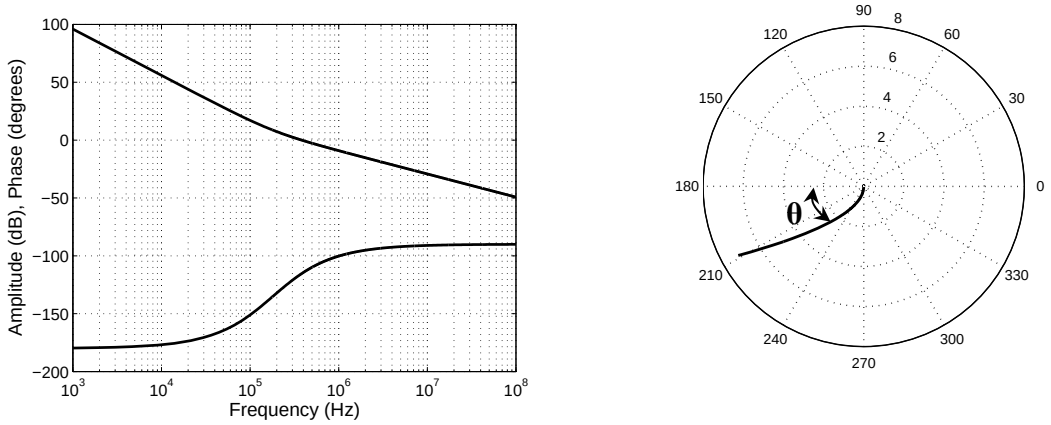
$$B_n = \frac{\frac{K_P K_V R_2}{NR_1} + \frac{1}{\tau_2}}{4} \tag{2.19}$$

Noise bandwidth is the abbreviation for equivalent rectangular noise bandwidth, which represents the ability of a PLL to reject input noise.

These are the design equations for this particular loop filter, the loop properties depending entirely on the choice of the two parameters: natural frequency ω_n and damping factor ζ. Natural frequency and damping factor are well suited for second-order loops. In general, ω_n determines the cut-off frequency of the response and ζ determines the shape of the characteristic. $\zeta = 1$ is the case for the critical damping. A value for ζ of between 0.5 and 1 is normally used with 0.707 being a popular design choice because it gives rise to a Butterworth polynomial in the denominator of equation (2.16).

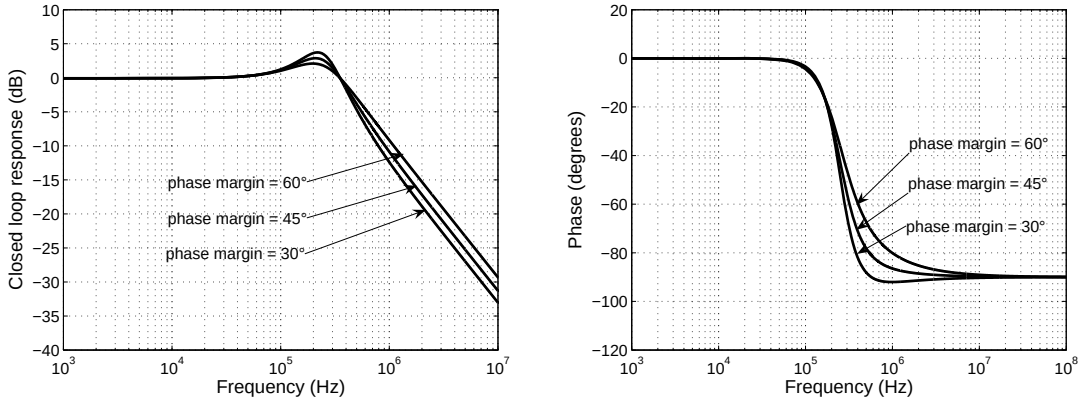
An important tool in the study of PLLs is the Bode plot: a pair of curves, amplitude and phase, which displays the polar components of the open-loop transfer function. Bode plots are valuable for several reasons:

1) They provide visual insight to PLL properties that are not apparent from the algebraic transfer-function equation.
2) Several loop parameters appear as distinctive points on the graphics.
3) They are well suited for experimental analysis of loop stability.



(a) (b)

Figure 2.12 Amplitude and phase of open loop complex phase response.



(a) (b)

Figure 2.13 Amplitude and phase of closed loop complex phase response.

The Bode plot and Nyquist plot for the second-order type II loop is shown in Figure 2.12. Compared with conventional plot method which only presents slopes and poles, this MATLAB plotted Bode plot shows the real gain and phase of the loop. It is

apparent that the amplitude slope is −40 dB/decade at low frequencies and the phase is −180°. The pole reduces the slope to −20 dB/decade and the phase approaches −90°. It is worth noting that a second-order type I loop will present different response. Figure 2.12(b) shows the Nyquist plot of open loop complex phase response. The phase margin, being defined as the difference between the argument of the loop gain and −180° at the frequency where the loop gain is unity, is presented in this plot. The closed loop response, as show in Figure 2.13, is plotted under the condition of 250 kHz natural frequency and phase margin of 30°, 45° and 60°. The amplitude response shows −20 dB/decade slopes and a 0 dB gain when the frequency offset is at the natural frequency.

2.4.3 Third Order Type II Loops

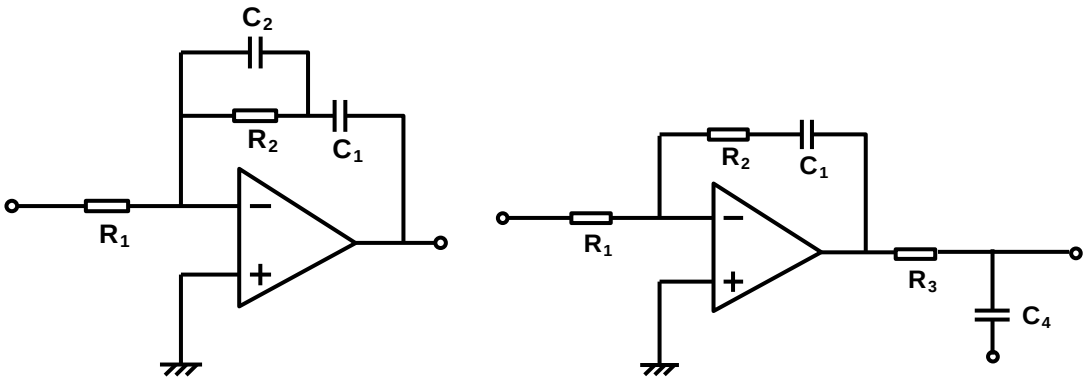


Figure 2.14 Two topologies of single input third order type II loop filters.

The second order type II loop filter considered until now is quite commonly used in PLL circuits because of its simplicity, inherent stability and ease of analysis. However, it does not offer sufficient rejection of high frequency signals from the phase detector, and the gain of the filter itself is a constant value of R_2/R_1 at high frequencies. It can only provide 20 dB/decade noise reduction beyond the natural frequency of the loop. Thus the trade-off between loop bandwidth and reference sideband levels is not particularly good (i. e. higher than −50 dB).

Improvements can be obtained either by using a higher order filter design or by including additional filtering in an existing second order loop design. In the latter case, the filtering should be designed to have little effect on the loop characteristics within or close to the loop natural frequency, so that stability is not impaired. Consequently it

should introduce some useful suppression at higher frequencies to reduce reference sideband levels.

A further pole may be introduced into the filter response by bypassing resistor R_2 with a capacitor C_2, as shown in Figure 2.14. This technique improves the performance of a second order loop filter or, by means of designing the additional component in, may be used to create a third order loop filter. The advantage of a third order loop over a second order loop with additional supplementary filtering is that the response rolls-off more rapidly beyond the loop natural frequency so that greater rejection of loop noise components is possible. This means that, for a given loop natural frequency, the reference sidebands are lower.

The transfer function of this type of loop filter is

$$G(s) = \frac{-\left(\frac{1}{sC_1} + \frac{R_2}{1+sC_2R_2}\right)}{R_1} = -\frac{1}{sC_1R_1}\left[\frac{1+s(C_1+C_2)R_2}{1+sC_2R_2}\right] = -\frac{1}{s\tau_1}\left(\frac{1+s\tau_3}{1+s\tau_2}\right) \quad (2.20)$$

where $\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$ and $\tau_3 = R_2(C_1 + C_2)$. τ_1 is chosen so that the loop gain, $K_PK_VG(s)/N$, falls to unity at the loop natural frequency, ω_n, and τ_2 and τ_3 are chosen to provide the required phase margin, ϕ.

$$\tau_3^2 - \frac{2\tan\phi}{\omega_n}\tau_3 - \frac{1}{\omega_n^2} = 0 \quad (2.21)$$

with the solution:

$$\tau_3 = \frac{\tan\phi + \sec\phi}{\omega_n} \quad (2.22)$$

Since $\tau_2 = \frac{1}{\omega_n^{\,2}\tau_3}$, then

$$\tau_2 = \frac{1}{\omega_n(\tan\phi + \sec\phi)} \tag{2.23}$$

$$\tau_1 = \frac{K_P K_V}{N\omega_n^2}(\tan\phi + \sec\phi) \tag{2.24}$$

hence:

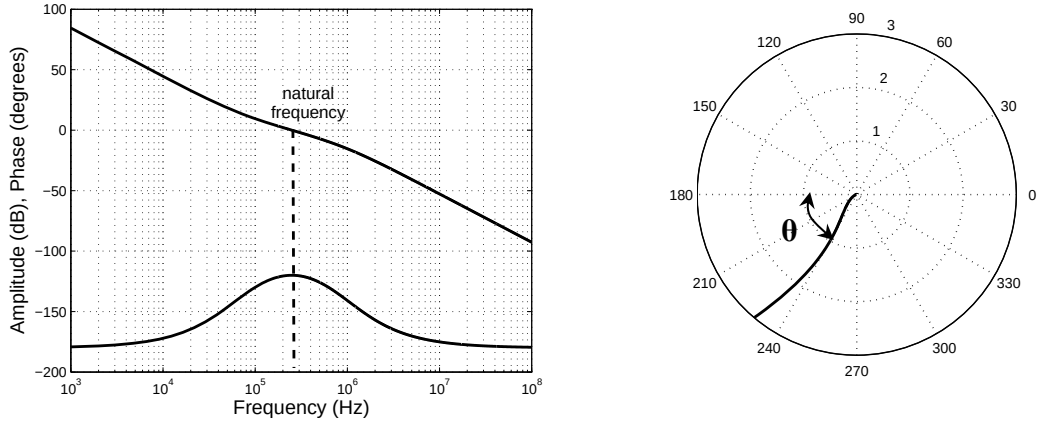
$$R_1 C_1 = \frac{K_P K_V}{N\omega_n^2}(\tan\phi + \sec\phi) \tag{2.25}$$

$$R_2 C_2 = \frac{1}{\omega_n(\tan\phi + \sec\phi)} \tag{2.26}$$

$$R_2 C_1 = \frac{2\tan\phi}{\omega_n} \tag{2.27}$$

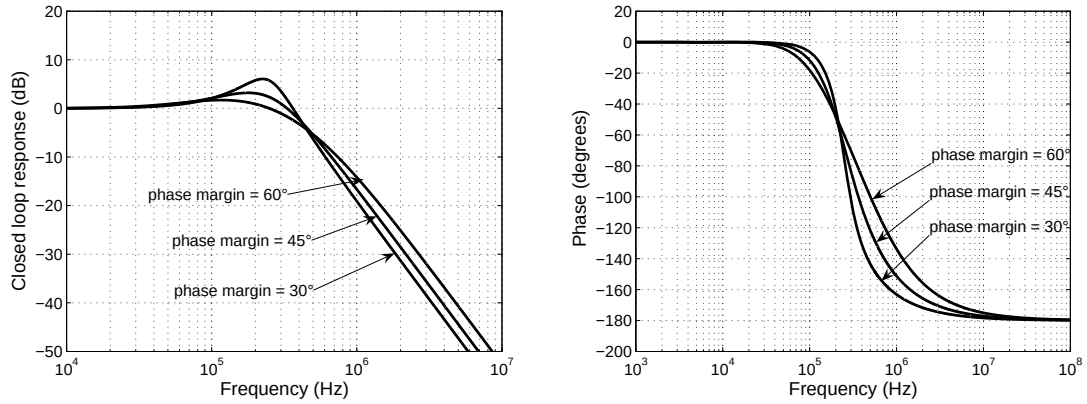
Although the analysis is more complex, the design process is almost as simple for a third order filter as it is for a second order one. Expected natural frequencies and damping factors can be easily achieved by choosing proper resistors and capacitors derived from equations (2.25-2.27). However, because the peak in the filter phase response must occur close to the frequency where the loop gain is unity, the design is more sensitive to errors in the estimation of loop parameters, in synthesiser applications, and in variations in their values with division ratio.

Figure 2.15 shows the Bode plot for a third-order type II loop, the maximum phase margin of 60° occurring, by definition, at the zero gain frequency. 60° is the most frequently used phase margin in real system designs to allow some variation in the hardware loop parameters whilst maintaining stability [1]. The closed loop amplitude and phase responses are as shown in Figure 2.16 (Appendix B), in which the amplitude response slope is −40 dB/decade, providing better noise suppression at higher frequencies.



(a) (b)

Figure 2.15 Amplitude and phase of open loop complex phase response.



(a) (b)

Figure 2.16 Amplitude and phase of closed loop complex phase response.

The phase modulation characteristic of the loop may be found by substituting the new filter response, $G(s)$, into equation (2.5):

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{\dfrac{K_P K_V}{s^2\tau_1}\left[\dfrac{1+s\tau_3}{1+s\tau_2}\right]}{1+\dfrac{K_P K_V}{Ns^2\tau_1}\left[\dfrac{1+s\tau_3}{1+s\tau_2}\right]} = \frac{N\left(1+\dfrac{(\tan\phi+\sec\phi)s}{\omega_n}\right)}{\dfrac{s^2}{\omega_n^2}(\tan\phi+\sec\phi)+\dfrac{s^3}{\omega_n^3}+1+\dfrac{(\tan\phi+\sec\phi)s}{\omega_n}} \tag{2.28}$$

$$\frac{\phi_o(s)}{N\phi_i(s)} = \frac{K_P\phi_o(s)}{NV_{pm}(s)} = \frac{{\omega_n}^2(\tan\phi+\sec\phi)s+{\omega_n}^3}{s^3+\omega_n(\tan\phi+\sec\phi)s^2+{\omega_n}^2(\tan\phi+\sec\phi)s+{\omega_n}^3} \tag{2.29}$$

The frequency modulation characteristic can be derived in a similar way, resulting in

$$\frac{\omega_o(s)}{K_V V_{fm}(s)} = \frac{1}{1+\dfrac{K_P K_V G(s)}{Ns}} = \frac{s^3 + \omega_n(\tan\phi + \sec\phi)s^2}{s^3 + \omega_n(\tan\phi + \sec\phi)s^2 + {\omega_n}^2(\tan\phi + \sec\phi)s + {\omega_n}^3} \quad (2.30)$$

Figure 2.17 shows the normalised phase and frequency modulation response of the third order type II loop. The phase modulation response is a third order low-pass response with a roll-off of −40 dB/decade at high frequencies; the frequency modulation response is a third order high-pass response with a roll-off of 40 dB/decade at low frequencies. The phase modulation and frequency modulation characteristics appear to be mirror images of each other about $\omega = \omega_n$.

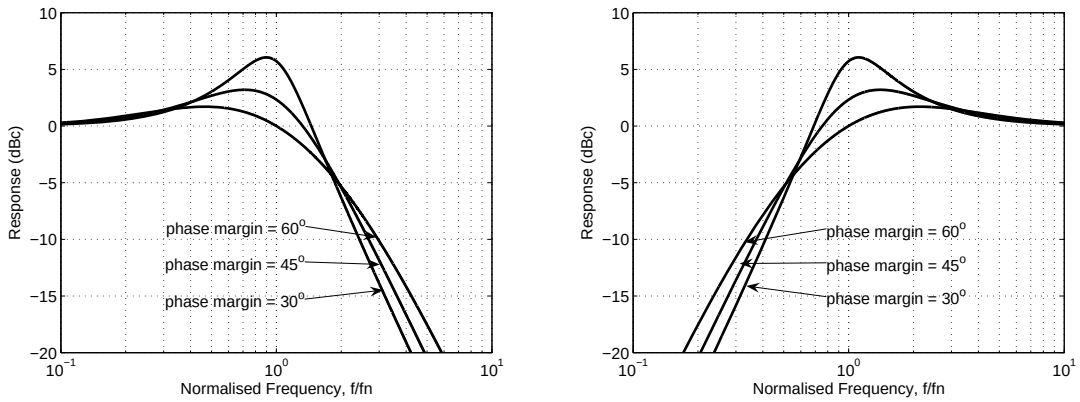


Figure 2.17 Modulation of loop for phase margin of 30, 45 and 60 degrees. (a) Phase modulation response. (b) Frequency modulation response.

2.5 Acquisition

The treatment given so far has assumed that the loop is in lock. But a loop starts out in an unlocked condition and must be brought into lock, either by its own natural action or with the help of additional circuit. The process of attaining lock is called acquisition and is of great importance in many PLL circuits. In frequency synthesisers, one of the most important parameters, tuning speed or switching time demonstrating the ability to

switch between channels within limited time, is directly related to the PLL acquisition [31].

If a PLL acquires lock by itself without the aid of any additional circuitry, the process is called self-acquiring. Any PLL using a phase/frequency detector falls into this category since this type of phase detector provides a very clear indication of the frequency deviation of the loop from its locked condition. Conversely, a PLL which is unable to acquire lock rapidly enough, or at all, by itself may require additional aided acquisition circuitry to assist the acquisition process. PLLs using analogue multiplier phase detectors are the most likely to require aided acquisition since their acquisition range (or capture range) is the smallest of all the commonly used phase detectors [32].

Besides the phase detector in a PLL, there are also some basic requirements on the VCO to satisfy the lock condition of the loop. Any PLL failed to satisfy these conditions is not able to lock at all.

1) The modulation bandwidth of the VCO must be wider than the noise bandwidth of the PLL response, meaning that the tuning speed of the VCO has to be fast enough to cover the desired range of operation.
2) Some external frequency lock devices may be necessary for some combinations of phase detector and VCO lack of self-acquiring mechanism.

The following definitions and results apply to PLLs using phase/frequency detectors and active loop filters which are widely used in frequency synthesisers, meaning that the PLL can keep locking without additional acquisition circuitry. The maximum phase error in the PLL can be expressed as [33]:

$$\lim_{t\to\infty}\theta_e(t) = \lim_{s\to\infty} s\theta_e(s) = \frac{\Delta\omega}{K_P K_V G(0)} \tag{2.31}$$

With the assumption $\theta \approx \sin\theta$, the maximum amount is 1 and therefore

$$\Delta\omega_H = K_P K_V G(0) \tag{2.32}$$

For an active loop filter, its zero point transfer function $G(0)$ is infinite and therefore

$$\Delta\omega_H = \infty \tag{2.33}$$

where $\Delta\omega_H$ is hold-in range which represents the range of frequencies that the loop will remain in lock after initially being locked [34].

If signal frequency is close enough to VCO frequency, a PLL locks up with just a phase transient; there is no cycle slipping prior to lock [35]. The frequency range over which the loop acquires phase with out slips is called lock-in. The lock-in limit for a second-order type II PLL can be described as [36, 37]:

$$\Delta\omega_L \approx 2\zeta\omega_n \tag{2.34}$$

The time taken for the loop to reach phase lock once the frequency error is within the lock-in limit is given approximately by [38]

$$T_L \approx \frac{1}{\omega_n} \tag{2.35}$$

The calculation referred to the phase lock. It becomes apparent from these equations that for damping factor $\zeta = 0.707$, the lock-in range is only equal to or slightly larger than the loop bandwidth. To move the VCO frequency within these limits, additional functions are required. This area is called frequency lock.

If the initial frequency offset is beyond $\Delta\omega_L$ but within the pull-in limit, then the loop is able to acquire lock but slips cycles during the acquisition process. The phase detector forms a beat note equal to the frequency offset of the loop from lock [39, 40]. The beat note generated at the output of the phase detector is an AC voltage together with a DC component. This DC component serves to adjust the mean frequency of the VCO and so bring the loop closer to lock. The process then accelerates until lock is acquired. Analysis of the situation is complicated and involves many approximations. An approximate expression for the pull-in limit is [41]

$$\Delta\omega_P = \pi\sqrt{\frac{2\zeta\omega_n K_P K_V}{N}} \tag{2.36}$$

The corresponding pull-in time is given by [42]

$$T_P \approx \frac{\Delta\omega^2}{2\zeta\omega_n{}^3} \tag{2.37}$$

from which it can be seen that for narrow loop bandwidths the pull-in time may be unacceptably long. A further practical factor which has not yet been taken into consideration is that the lock-in limit may be greatly diminished by the phase detector DC offset. This offset can very easily exceed the small DC component of the phase detector output and, if its polarity is unfavourable, prevent lock from occurring. In a loop using an active filter this invariably means that the loop latches-up at one of its extreme values of VCO frequency [26].

There are several ways of helping a PLL to attain lock. The most common of these involves the use of a DC signal inserted at the loop filter input which linearly sweeps the frequency of the VCO. If the sweep rate is sufficiently low, then when lock is imminent the natural action of the loop takes over from the imposed sweep signal bringing the frequency sweep to a halt and allowing the loop to lock. A lock detector is then used to disable the sweep signal.

A different method for aiding acquisition is to initially widen the loop bandwidth. A loop can be built to have a large bandwidth for rapid acquisition and a much narrower bandwidth for good tracking in the presence of noise. This is a useful technique for improving the tuning speed of synthesisers whilst maintaining good reference sideband suppression, but is not as useful for low-level applications since the loop noise bandwidth is also widened which may make it impossible for the loop to respond [1]. Other more elaborate techniques include the use of frequency discrimination to detect when the loop is close to lock without relying on the natural loop characteristics to halt the frequency sweep. This open-loop technique enables a higher sweep rate to be used but does require that the discriminator has a rapid response so that the sweep is disabled before the VCO frequency overshoots the required value.

2.6 Summary

Within this chapter, the basic concepts of PLLs are introduced and fundamental components of a typical PLL are analysed. To work as a fractional-*N* frequency synthesiser, the frequency divider must divide by consecutive values rather than a fixed ratio. Furthermore, the frequency divider is programmable and it is controlled by some digital block. Second order and third order loops are commonly used in frequency synthesisers because of their good stability tolerance and simple architecture. Higher order designs can provide better noise suppression beyond cut-off frequency of the loop. The phase noise at high offset frequencis is able to be effectively suppressed, which is very important especially in a wide bandwidth application. The real frequency synthesiser design throughout this work employs a third order topology. In order to benefit from sufficient noise suppression without affecting stabilities at the same time. Extra poles with high cut-off frequencies are added. This will be presented in the following prototype designs.

Chapter 3

Sigma-Delta Fractional-*N* Frequency Synthesis

3.1 Introduction

Several different frequency synthesis techniques have been invented and widely used in a variety of electronic applications over years. They can be classified into three separate categories, namely direct digital synthesis, direct analogue synthesis, and indirect analogue synthesis. In this context, "indirect" refers to a system based on some kind of feedback action, mostly PLL topology; whereas "direct" refers to a system having no feedback. The direct digital synthesiser usually employs a look-up table, and the waveform is created piece by piece by using the digital values of the waveform stored in a memory [43]. The direct analogue synthesiser synthesises the wanted output frequency from a single reference by multiplying, mixing or dividing. Indirect analogue synthesis is the most suitable technique for the synthesis of high-frequency sinusoidal signals because no block has to operate at a frequency higher than the output frequency. Also, they are suitable for monolithic implementation to reduce the fabrication size, cost and power consumption. As a result, almost all the microwave and radio frequency applications employ indirect methods to generate stable frequencies.

PLL-based frequency synthesis is an essential technique utilised in wireless communication systems for local oscillator (LO) generation. Frequency synthesisers provide many of the RF and microwave signals in communications, radar, and microwave systems. Such synthesisers come in many forms and performance levels, from tiny PLL integrated circuits (ICs) to rack-mountable subsystems and precision test instruments with programmable control. The ultimate goal in any design of frequency synthesisers is to generate stable and clean output frequencies with minimal spurious and phase noise, although they come in many shapes and sizes.

There are three kinds of indirect analogue synthesisers in practical systems, including integer-*N* synthesis, fractional-*N* synthesis and multi-loop synthesis. The architecture

simplicity of integer-*N* PLL frequency synthesiser [44, 45] has made them a popular choice for almost all kinds of telecommunications system. However, the integer-*N* architecture has a major drawback: the frequency resolution equals to the reference frequency, meaning that only integer multiples of the reference frequency can be generated. In addition, stability requirements limit the loop bandwidth to about one tenth of the reference frequency and thus the loop bandwidth needs to be even smaller for the reason of noise suppression. As a result, the dynamic behaviour of the integer-*N* synthesiser is limited.

Fractional-*N* synthesisers break this coupling between resolution and agility: the frequency steps can be very small, whist the reference frequency can be very high indeed [46-48]. In these synthesisers, rational multiples of the reference frequency can be synthesised, allowing a higher reference frequency for a given frequency resolution, which means that the loop bandwidth can be increased, without deteriorating the spectral purity. In addition, these synthesisers offer the dual advantages of significant improvement in reducing the PLL phase noise and shorting the lock times. Therefore, the synthesiser switching time is reduced and the capacitance required in the loop filter can be decreased, such that the integrated frequency synthesisers become feasible and they are suited to various portable applications.

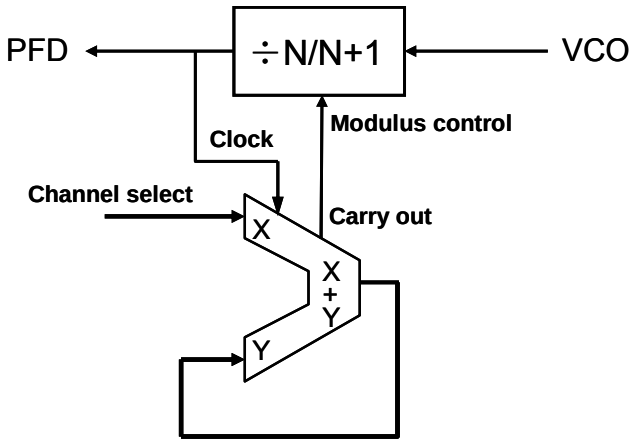


Figure 3.1 The Fractional-*N* frequency divider controlled by a digital accumulator.

The main difference of fractional-*N* synthesis is division by fractional ratios, instead of only integer ratios in integer-*N* synthesis. To accomplish fractional division, a similar frequency divider as in an integer-*N* frequency synthesiser is employed, but the division

is controlled differently. Figure 3.1 shows the simplest fractional divider controlled by the carry out signal of a single digital accumulator of *k*-bit width to illustrate the fractional division theory. The carry out bit of the accumulator circuit is used to control the choice of divider values, which leads to a periodic dithering pattern. To realise a fractional division ratio $N+n$, in which *N* is an integer and *n* is a fraction with $n \in [0, 1]$, a digital input $K = n \cdot 2^k$ is applied to the accumulator. The carry out is produced every *K* cycles of the reference frequency f_{ref}, which is also the sampling frequency of the digital accumulator. This means that the frequency divider divides $2^k - K$ times by *N* and *K* times by $N+1$, resulting in a division ratio N_{frac}, given by

$$N_{frac} = N + n = \frac{\left(2^k - K\right) \cdot N + K \cdot \left(N+1\right)}{2^k} = N + \frac{K}{2^k} \tag{3.1}$$

The equation states that for a given reference frequency, it is possible to make the frequency resolution arbitrary fine by choosing a sufficiently large width of the accumulator. For example, in a GSM-900 handsets the channel spacing of 200 kHz is synthesised by using a reference frequency of 13 MHz, so the accumulator input range is $\frac{13MHz}{200kHz} = 65$. An accumulator with an input width *k* of 7 bits, $2^7 = 128$, can cover all of its channels.

When the PLL is locked, the VCO output frequency f_{out} is equal to N_{frac} times the reference frequency, f_{ref}, such that

$$f_{out} = N_{frac} \cdot f_{ref} = N \cdot f_{ref} + \frac{K}{2^k} \cdot f_{ref} \tag{3.2}$$

The VCO output frequency can be controlled by altering the divider value, N_{frac}. Thus the circuit behaves as a phase multiplier and also, since frequency is the time derivative of phase, as a frequency multiplier.

Since the fractional division is applied to a PLL system, it is important to investigate what happens to the phase in the loop, to fully understand the effects on the overall loop performance. During each cycle of the reference clock, the accumulator accumulates the input *K* until the accumulator output overflows. At overflow, the carry output is set

high and $2k$ is subtracted from the accumulator output. The resulting accumulator output is a sawtooth waveform with a frequency depending on n, as shown in Figure 3.2 for $n = 0.25$. The carry out of the accumulator is then used to control the division ratio of the divider. The carry out has a mean value of n, but the instantaneous value is merely a "prediction" of the mean value, since the output can only be 0 or 1. Therefore, the frequency divider is dividing only by integer ratios, N or $N+1$, while the output of the PLL is a fractional multiple of the reference frequency, giving rise to an increasing phase difference between two phase detector inputs. The phase detector output starts to accumulate. When the accumulator overflows, the divider modulus is changed from N to $N+1$, meaning that one output period of the VCO is "swallowed" by the frequency divider. This causes a phase shift at the input of the phase detector that eliminates the previously accumulated phase error. Figure 3.2 shows the time diagram of the open loop output of the phase detector versus the VCO output and f_{ref} for $n = 0.25$. It is evident that the periodic dithering pattern leads to a periodic phase error pattern with lower frequency than the reference frequency. Suppression of the resulting spurious noise requires that the bandwidth of the synthesiser be carefully chosen below the frequency of the periodic error pattern, which undermines the objective of obtaining a high bandwidth and fast lock-in time [49, 50].

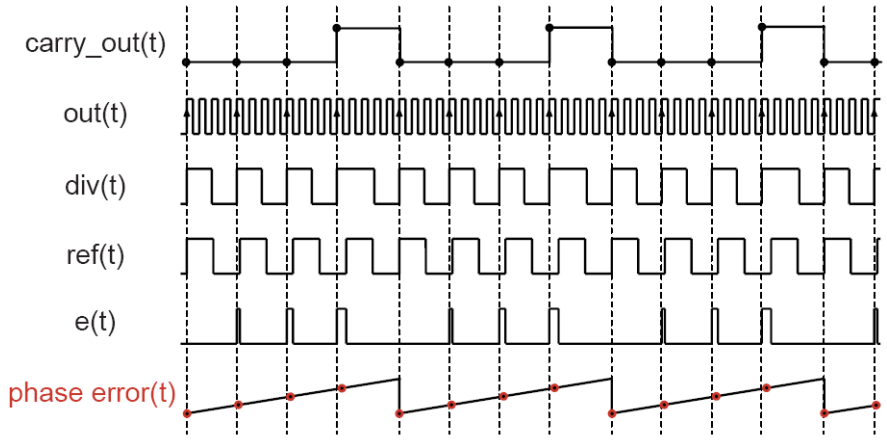


Figure 3.2 The time diagram of the VCO and frequency divider output, carry out and phase error for $n = 0.25$.

Fractional-N synthesisers work by periodically changing the division ratio from N to $N+1$ and back such that the average is $N + F/M$, where $0 \le F < M$; N, F and M are integers and F/M is the *fractionality*. For example, if N is 5 for 37 cycles and 6 for 63 cycles, 5.63 is the average division ratio, so a frequency counter would read 5.63 times

f_{ref}. In fractional-*N* synthesis, especially with Σ-Δ modulation, as shown in Figure 3.3, the choice of the reference frequency is almost completely independent of the step size since the latter is related to the former by the following relationship:

$$\text{Step size} = \frac{f_{ref}}{2^k} \tag{3.3}$$

where the exponent, *k*, is the number of bits in the input of the accumulator. For example, if f_{ref} is 13 MHz for the GSM-900 system, with *k* equal to 10 bits, a step size as small as 12.695 kHz can be achieved. Obviously, the benefit of fractional-*N* is that small step size and high reference frequency can be hopefully achieved at the same time, at least in principle. In practice, the discussed topology is not able to satisfy all of these requirements due to significant spurs which will be present on the VCO output spectra.

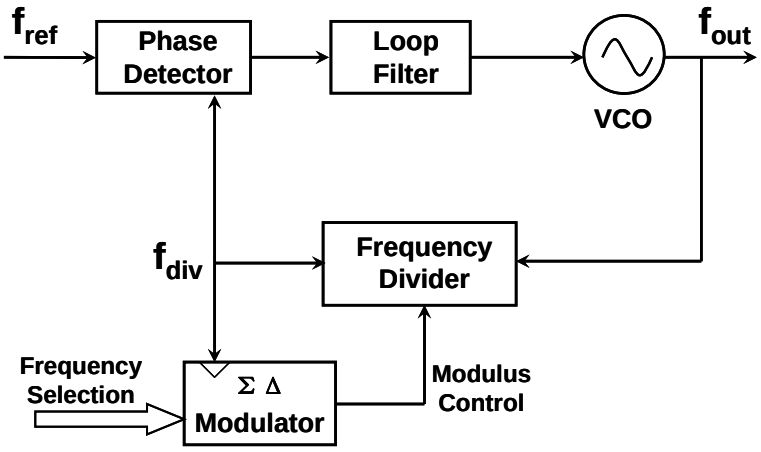


Figure 3.3 A typical arrangement of a Σ-Δ fractional-*N* frequency synthesiser.

The combination of a Σ-Δ modulator and a multi-modulus frequency divider leads to much better performance than the single accumulator method indicated in Figure 3.1, especially the spurious components reduced by noise shaping. The divider is controlled by a form of the Σ-Δ modulator and the division ratio $N + \Delta N$ is not necessarily confined to N and $N+1$ but may span multiple modulus values. The VCO frequency is governed by the long-term mean of Δ*N* which is exactly *F*/*M*. Noise shaping moves the quantisation noise produced at the PFD output to higher frequencies where it is removed by the low-pass filter action of the PLL [1].

Low phase noise may be achieved by the use of a high reference frequency and an associated low division ratio. With Σ-Δ fractional-*N* synthesisers, the reference can be tens of MHz. For example, 13 MHz and 26 MHz reference frequencies are chosen by GSM-900 and DCS-1800 handset applications, respectively. As a result of the high reference frequency, reference feedthrough spurs are simply not an issue at all, because they can be easily deleted or partially removed by the loop filter. Also, the step size can be arbitrarily small. Many synthesisers with a step size of less than 1 Hz have been implemented and reported while using a high reference source. Tuning speed is increased because of a widened loop bandwidth. It can be further improved with the addition of some form of pre-tuning or fast lock feature. The main problem afflicting fractional-*N* synthesis is fractional spurs which dominate the whole band and adversely affect the performance. However, they can be suppressed to a degree by using the appropriate Σ-Δ modulator architecture and introducing dithering and optimisation techniques. The detailed analysis and strategies will be discussed as follows.

3.2 Frequency Dividers

Together with the Σ-Δ modulator or some other digital blocks with similar dithering and noise shaping functions, the frequency divider is a digital component of PLL frequency synthesisers. To generate frequencies in a range, the division ratio of the feedback system must not be a constant value for a time cycle or longer. The frequency divider is controlled to implement variable division ratios by one or more digital blocks, so that it can adjust the VCO to a desired output frequency.

3.2.1 Dual-Modulus Dividers

Dual-modulus dividers are used in frequency synthesisers as a cost effective solution with wide usage not only limited to frequency synthesisers. They have many merits: simple architecture, high operating frequency, low cost and good power efficiency. In a fractional-*N* synthesiser, the actual programmable divider is used to switch the modulus of the prescaler between two consecutive values, *N* and *M*. The dual modulus divide-by-*N*/*M* divider performs frequency division to produce an output with a cycle time that is equal to either *N* or *M* cycles of its input. If the programmable divider divides by *C*,

and the prescaler is made to divide by N for A cycles and by M for the rest $(C-A)$ cycles, the total division ratio will be

$$N = N \cdot A + (C - A) \cdot M \tag{3.4}$$

Compared with fixed ratio frequency division, dual-modulus increases the complexity of the divider only slightly, but it avoids the problems of increasing N and decreasing the reference frequency. Conventionally, dual modulus dividers are implemented by using a synchronous divide-by-2/3 stage followed by asynchronous divide-by-2 or divide-by-4 stages [51, 52]. The modulus of the divide-by-2/3 stage is controlled by the outputs of the asynchronous stages and the modulus control input signal in such a way that the total modulus of the prescaler can be switched between two consecutive integer values. The advantage of this topology is that only a small section of the overall divider operates at the high frequency of the input; the stages that follow operate at progressively lower frequencies. The conceptual block diagram of a complete $\div 8/9$ dual-modulus prescaler is shown in Figure 3.4. The core of the divide-by-2/3 state machine is a divide-by-2 circuit that swallows an extra input cycle when a binary control signal, *MC*, is asserted. The number of input cycles swallowed per output cycle is limited to be either zero or one by the control qualifier block. The $\div 8/9$ prescaler produces an output consisting of 9 input cycles when *MC* is set to 1 in the previous output cycle. When *MC* is set to 0, the input cycle is not swallowed so that the output consists of 8 input cycles.

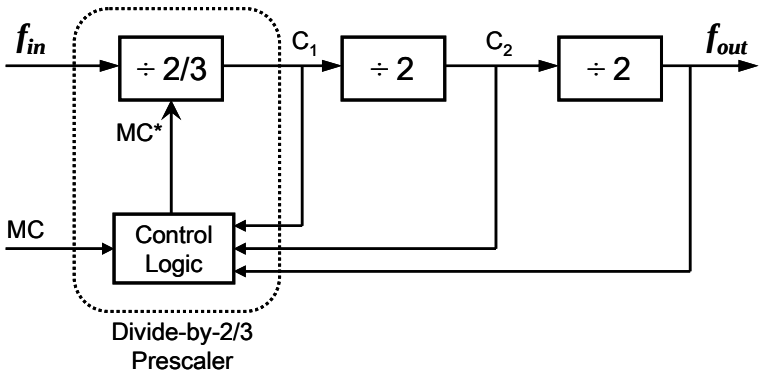


Figure 3.4 A divide-by-8/9 dual-modulus divider.

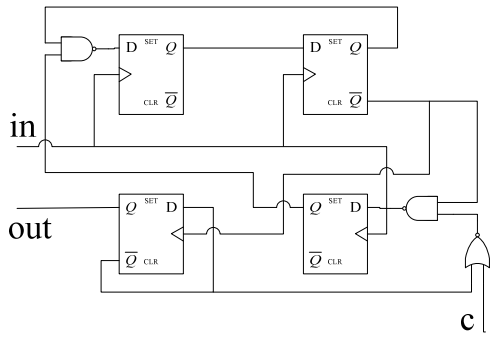


Figure 3.5 Logical architecture of a divide-by-8/9 prescaler.

Figure 3.5 illustrates an alternative ÷8/9 divider implemented by four D-type flip-flops and several logic gates. Its architecture is similar to the divide-by-2/3 core and without any other fixed ratio dividers, so that its cascaded delay is smaller than the cascaded divider. This divider consists of three flip-flops as a synchronous block driven by the input clock, meanwhile another flip-flop acts as an asynchronous divider-by-2 block with asynchronous driving clock. In practice, the timing of the feedback signal from the asynchronous dividers can be critical, and special attention must be paid to the design of the logic gates in the feedback path. The maximum operating frequency of this prescaler is naturally limited by the synchronous divide-by-4/5 stage, since the rest of the circuit operates with a speed of one fourth of the input frequency, or lower. In comparison to the divider shown in Figure 3.4, this architecture is able to work at higher frequencies, because the feedback modulus control signals as shown in Figure 3.4 slow down the operation.

3.2.2 Multi-Modulus Dividers

With the rapid development of wireless communication systems, the need for fine channel resolution, fast tuning and high spectral purity has led to the adoption of multi-level Σ-Δ modulators in which, of course, the modulus of the divider must often be controllable over a wider range than only two consecutive values. The modulus control could be for example a 3-bit word, which would require a prescaler that has $2^3 = 8$ possible modulus values. Therefore, multi-modulus dividers have been playing an increasingly significant role in Σ-Δ fractional-*N* frequency synthesis. In a synthesiser context, the Σ-Δ modulator and the frequency divider provide a fractional mean division ratio with low close-in phase noise at the expense of increasing phase noise further from

the carrier where it may be readily suppressed by the action of a PLL Loop filter [1]. Multi-modulus division provides adequate randomisation of noise shaping sequence, so that the noise profile is whitened with continuous spectra.

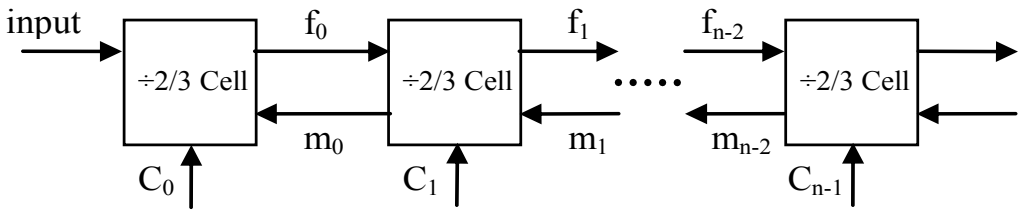


Figure 3.6 The architecture of a conventional ripple fashion divider.

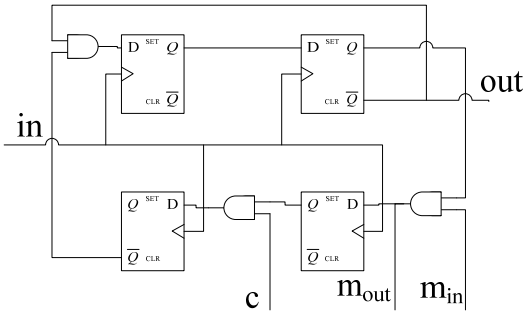


Figure 3.7 A divide-by-2/3 cell in ripple fashion dividers.

Ripple fashion and phase-switching are two main multi-modulus prescaler architectures commonly used in fractional-*N* synthesisers. A conventional ripple fashion architecture [53, 54] is shown in Figure 3.6, in which the prescaler structure is based on the cascade of *n* divide-by-2/3 dual-modulus blocks. Each divide-by-2/3 block divides its input by 2 or 3 depending on its modulus control signal C_n and the feedback signal m_n simultaneously, as shown in Figure 3.7. Firstly, each divide-by-2/3 block divides its input by 2 or 3 depending on its control signal C_n. However, to prevent the block from continuously dividing by 3 when its control is high, an extra condition is required such that it divides by 3 only once during a complete division cycle of the whole prescaler. This is achieved by using the input feedback signal, m_n, which has to be high for the block to be divided by 3. Otherwise, it will continue dividing 2 even if C_n is high. The feedback signals are generated from the last block (operating at the lowest frequency thus does not need an input feedback signal) and propagate up the chain. Division by 3 of a block in this context means that the block swallows an extra single input pulse in a

complete division cycle, thus increases the period of the block's output signal by one period of its input signal. A cascade of *n* blocks can produce division ratios over the range 2^n to $2^{n+1}-1$. The resultant range of available modulus values is thus:

$$N_{RF} = 2^{n+1} - 2^n \tag{3.5}$$

For example, if *n* is 6, the divider has 64-modulus with division ratios from 64 to 127. In an odd number dividing mode, the propagation delay time of the control signal, which returns from the next stage, is critical. In an even number dividing mode, the divided signals are transferred to the next stage in turn. So there is no limitation with high frequency operation. However, the flip-flop and latch circuit, which transfers a signal to the next stage, was designed to have a higher driving capability. Thus, a return signal of the control signal to the previous stage is sent quickly, and the large operating margin can be obtained in an odd number dividing mode.

Power optimisation of this structure may be achieved by downscaling the current of the cascaded blocks, such that the power dissipation of each block decreases as its input frequency decreases. Feedback lines are only present between adjacent blocks. This simplifies the layout and decreases potential parasitic capacitances due to long paths thus an obvious advantage of this structure. The topology of the cascaded divide-by-2/3 blocks is the same thus lends itself of better reusability and programmability that facilitates the layout work [53].

An alternative multi-modulus architecture is the phase switching prescaler, multiplexing the output of the divider. As illustrated in Figure 3.8, the phase-switching prescaler generates four 90° space phases using two stages of divide-by-2 cells in cascade. The phase-switching architecture makes use of the internal structure of a D flip-flop. A divide-by-2 stage is usually a flip-flop consisting of two latches: a master latch and a slave latch. The outputs of these latches have a 90° degree phase difference with each other. Therefore, the second divide-by-2 flip-flop has four outputs: the "usual" D flip-flop outputs after the slave latch (0° and 180°), and the quadrature outputs after the master latch (90° and 270°). Then it uses a 4-to-1 multiplexer (MUX) to switch from one phase to the next phase lagging 90°. One of these four phases is directed to the

output at any given time, and input cycles are swallowed by shifting the output from one phase to another.

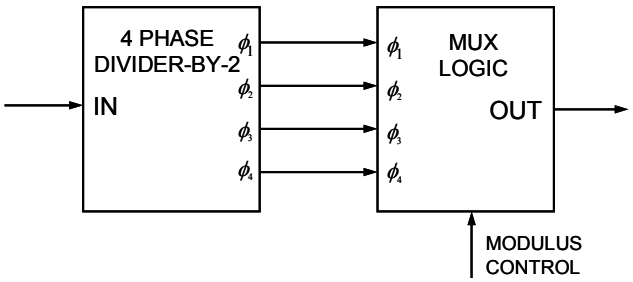


Figure 3.8 The architecture of a multi-modulus phase switching prescaler.

The core block is extended by introducing some fixed high frequency prescalers which are connected to the input and followed by some low frequency dividers to achieve flexible multi-modulus frequency division. For example, a divide-by-64/65/66/67 divider can be achieved by using a divide-by-16 divider. Modulus 64 is accomplished by selecting one of the signals at the output of the second divide-by-two flip-flop (e.g. the 0° signal), and dividing this signal further by 16. The total modulus will thus be $4 \times 16 = 64$. Dividing by 65 is accomplished by switching the signal directed to the divide-by-16 stage once per output period. The switching is done so that the selected new signal always lags the previous one by 90°, e.g. from the 0° signal to the 90° signal. Switching 90° forward at one fourth of the input frequency corresponds to switching 360° forward at the input frequency, i.e. swallowing one input pulse. If one input pulse is swallowed once per output period, the final modulus will be $(4 \times 16) + 1 = 65$.

The MUX circuitry operates at one fourth the input frequency, and thus the power dissipation can be reduced. This architecture exploits the toggling speed of a flip-flop or even an analogue divide-by-2 frequency divider, and thus, it can work much faster than the prescalers based on the synchronous counter. However, the main drawback of this approach is the potential glitches, which can cause the following counter to miscount. If the actual phases of the output signals are not exactly 0°, 90°, 180° and 270°, but for example 0°, 89°, 180° and 179°, a spurious tone will appear at a fraction of the output frequency. This means that the speed of phase switching prescalers is seriously affected.

3.3 Sigma-Delta Modulators

3.3.1 Introduction to Sigma-Delta Modulation in Frequency Synthesis

The Sigma-Delta (Σ-Δ) technique is well known in the field of communications and has been used extensively for analogue-to-digital (A/D) conversion applications. A/D converters based on Σ-Δ techniques are now widely used in signal processing and electronic applications. In the past 30 years, analogue Σ-Δ modulators have developed rapidly and are mainly used in data converters [56-58]. On the other hand, digital Σ-Δ modulator designs have received less attention though this situation has changed recently since they are used as a digital control component in PLL fractional-*N* frequency synthesisers. Σ-Δ modulators in fractional synthesis were first introduced and analysed by Miller [59, 60] and further refined by Riley [5]. In recent years, they have draw most attention to evaluate the performance of fractional-*N* synthesisers. New topologies and techniques have emerged to provide better noise performance in these synthesisers.

As mentioned before, Σ-Δ modulators are playing an increasingly important role in both frequency synthesis and A/D conversion. They are capable of achieving the same resolution as Nyquist-rate multi-bit quantizers by employing a 1-bit quantizer operating at many times the Nyquist rate. The modulators generally require less components than Nyquist-rate converters, and they are more robust against circuit imperfections because of much higher sampling frequencies and over-sampling rate [61].

Figure 3.9 presents a fuction demonstration of a basic Σ-Δ modulator. The input is a continuous analogue signal indicated by the curved line; the output has two states (high and low) which provides a sequence in response to the input. In fact, the shown output is an over-simplified version, in order to clarify the performance of Σ-Δ modulators in which the over-sampling rate can be greatly reduced [57]. It can be seen from the figure that, while the input has high positive amplitude, the output consists mostly of 1s; similarly, when the input has high negative amplitude, the output consists mostly of −1s; when the input is nearly zero, the output oscillates between 1 and −1. It is clear from

this behaviour that, as the over-sampling rate is increased, an average value of the output is approximated toward the input.

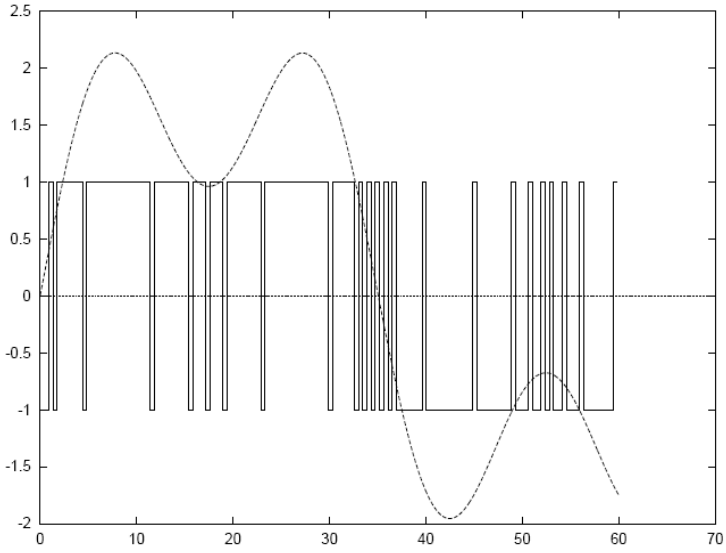


Figure 3.9 Time domain function diagram of a basic Σ-Δ modulator.

The fundamental operation of Σ-Δ modulators relies on the fact that the spectrum of the quantisation noise is shaped, such that a small amount of noise power remains within the useful signal band, while the rest of the quantisation noise is pushed to higher frequencies where it is then eliminated by analogue filtering, such as a low-pass filter. The same principle can also be exploited in fractional-*N* frequency synthesis applications by pushing the quantisation noise towards higher frequencies, so that the phase noise in the vicinity of the desired carrier frequency is small. The high frequency phase error is subsequently suppressed by the loop filter, which has a low-pass characteristic. The Σ-Δ modulator is employed to generate a digital signal to control the frequency division ratio. To address industry requirements, Σ-Δ modulator design must consider the desirable performance: low power consumption (for portable applications), high operating frequency, simple architecture, good noise performance, high agility (low noise) in base station applications.

Although tens of topologies of Σ-Δ modulator have been invented in the last 30 years, they can roughly be classified into two kinds: single stage and Multi-Stage Noise Shaping (MASH), which will be compared and analysed as follows. All of the Power Spectral Density (PSD) is obtained from Σ-Δ modulators which are simulated or measured under the same condition of a random selected input of 0.46.

3.3.2 First Order Sigma-Delta Modulator

Normally a first order Σ-Δ modulator consists of an analogue comparator, an analogue integrator and a 1-bit quantizer in a feedback loop. The difference between the input signal and the quantised output value (i.e. the quantisation error between the current input and the previous sampled output) is integrated. The output of the integrator is then quantised to 1-bit to generate the output value, which is fed back for comparison to the input during the subsequent sampling period. The quantised output is fed to input for comparison to the DC input. It also introduces a delay so that the previous output is compared to the current input. Although the quantisation error at any particular instance is high due to the coarse nature of the two-level quantizer, the repeated action of the feedback loop produces a string of 1 or 0 output which can be averaged over many sampling periods to give a very precise result.

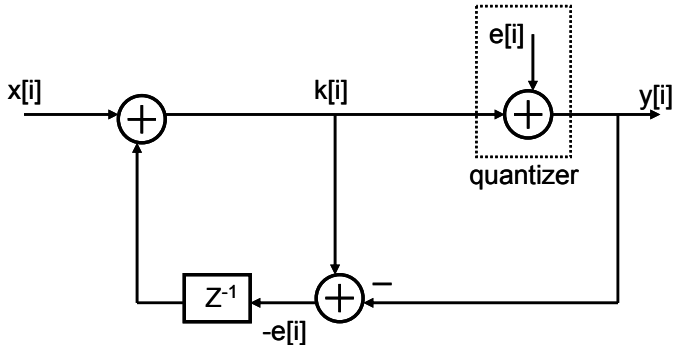


Figure 3.10 First-order Σ-Δ modulator with error-feedback topology.

A block diagram of the first-order Σ-Δ modulator with an error-feedback topology is shown in Figure 3.10, where the quantizer is modelled as an additive white noise source $e[i]$. This simple structure is often used in A/D applications since the loop is perfectly implemented in the digital domain [62]. A simple accumulator, as shown in Figure 3.1, can be used as the digital implementation of the first-order Σ-Δ modulator with the error-feedback topology shown in Figure 3.10. The accumulator overflow and the accumulation result correspond to the 1-bit quantizer output and the inverse of the quantisation error at any time, respectively. Supposing the width of the accumulator is k-bit and the accumulated value with a number between 0 and $2k + 1$ is added to the input. If this number is larger than $2k$, the carry out of the accumulator is set to 1 and $2k$ is subtracted from the accumulated value. The discrete time behaviour of the transfer function is described as

$$y[i] = x[i] + (e[i] - e[i-1]) \tag{3.6}$$

$$Y(z) = X(z) + (1 - z^{-1})E(z) \tag{3.7}$$

As can be seen from equations (3.6) and (3.7), the carry out of the accumulator is a delayed version of the input with high passed quantisation noise. The 1-bit quantizer generates a pre-defined 2-level digital output, i.e. 0 and 1. Figure 3.11 presents a comparison of simulated and theoretical quantisation noise, in which the theoretical plot is generated by equation (3.7). In the frequency domain, this feedback system tends to push quantisation noise to high frequencies. However, its simple architecture can only provide limited randomisation and the noise power is concentrated around some high spurious components, which leads to a series of spurs with higher amplitude than the simulated characteristic. The phase error of the first order Σ-Δ modulator is presented in Figure 3.12, which shows apparent repetition of dithering sequence length.

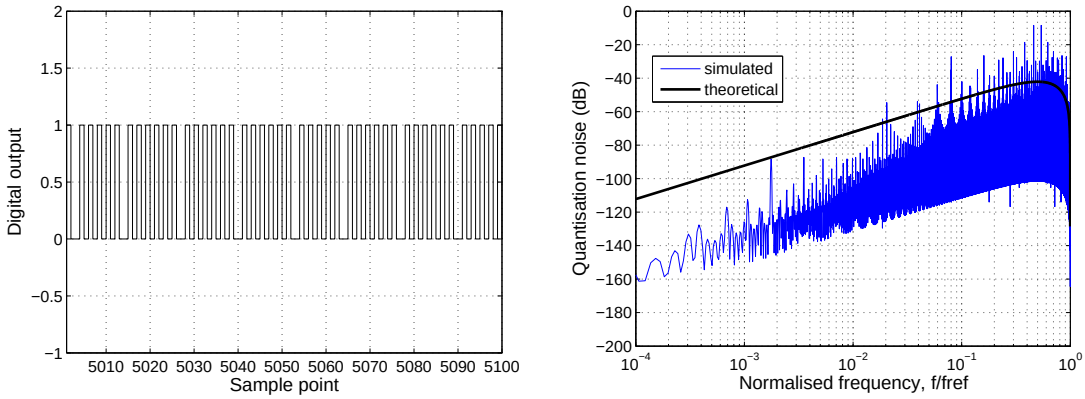


Figure 3.11 Time domain output and quantisation noise of a first-order Σ-Δ modulator.

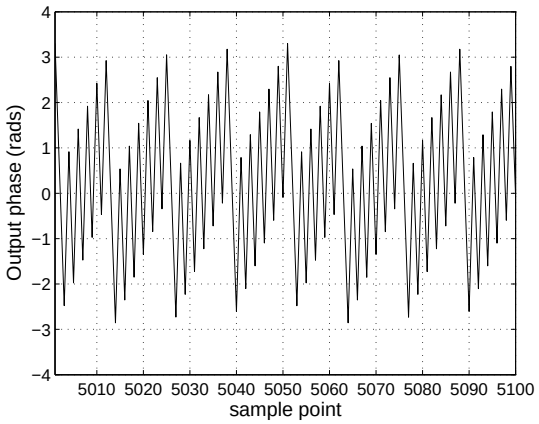


Figure 3.12 Phase error of the first-order Σ-Δ modulator.

3.3.3 MASH 1-1-1

The third order multi-stage noise shaping (MASH) [63-65] modulator is one of the most popular architectures, which is widely used in A/D conversion and frequency synthesis. The MASH 1-1-1 Σ-Δ modulator is cascaded by three first order Σ-Δ modulators with 1-bit quantizers. Its architecture is shown in Figure 3.13.

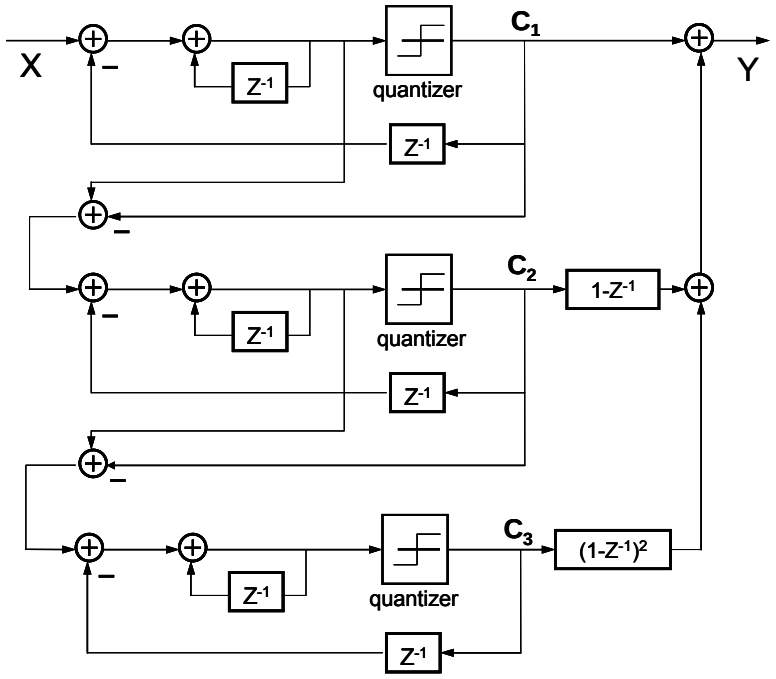


Figure 3.13 Block diagram of a MASH 1-1-1 Σ-Δ modulator.

There are two obvious advantages that promote this architecture to become the focus of attention: first, its architecture is with less complexity compared to all the other third order Σ-Δ modulators. To implement such a digital modulator, only three accumulators and latches are necessary. Single-stage modulators with the same order demand more registers to achieve their functions. The overflow from each accumulator is 1-bit, i.e. 0 or 1, so the noise cancellation logic is simple, which is similar to the pipeling technique. The other significant merit of the MASH architecture is that it can work at much higher frequencies. Signal delays are cancelled by the following stage which can maximise sampling frequencies. If implemented by the same monolithic circuits or FPGA techniques, the MASH architecture will work at much higher sampling frequencies than single stage Σ-Δ modulators, benefiting from its simple error cancellation logic. The Noise Transfer Function (NTF) of the MASH 1-1-1 modulator is derived as follows:

$$C_1(z) = \left(1 - z^{-1}\right) \cdot E_1(z)$$

$$C_2(z) = -E_1(z) + \left(1 - z^{-1}\right) \cdot E_2(z)$$

$$C_3(z) = -E_2(z) + \left(1 - z^{-1}\right) \cdot E_3(z)$$

$$NTF_1 = \frac{Y(z)}{E(z)} = \frac{C_1(z) + \left(1 - z^{-1}\right) \cdot C_2(z) + \left(1 - z^{-1}\right)^2 \cdot C_3(z)}{E(z)} = \left(1 - z^{-1}\right)^3 \tag{3.8}$$

where C_1, C_2, C_3 are the carry out signals of the first, second and third accumulators respectively as indicated in Figure 3.13; E_1, E_2, E_3 are errors introduced by the quantizers. Equation (3.8) reflects that the NTF contains three high-pass zeros on the unit circle, and all of the MASH architectures have only one pole lying on the crossing of the real and image axes in the z-domain, which does not change with the increasing order of the modulator. So theoretically speaking, the MASH modulators are unconditionally stable for any order.

The time domain output of this modulator, as shown in Figure 3.14, has 8 levels and spreads from −3 to 4 with an average value between 0 and 1. The logic output distribution shows that the central four levels (from −1 to 2) attract most power of the quantisation output; while the edge levels, −3 and 4, are rarely used. However, more output levels can provide further randomisation and produce relatively more continuous and smoother spectra. The stable input range normalised to the modulus is from 0 to 1, and it is inherently stable. The time domain logic outputs are measured as shown in Figure 3.15. The logic results were continuously recorded for 65536 samples by HP 16500C Logic Analysis System, and then converted to frequency domain using MATLAB. The phase error of this modulator is shown in Figure 3.16(a), which presents much better randomisation and the sequence repetition is effectively extended. The simulated and measured PSDs are compared in Figure 3.16(b) together with theoretical NTF derived in equation (3.8). It is clear that the two sets of signals match well without any cycle slip in time domain.

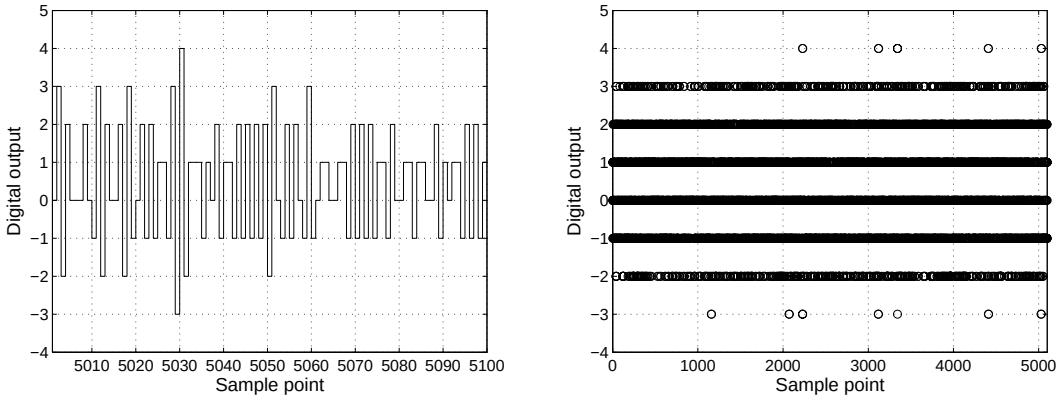


Figure 3.14 Time domain output and distribution of a MASH 1-1-1 Σ-Δ modulator.

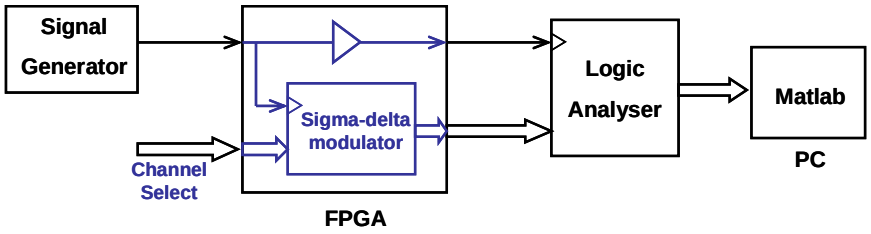
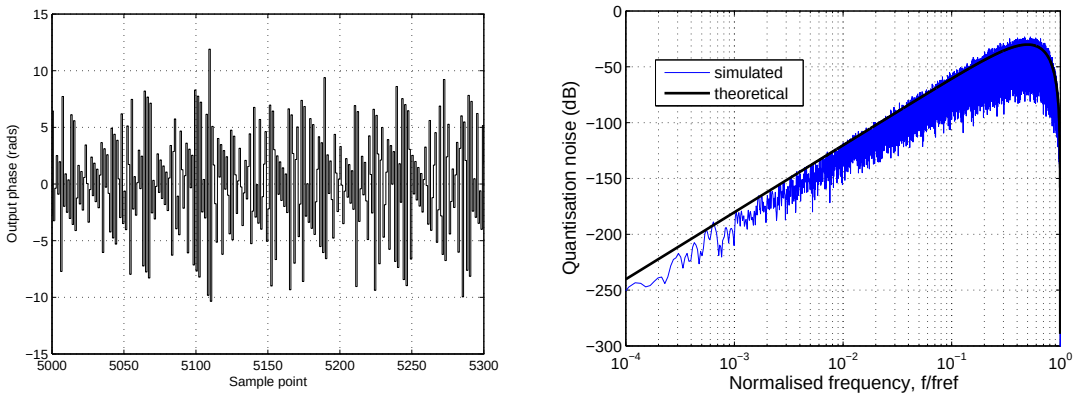


Figure 3.15 A setup for Σ-Δ modulator time domain output measurements.



(a) (b)

Figure 3.16 Phase error (a) and theoretical and simulated PSD (b) of the MASH 1-1-1 Σ-Δ modulator.

3.3.4 MASH 2-2

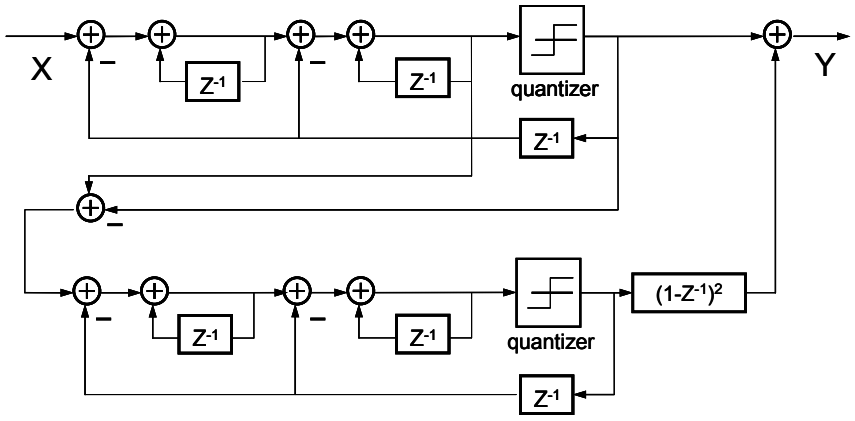


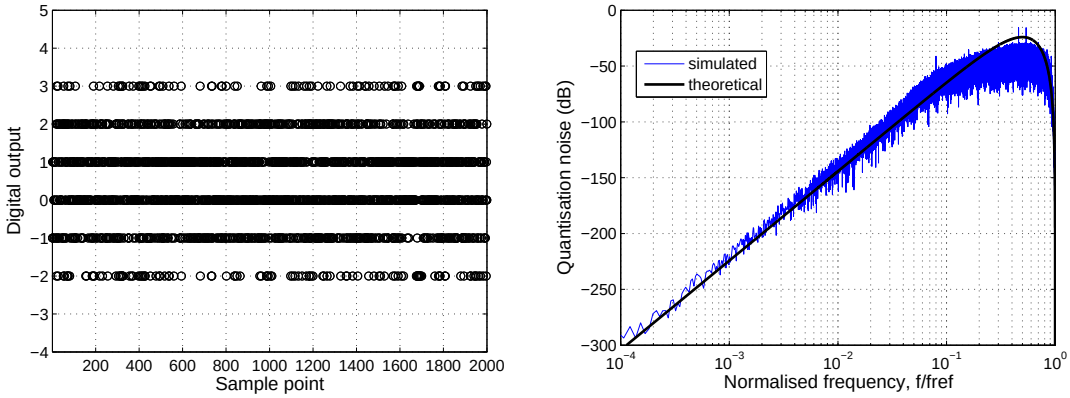
Figure 3.17 Block Diagram of a cascaded 2-2 MASH Σ-Δ modulator.

There are two conventional approaches to obtain satisfactory in-band noise performance for high resolution applications, either using high order Σ-Δ modulator architectures or increasing overs-ampling rates [66]. Limited by the delays and stability limitation of high order single stage Σ-Δ modulators, it is extremely difficult to design such a stable modulator at high sampling frequencies. MASH architectures are used as an applicable solution by cascading several first or second order Σ-Δ modulators together to achieve the desirable noise shaping and performance. The carry out bits of accumulators are delayed and added before generating a final multi-level output, so this pipelined architecture can cancel cascaded delays and achieve higher sampling frequencies. MASH 1-1-1-1 by cascading four first order Σ-Δ modulators [67-69] and MASH 2-2 by cascading two second order Σ-Δ modulators are two commonly used architectures with the same noise transfer function, which can be derived by using the same method described in equation (3.9).

$$NTF_2 = \left(1 - z^{-1}\right)^4 \tag{3.9}$$

The MASH 2-2 Σ-Δ modulator architecture is shown in Figure 3.17. Its first and second stages respectively consist of two second-order single-stage sections and a 1-bit quantizer in the feedforward path. The quantisation noise of the first stage is fed to the input of the second stage. The output is the sum of the double delayed version of the two second order Σ-Δ modulators. The time domain output of this modulator is shown

in Figure 3.18(a), and Figure 3.18(b) compares the theoretical and simulated PSDs as indicated in equation (3.9).



(a) (b)

Figure 3.18 Output distribution (a) and theoretical and simulated PSDs (b) of MASH 2-2 Σ-Δ modulator.

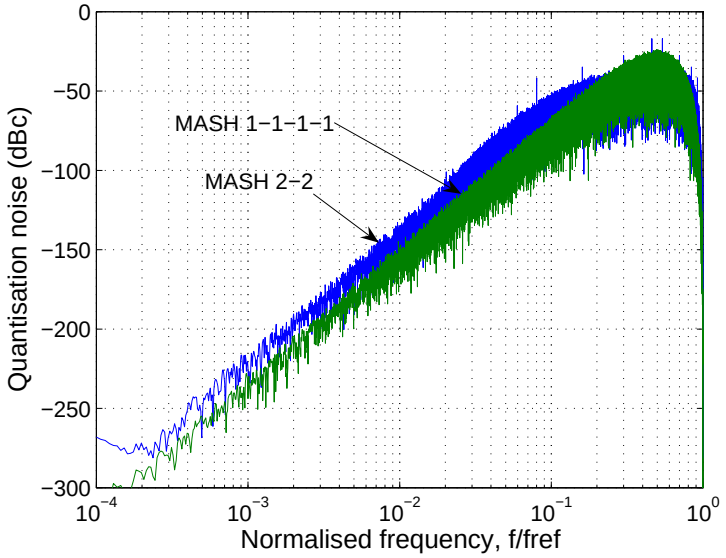


Figure 3.19 PSD comparison of MASH 2-2 and MASH 1-1-1-1 Σ-Δ modulators.

Figure 3.19 displays a PSD comparison of a MASH 2-2 and a MASH 1-1-1-1 Σ-Δ modulators. It is apparent that the close-in quantisation noise of MASH 2-2 is about 8 dB higher than that of MASH 1-1-1-1, which will substantially increase the in-band noise of the synthesisers. This is because that more output levels of MASH 1-1-1-1 provides better randomisation. However, the latter architecture also has its disadvantage of more output levels. MASH 2-2 has only 6-level output, which is much easier to implement rather than MASH 1-1-1-1 which spreads to 16-level output. In

addition, with the increment of the output levels, the stability margin of the system is limited [70].

3.3.5 Single-Stage Sigma-Delta Mdulators with Feedforward

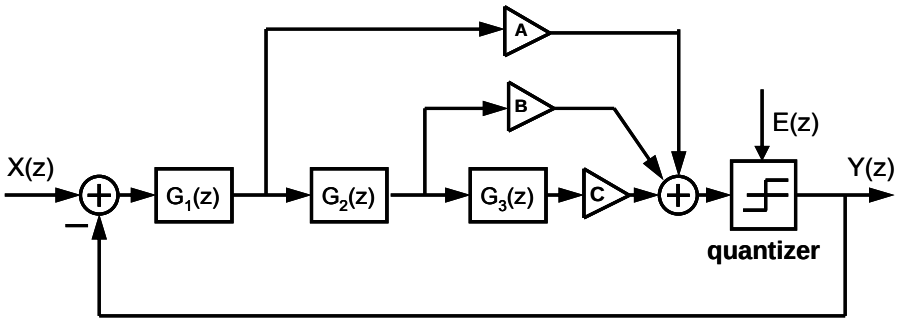


Figure 3.20 Block diagram of a third order Σ-Δ modulator with feedforward.

Compared with MASH Σ-Δ modulator architectures, the noise shaping of the single stage Σ-Δ modulator with feedforward is more flexible as it can be defined by some coefficients [56]. A common architecture of this kind of Σ-Δ modulators is shown in Figure 3.20; its performance is decided by the linear functions G_1, G_2, G_3 and coefficients A, B, C.

Two groups of commonly used transfer functions of G_1, G_2, and G_3 are listed in equations (3.10) and (3.11), which are used to achieve a high-pass Noise Transfer Function and a low-pass Signal Transfer Function, respectively.

$$G_1(z) = G_2(z) = G_3(z) = \frac{z^{-1}}{1-z^{-1}} \tag{3.10}$$

$$G_1(z) = \frac{z^{-1}}{1-z^{-1}};\ G_2(z) = G_3(z) = \frac{1}{1-z^{-1}} \tag{3.11}$$

In the z-domain, the Σ-Δ modulator output noted Y in Figure 3.20 can be expressed as a linear contribution of the small amplitude input X and the quantisation noise E.

$$Y(z) = H_{STF}\ X(z) + H_{NTF}\ E(z) \tag{3.12}$$

where H_{STF} is the signal transfer function defined by:

$$H_{STF} = \frac{Y(z)}{X(z)} = \frac{A \cdot G_1(z) + B \cdot G_1(z) \cdot G_2(z) + C \cdot G_1(z) \cdot G_2(z) \cdot G_3(z)}{1 - A \cdot G_1(z) - B \cdot G_1(z) \cdot G_2(z) - C \cdot G_1(z) \cdot G_2(z) \cdot G_3(z)} \tag{3.13}$$

and H_{NTF} is the Noise Transfer Function given by:

$$\begin{aligned} H_{NTF} &= \frac{Y(z)}{E(z)} \\ &= \frac{1}{1 - A \cdot G_1(z) - B \cdot G_1(z) \cdot G_2(z) - C \cdot G_1(z) \cdot G_2(z) \cdot G_3(z)} \\ &= \frac{\left(1 - z^{-1}\right)^3}{1 + C_1 \cdot z^{-1} + C_2 \cdot z^{-2} + C_3 \cdot z^{-3}} \end{aligned} \tag{3.14}$$

It is evident that the Σ-Δ modulator presents a low pass response to the input signal $X(z)$ and a high pass response to the quantisation noise $E(z)$, allowing the quantisation noise to be pushed to out-of-band, leaving low in-band noise. From the NTF, it can be easily found that the characteristic is a third order high pass function which has one zero lying on the real axis and three poles in the z-plane determined by the cut-off frequency. Butterworth and Chebyshev type II high-pass filter characteristic are two of best methods to achieve the high-pass function in Σ-Δ modulators, because both of them have relatively flat high frequency response. The Butterworth model is widely used because of its outstanding high pass response. However, they have similar high frequency responses when the cut-off frequency is lower than $0.2f_S$ in fractional-N frequency synthesisers.

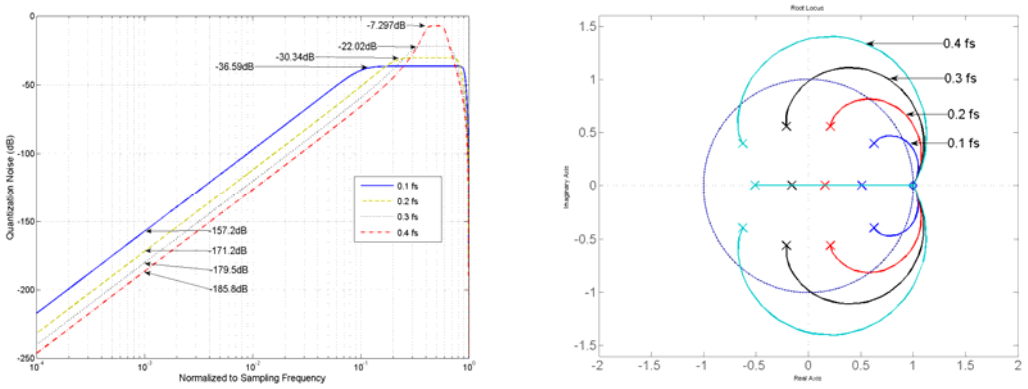


Figure 3.21 NTF and stability of Butterworth high pass topology.

Figure 3.21 shows the NTF derived by the Butterworth method at different cut-off frequencies and z-plane root locus plot, under the condition of $A = 2$, $B = 0.5$ and C is variable. With the increment of the cut-off frequency, three poles start from $z = 1$ in z-plane, and end at $z = -1$ when the cut-off frequency equals to 0.5, at which point the Σ-Δ modulator works under a critical condition: twice the Nyquist frequency. In fact, the Σ-Δ modulator will not work under this condition, because its root locus will lie completely outside of the unit cycle in the z-plane. The trade-off between in-band and out-of-band quantisation noise under different cut-off frequencies is indicated in Figure 3.21. The quantisation noise under $0.2f_S$ cut-off frequency at $10^{-3}f_S$ offset is 14 dB lower than that at $0.1f_S$, but the high frequency noise is 6.2 dB higher. The root locus is also shown in Figure 3.21, from which we can deduce that the poles are on the imaginary axis when the cut-off frequency is about $0.25f_S$. Normally, a cut-off frequency between $0.1f_S$ and $0.25f_S$ is chosen to obtain a balance between the oversampling rate and transient response in a Σ-Δ modulator.

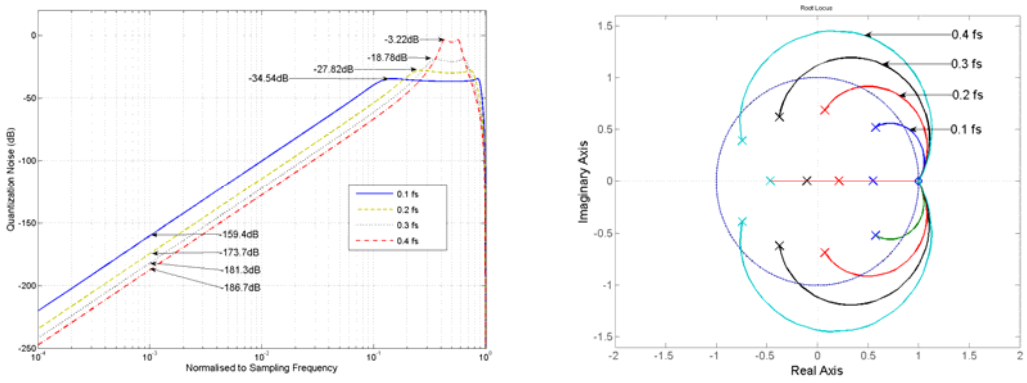


Figure 3.22 NTF and stability of Chebyshev type II high pass filter.

The Chebyshev type II filter is another high-pass function widely used in Σ-Δ modulators, which presents ripples in gain at stopband. Figure 3.22 shows the NTFs at different cut-off frequencies and their root locus. Its high-pass performance is quite similar to the Butterworth function in the frequency domain relevant to fraction-*N* frequency synthesisers. Compared with Figure 3.21, the theoretical quantisation noise shows that the high frequency noise is about 2 dB higher, meanwhile the in-band noise is 2 dB lower at the same cut-off frequency. Figure 3.23 presents a comparison of PSDs of Σ-Δ modulators based on Butterworth and Chebyshev type II high pass theories respectively. The theoretical plots are according to equation (3.14), under the condition

of $A = 2$, $B = 0.5$, $C = 1$. The quantisation noise at high frequency offsets is higher in Chebyshev type II modulators than that of Butterworth Σ-Δ modulators.

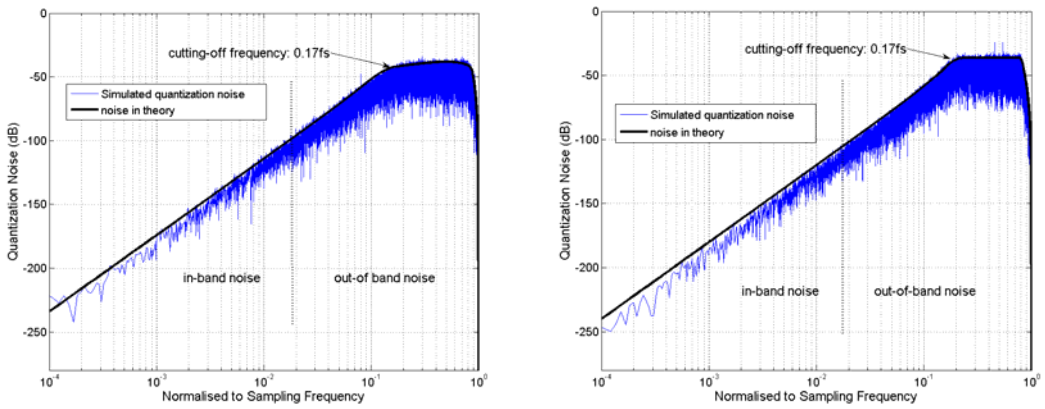


Figure 3.23 PSDs of Σ-Δ modulators based on Butterworth (left) and Chebyshev type II (right) high pass theories with the same cut-off frequency of 0.17*fs*.

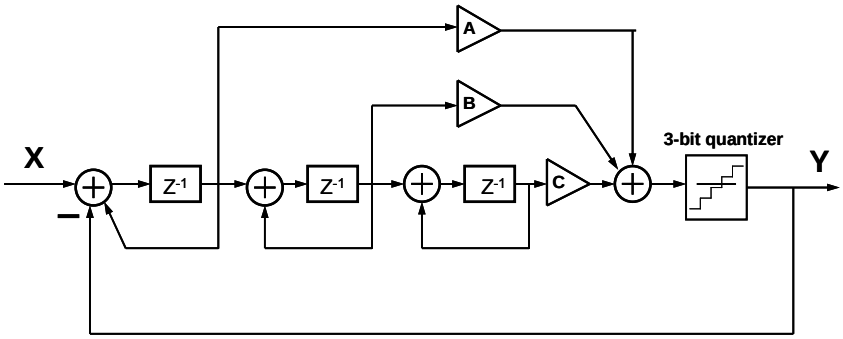


Figure 3.24 An implemented third order feedforward Σ-Δ modulators based on Butterworth characteristic.

A typical third order single stage Σ-Δ modulator is shown in Figure 3.24. For the same order, single-stage Σ-Δ modulators have even better overall noise shaping than the MASH architecture by choosing proper feedforward coefficients as discussed previously. If the cut-off frequency of the high pass filter is $0.17f_S$, the coefficients are {0.9627, 0.5627, 0.1003}, leading to the NTF:

$$NTF_3 = \frac{\left(1-z^{-1}\right)^3}{1-0.9627z^{-1}+0.5627z^{-2}-0.1003z^{-3}} \tag{3.15}$$

To avoid digital multiplication, the coefficients in the denominator are approximated in a real-time implementation such that the noise shaping can be achieved by shifting

operations. The modified NTF is given in equation (3.16) , which maintains high pass and good stability. Its root locus together with poles are shown in Figure 3.25.

$$NTF_3' = \frac{\left(1-z^{-1}\right)^3}{1-z^{-1}+0.5z^{-2}-0.1z^{-3}} \tag{3.16}$$

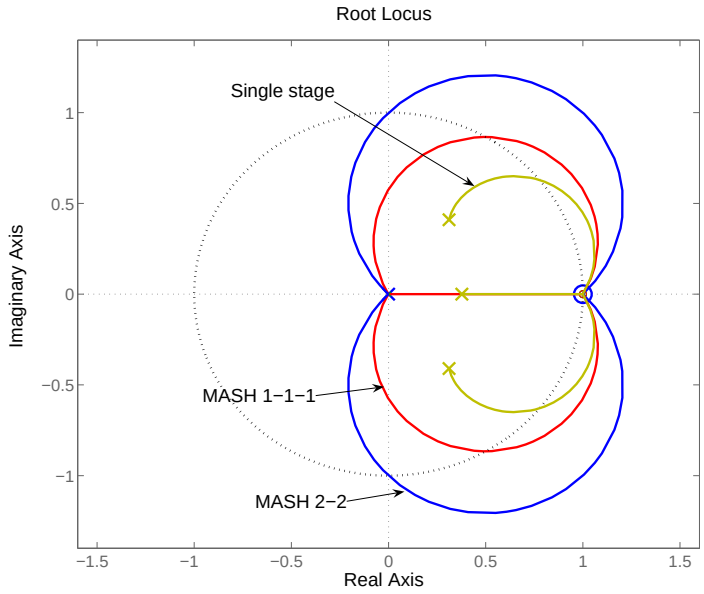


Figure 3.25 Root locus and poles of the NTF.

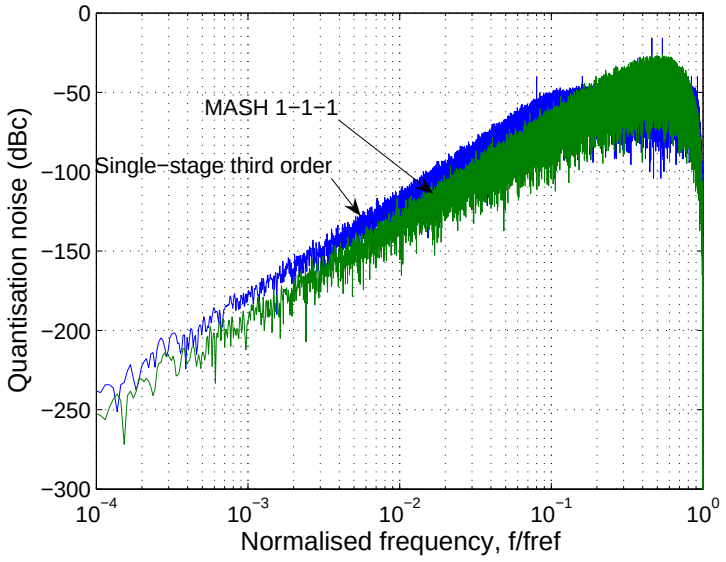


Figure 3.26 PSD comparison of MASH 1-1-1 and single stage Σ-Δ modulators.

In contract to MASH, the stability analysis of the single stage architectures is slightly more complex. From the NTF in equation (3.16) it is easy to get positions of three poles: 0.382, 0.311 ± 0.41*i*, which move slightly from the poles determined in equation (3.15): 0.2568, 0.335 ± 0.5277*i*. However, the modified NTF does not deteriorate its stability or change its transient response.

Figure 3.26 shows a PSD comparison of MASH 1-1-1 and third order single stage Σ-Δ modulators, from which it can be seen that the in-band noise of the MASH architecture is about 7 dB lower than that of the single stage architecture. Meanwhile, its high frequency noise is much higher than the latter one. As a result, the out-of-band phase noise of the frequency synthesiser output is not able to be ideally suppressed.

3.3.6 Single-Stage Sigma-Delta Modulators with Feedback

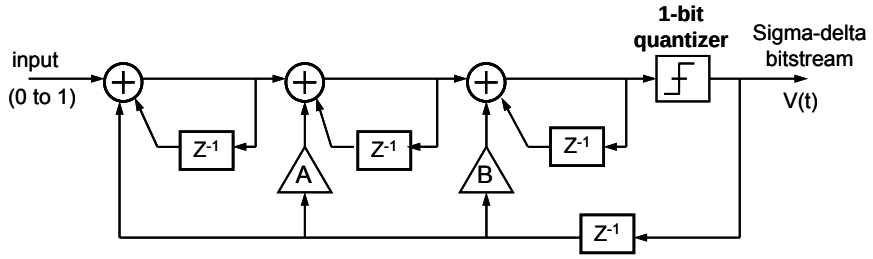


Figure 3.27 A typical third-order single-bit feedback Σ-Δ modulator.

Figure 3.27 shows a block diagram of a typical third order single-stage Σ-Δ modulator with feedback paths. The STF and NTF of the Σ-Δ modulator can be derived by Mason's rule [70] as:

$$\begin{aligned} H_{NTF}(z) &= \frac{1}{1-\frac{1}{z}\left[-\frac{Bz}{z-1}-A\left(\frac{z}{z-1}\right)^2-\left(\frac{z}{z-1}\right)^3\right]} \\ &= \frac{1}{1+\frac{B}{z-1}+A\frac{z}{(z-1)^2}+\frac{z^2}{(z-1)^3}} \\ &= \frac{(1-z^{-1})^3}{1+(A+B-2)z^{-1}-(A+2B-3)z^{-2}+(B-1)z^{-3}} \end{aligned} \tag{3.17}$$

$$H_{STF}(z) = \frac{z^{-3}}{1+(A+B-2)z^{-1}-(A+2B-3)z^{-2}+(B-1)z^{-3}} \tag{3.18}$$

where $z = e^{j\omega T_{ref}} = e^{j2\pi f / f_{ref}}$.

The frequency domain signal transfer function and noise transfer function are shown in Figure 3.28 under the assumption of $A = -8$, $B = -16$. It is clear that the signal transfer function presents a low-pass frequency response whilst the noise transfer function is a high-pass response.

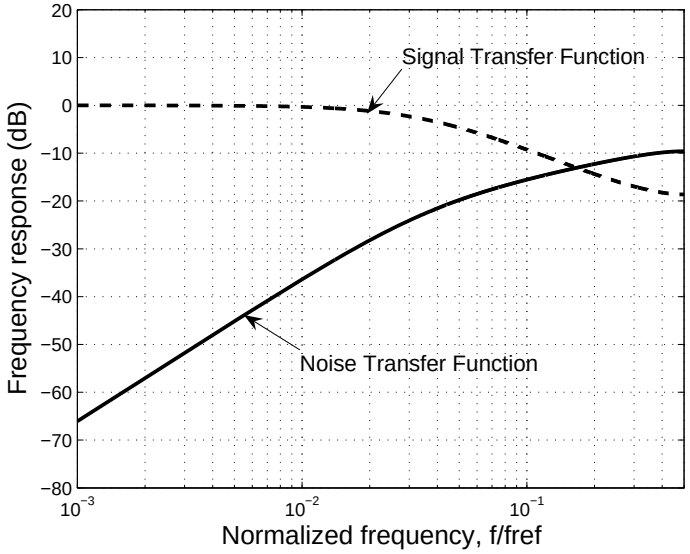


Figure 3.28 Modelled frequency response of signal transfer function and noise transfer function of the third order single-bit Σ-Δ modulator.

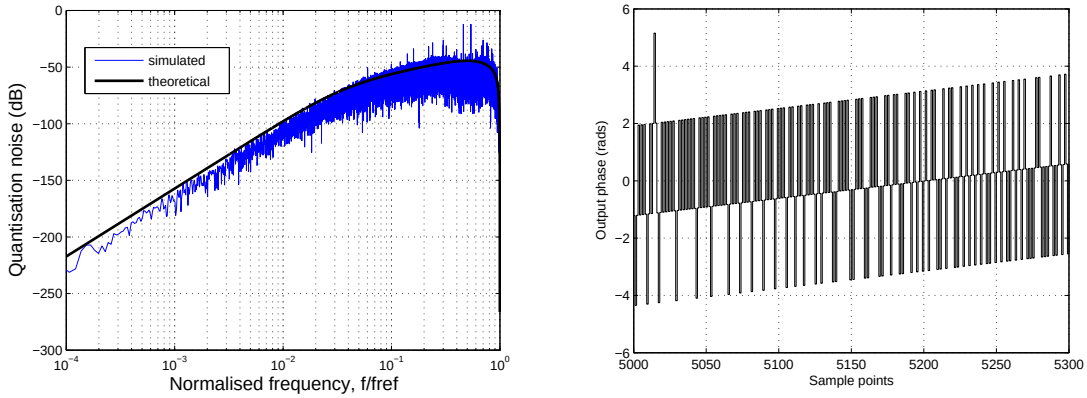


Figure 3.29 PSD and phase error of the third order single stage modulator.

A and *B* are negative feedback coefficients. Setting *A* and *B* equal to −1 gives a high pass characteristic of 40 dB/decade, which forms a simple third order architecture, although it leads to more negative feedback and less noise suppression. Stability analysis of this topology is generally complicated due to the quantizer presence [71], although simulation can be used to obtain the best noise suppression consistent with stable operation. The noise shaping and phase error for $A = -8$ and $B = -16$ are shown in Figure 3.29, in which the theoretical characteristic is plotted according to equation (3.17). It is apparent that there is a series of discrete spurs presenting at high frequencies. These spurs can be suppressed by the PLL closed-loop response.

Table 3.1 Performance Comparison of Σ-Δ modulators.

ARCHITECTURE	SAMPLING FREQUENCY	STABLE INPUR RANGE	NOISE SHAPING RATE	SPURS
MASH 1-1-1	176.900 MHz	0 − 1	−60 dB/decade	Free
MASH 2-2	109.430 MHz	0.09 − 0.91	−80 dB/decade	Free
Single-Stage Feedforward	98.870 MHz	0.12 − 0.88	−60 dB/decade	Many
Single-Stage Feedback	85.210 MHz	0.15 − 0.85	−60 dB/decade	Many

A comparison of commonly used third and fourth order Σ-Δ modulators is shown in Table 3.1. The indicated sampling frequencies are measured results by the same FPGA XC2V1500 real time implementation which will be presented in chapter 4, and the stable input range is simulated by MATLAB. A series of simulation results show that MASH modulators have wider stable input range, and single-stage architectures fall into instabilities at the input boundaries of 0 and 1. Finally, on specific channels, single-stage modulators will present spurious components on the quantisation noise spectra. This problem will be analysed in the following chapters.

3.4 Modelling Synthesiser Phase Noise

3.4.1 Noise Sources

The phase noise of frequency synthesisers is a key figure of merit in RF communications system designs. Higher than desired phase noise (Figure 1.1) can cause degraded system performance in terms of reducing the signal to noise ratio (SNR), increasing adjacent channel power, and reducing adjacent channel rejection. From a design perspective, the quantities of interest are the spectral properties of the output noise and the RMS phase error. $L(f_m)$ is defined as the ratio of the single sideband (SSB) power of phase noise in a 1 Hz bandwidth f_m hertz away from the carrier frequency to the total signal power.

The fractional-*N* noise analyses are based on a series of assumptions. First of all, the synthesiser/PLL is assumped to be in lock, in order to avoid unstable PFD phase error occurred in unlocked loops. Secondly, all the noise sources in the loop are uncorrelated. Based on these conditions, the phase noise due to the individual blocks of a fractional-*N* synthesiser is added, to give an overall two-sided phase noise profile:

$$L_{\phi}(f_m) = L_{\phi_{VCO}}(f_m) + L_{\phi_{SDM}}(f_m) + L_{\phi_{filter}}(f_m) + L_{\phi_{PFD}}(f_m) \tag{3.19}$$

The modified Leeson equation [72], stated in equation (3.19) expresses the output phase noise PSD of the VCO. The overall RMS phase error can be determined from a given synthesiser's phase noise profile by integrating the SSB phase noise profile across a specified frequency offset, f_1 to f_2:

$$\phi_{rms}^2 = 2\int_{f_1}^{f_2} L_{\phi}(f_m)df_m \tag{3.20}$$

A. VCO Noise

Leeson's oscillator model [72] consists of an amplifier with a gain of $A(s)$ at the output stage and a resonator with a gain of $R(s)$ in the positive feedback path. So the transfer function of this feedback loop is

$$\frac{v_o(s)}{v_i(s)} = \frac{A(s)}{1 - A(s)R(s)} \tag{3.21}$$

If this feedback loop oscillates at a frequency f_o, $A(s)R(s) = 1$ and the phase shift around the complete loop is 2π.

The VCO phase noise appears at the output of the fractional-N synthesiser as [44]

$$L_{\phi_{VCO}}(f_m) = \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{F_{out}}{2Q_L}\right)^2\right]\frac{FkT}{Ps}\left(1 + \frac{f_c}{f_m}\right) \tag{3.22}$$

where k is Boltzmann constant, T is temperature, P_S is average power dissipated in the resistive part of the tank, Q_L is loaded Q of VCO, f_m is frequency offset from carrier, F_{out} is oscillator carrier frequency, f_c is the flicker noise corner frequency, and F is device noise factor of the VCO operating at power level P_S. The noise factor is a ratio of the noise produced by a real VCO to the simple thermal noise of an ideal VCO.

B. Loop Filter Noise

Besides the closed-loop response of the filter, components such as resistors and op-amps introduce some extra noise. Op-amp noise is derived experimentally or given by the manufacturer. The noise model available for a resistor is assumed to be thermal noise and is defined by equation (3.24) which shows the noise valtage in the resistor. The filter phase noise contribution is:

$$L_{\phi_{filter}}(f_m) = 10\log\frac{V_n^2 N^2}{K_P^2} \tag{3.23}$$

The noise voltage V_{n} introduced by resistors and op-amps is:

$$V_n = \sqrt{4kTBR} \tag{3.24}$$

where k is the Boltzmann constant, T is the absolute temperature, B is the Bandwidth of the filter and R is the resistor value.

C. Phase/Frequency Detector Noise

Thermal and sources of noise of the PFD result in timing jitter on both rising and falling edges of the PFD output pulses [73]. This jitter may be considered equivalent to a certain input timing jitter of Δt seconds RMS on the reference input of an ideal, noise free PFD. Depending upon the PFD design, one or other of the edges of each incoming waveform independently triggers each input device allowing phase comparison. The time difference between these edges is translated to the required current pulse duration at the charge pump output, which is necessary to maintain phase lock [73, 74]. Thus, each PFD timing jitter is translated to an equivalent phase jitter on the VCO output, elevating its phase noise floor. For a PFD with an operating frequency of f_{ref}, the equivalent phase jitter is:

$$\Delta\phi_{in} = 2\pi f_{ref} \Delta t \tag{3.25}$$

In practice, Δt is very small − with the order of pico-seconds − whilst the noise occupies a bandwidth much greater than the PFD sampling frequency. The PFD, being an edge triggered sampling device with an output pulse train of very low duty cycle in a locked loop, is a good approximation to an impulse sampler possessing an equivalent noise bandwidth of half the sampling frequency and virtually uniform spectral density of translated components over this frequency range [75]. Hence, the equivalent input double-sided spectral density of phase fluctuations is:

$$S\phi_{in}(f_m) = \frac{(\Delta\phi_{in})^2}{f_{ref}/2} = 8\pi^2 f_{ref} \Delta t^2 \tag{3.26}$$

This indicates a 10 dB/decade increase in the PFD noise output with the phase detector operating frequency, of f_s. For a typical phase locked synthesiser with only a divider feedback path, the resultant output phase noise spectral density is subject to a gain

equivalent to the divider ratio gain $N = f_o / f_s$, where f_o is the output frequency of the synthesiser. The value of N can be either integer or fractional. Therefore, it follows that,

$$S\phi_{out}(f_m) = 8\pi^2 f_{ref}\, \Delta t^2\, N^2 = \frac{8\pi^2\, \Delta t^2\, f_{out}^2}{f_{ref}} \tag{3.27}$$

This now indicates an overall 10 dB/decade decrease in output phase noise with the phase detector operating frequency of f_{ref}. Assuming the overall output phase noise is smaller than 0.1 radians, then from [76], the output SSB phase noise power, $L(f_m)$, is equal to one half of the double-sideband power spectral density of phase fluctuations;

$$L(f_m) = \frac{1}{2} S\phi_{out}(f_m) = 10\,\mathrm{Log}_{10}\left(\frac{4\pi^2\, \Delta t^2\, f_{out}^2}{f_{ref}}\right) \tag{3.28}$$

D. Frequency Divider and Reference Frequency

Equation (3.28) also reveals the realtionship between reference frequency and overall phase noise, which was stated by Banerjee [77]. The noise contribution from the digital components in the PLL can be summarised into the 1 Hz normalisd Phase Noise Floor, $L(f_m)$, which can be determined from a direct measurement. The in-band phase noise of the fractional-N synthesiser can be determined by:

$$L_{in-band}(f_m) = L(f_m) + 20\log_{10} N + 10\log_{10} f_{ref} \tag{3.29}$$

where N is the division ratio and f_{ref} is the reference frequency. Substituting $N = \frac{f_{out}}{f_{ref}}$ into equation (3.29) gives

$$L_{in-band}(f_m) = L(f_m) + 20\log_{10} f_{out} - 10\log_{10} f_{ref} \tag{3.30}$$

From equation (3.30) it can be easily seen that the phase noise floor of the synthesiser will be further suppressed by employing higher reference frequencies at a rate of

10 dB/decade. For example, if a 100 MHz reference frequency is used in the fractional-*N* synthesiser to replace the 13 MHz reference frequency used before, the in-band phase noise will decline by

$$D = 10\log_{10}\frac{100MHz}{13MHz} = 10\log_{10}7.69 = 8.86dB \tag{3.31}$$

It is evident that higher reference frequencies enable the use of lower prescaler ratios, with a resultant reduction in the multiplied PFD and reference noise, and thus the ability to achieve wide fractional operating bandwidths. However, the speed of Σ-Δ modulators becomes the greatest challenge. Few design of high frequency (> 50 MHz) modulator used in fractional-*N* frequency synthesisers has been reported due to the bottleneck of low operating frequency, which can be overcome by using the stored-sequence technique.

3.4.2 ADS Noise Model

A circuit level phase-locked loop model has been built in the Hewlett Packard advanced design system (ADS), as shown in Figure 3.30. This model comprises a PLL based on a third-order type II loop, a 100 MHz reference frequency and a fixed divider with a division ratio of 8.5. The model is used to predict loop response and noise performance of a high reference frequency integer-*N* synthesiser. Σ-Δ modulation and quantisation noise are not considered in this model.

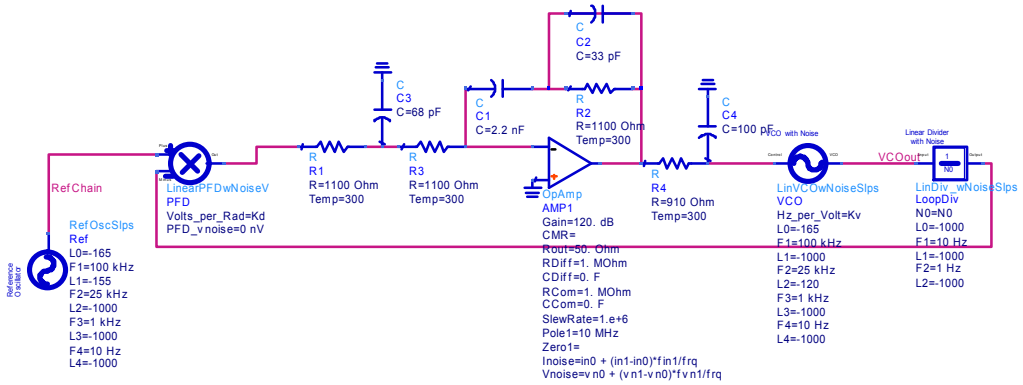


Figure 3.30 A HP ADS model of a third-order type II phase-locked loop.

The noise contributions from every component in the loop are simulated, the results of which are shown in Figure 3.31. It uses linear, small signal models for each of these loop components. Also, the contribution of each noise source to the total VCO phase noise is uncorrelated, and the phase noise contributions are computed by RMS integrating the SSB phase noise. The loop filter in the system is an active third-order architecture, with an additional noise suppression pole (C_4 and R_4) at 500 kHz offset to further suppress high frequency noise. The op-amp specifications are set according to an AD8031 which is used in the synthesiser design. In Figure 3.31, the simulated VCO output phase noise shows that the in-band phase noise is around −120 dBc/Hz and the cut-off frequency is about 250 kHz. It is apparent that in an ideal PLL, the in-band noise is mainly decided by the loop response and the component noise, which means that low frequency offset performance of a free-running VCO does not affect the in-band phase noise. The simulated out-of-band noise is a combination of loop response, PFD and the component noise in the loop filter. This prediction is valid for all the integer-*N* synthesisers. In fractional-*N* designs, the out-of-band noise is normally dominated by the digital control part, i.e. the Σ-Δ modulator.

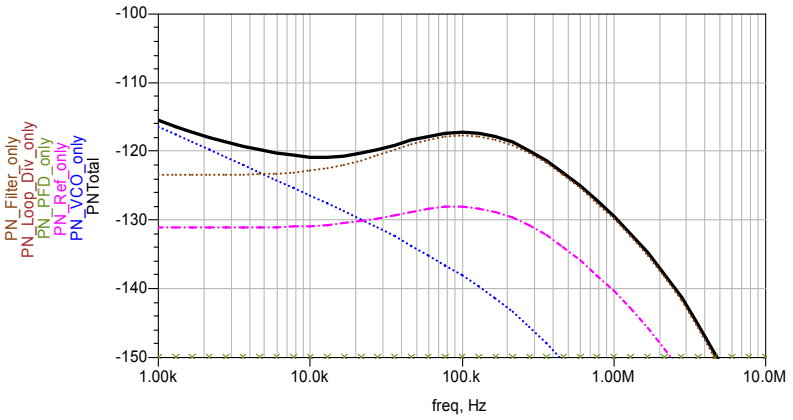


Figure 3.31 Contributions to VCO phase noise in an integer-*N* synthesiser.

Figure 3.32 shows further analysis of the VCO noise in a closed loop. The low frequency offset (≤ 1 kHz) phase noise is suppressed to a lower level than a free-running VCO phase noise. This is caused by the low pass response of the PLL. At higher frequency offsets, the VCO output phase noise is directly shaped by the closed

loop response of the PLL, and its noise level is higher than the VCO free-running noise, due to the contribution from the components in the loop.

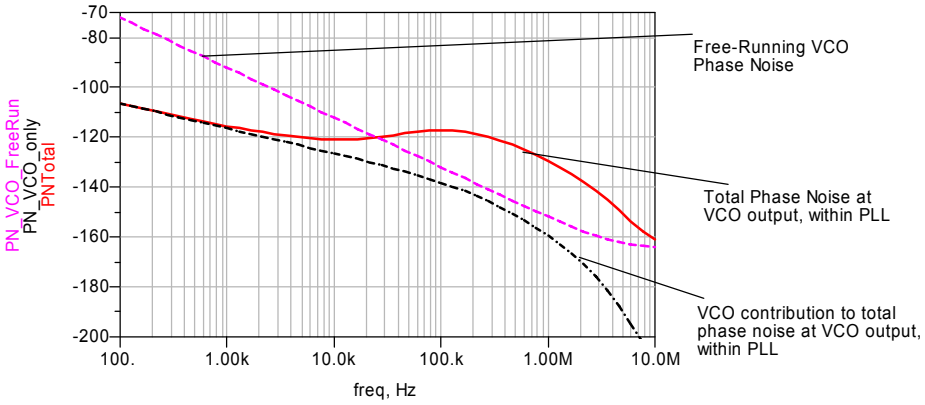


Figure 3.32 Loop reduction of VCO phase noise.

3.4.3 Matlab Noise Model

A Matlab noise model has been developed to predict and analyse phase noise and switching time of synthesisers. An typical integer-*N* synthesiser widely used in GSM base stations as shown in Figure 2.7 is initially modelled. This synthesiser consists of a third-order type II loop filter, whose bandwidth is set to 20 kHz which is a normally used value to suppress fractional spurs at *N* times 200 kHz frequency offsets. Figure 3.33 displays the modelled synthesiser output phase noise and the component contributions (Appendix B.3). It is apparent that the in-band phase noise of the VCO output is dominated by PFD and the component noise, and the out-of-band noise is dictated by the VCO free-running noise. The modelled switching time of this synthesiser is shown in Figure 3.34. This switching time is modelled by a MATLAB built-in function *LSIM* which uses a loop to predict time response of a model to input signals according to a closed loop response function as shown in Equation (2.29). It is obvious that this narrow bandwidth PLL requires longer than 100 μs to lock-in, which is significant longer than the guard time (30.5 μs) between two channels in GSM systems. Hence, every single GSM base station employs two separate integer-*N* synthesisers combined in a "ping-pong" synthesiser arrangement for local oscillator functions, which reduces the efficiency and significantly raises the cost.

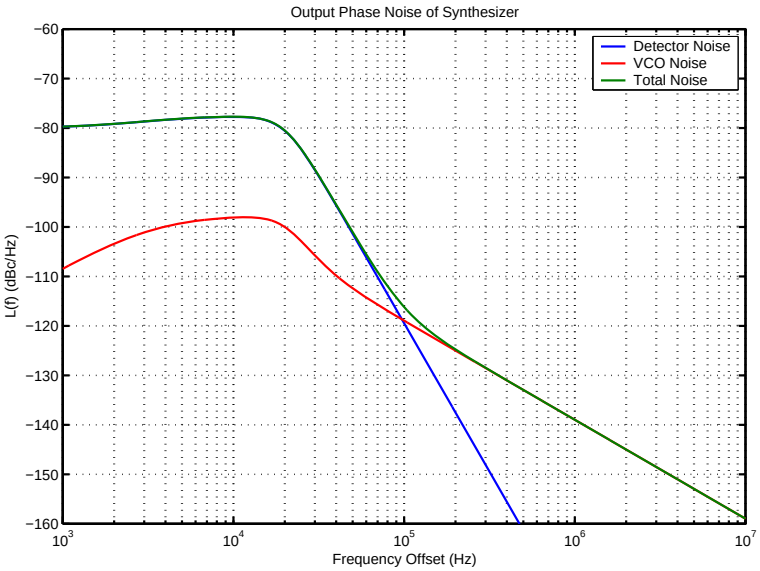


Figure 3.33 Modelled integer-*N* synthesiser phase noise.

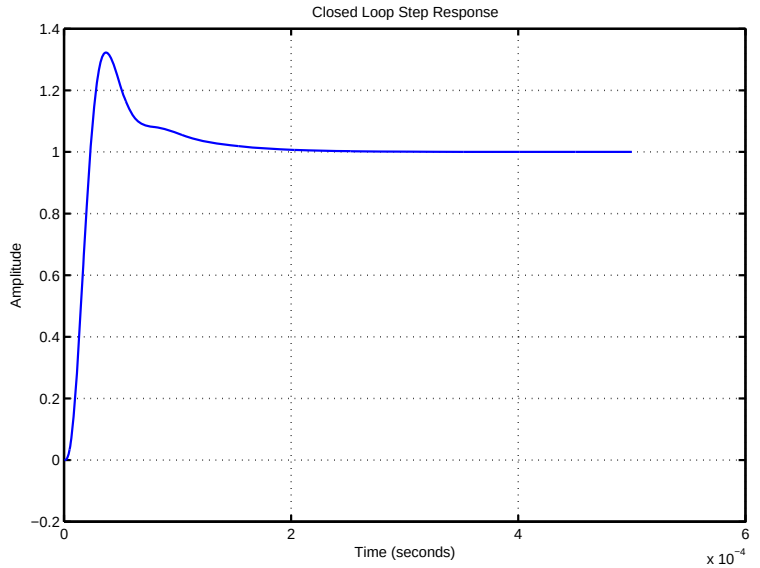


Figure 3.34 Modelled integer-*N* synthesiser switching time.

To replace the "ping-pong" synthesiser, a typical fractional-*N* architecture commonly used in cellular applications is modelled, with the bandwidth extended to 250 kHz. The wider bandwidth allows the synthesiser to switch faster to a new frequency. A 13 MHz reference frequency is chosen to be consistent with mobile applications so that similar techniques, especially the Σ-Δ modulator, can be used to conveniently control the division ratio and the output frequency. A third order MASH modulator is employed to suppress close-in noise in this model. The modelled phase noise is presented in Figure 3.35, which is based on a fractional-*N* synthesiser as shown in Figure 3.3. The in-band phase noise at 100 kHz offset is −94 dBc/Hz which is also influenced by the

PLL response and PFD component noise. The phase noise between 100 kHz and 700 kHz offset is a combination of quantisation noise and PLL response. At higher frequency offsets, the synthesiser output phase noise is dominated by the quantisation noise of the Σ-Δ modulator. The modelled result also shows that the overall phase noise is much larger than the integer-*N* synthesiser phase noise at frequency offsets higher than 40 kHz, which fails to meet the GSM base station specifications.

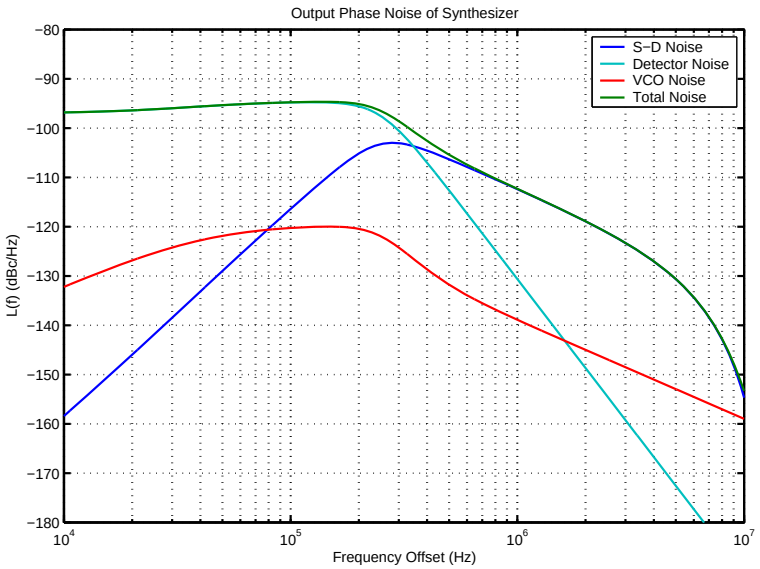


Figure 3.35 Modelled fractional-*N* synthesiser phase noise, with 13 MHz reference frequency.

A direct method of suppressing the overall phase noise of Σ-Δ fractional-*N* synthesisers is to reduce the division ratio by using a high reference frequency. The largest difficulty of applying this method is the requirment of fast sampling speed in the Σ-Δ modulator, which is a real challenge as no Σ-Δ modulator with higher than 80 MHz sampling frequency has been reported. However, it is feasible, in theory, without introducing extra circuitry to get better noise performance. Figure 3.36 presents the modelled results of a fractional-*N* synthesiser with 100 MHz reference frequency. All of the components and noise are set exactly the same as the real synthesiser design with 13 MHz reference frequency as shown in section 4.4. The in-band noise of this synthesiser is now −113 dBc/Hz, about 9 dB lower than that shown in Figure 3.35. The impact of quantisation noise of the Σ-Δ modulator is alleviated in such a high reference frequency synthesiser. However, if a single-stage Σ-Δ modulator is used, it may affect the phase noise at high frequency offsets due to its large quantisation noise, as illustrated in Figure 3.26. The modelled switching time of this synthesiser is about

10 μs, which can meet the requirement of fast switching applications, such as GSM and DCS. The in-band phase noise of the fractional-*N* synthesiser is 33 dB lower than the integer-*N* synthesiser displayed in Figure 3.33. However, its phase noise between 100 kHz and 500 kHz frequency offsets is higher than the integer-*N* synthesiser. Benefiting from the wider bandwidth, its switching time (10 μs) is much shorter than the integer-N synthesiser (100 μs).

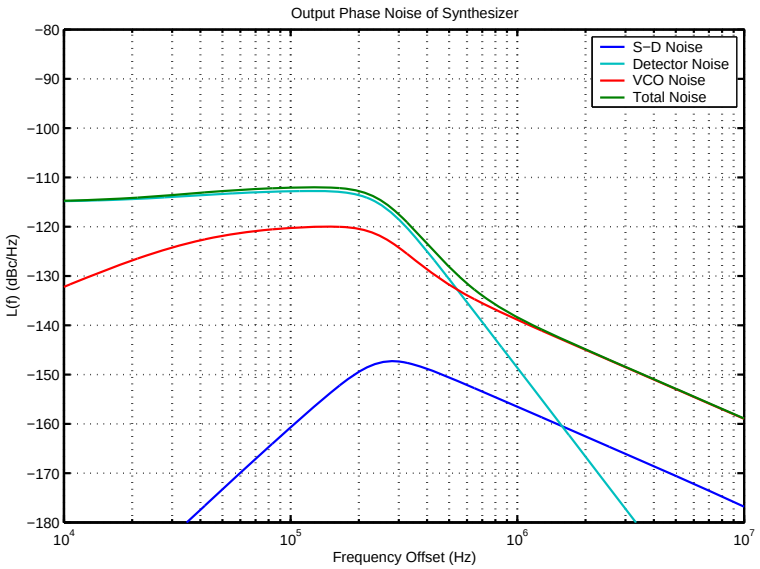


Figure 3.36 Modelled fractional-*N* synthesiser phase noise, with 100 MHz reference frequency.

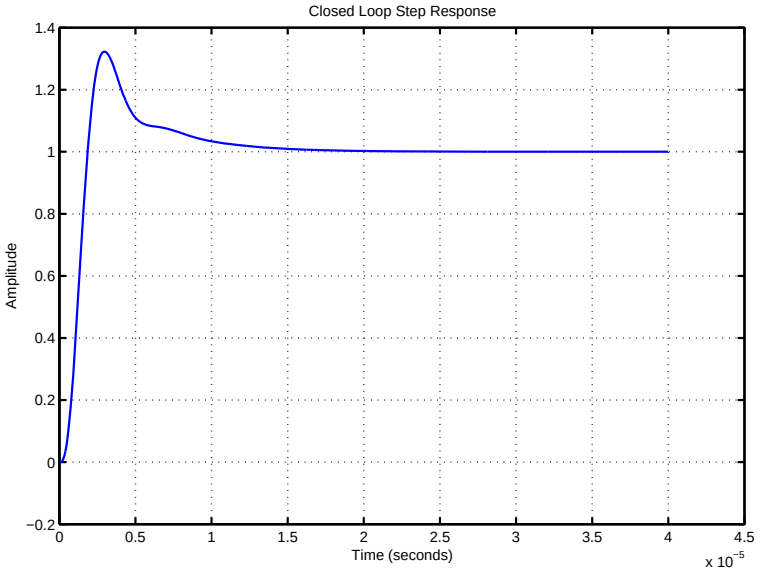


Figure 3.37 Modelled fractional-*N* synthesiser switching time.

3.5 Summary

This section has introduced Σ-Δ modulation of a fractional-*N* synthesiser based on a combination of a multi-modulus frequency divider and a Σ-Δ modulator. Some popular Σ-Δ modulator topologies are analysed in detail with emphasis on noise shaping which determines the noise performance of the synthesiser. To cover all the channels in mobile systems, unconditionally stable modulator topologies are mandatory in frequency synthesis. These include first, second and third order modulators as well as cascaded MASH architectures. Low order modulators have the disadvantage of poor noise shaping, whilst high order topologies tend to suffer from cascaded delays.

Two noise models are presented to predict overall phase noise and tuning time of the synthesiser. The modelled results show that a high reference frequency design can effectively suppress phase noise based on a basic fractional-*N* synthesiser. However, Σ-Δ modulators are difficult to fabricate at high operating frequencies due to the limited speed of the digital data path elements. In particular the resolution of the adders and multipliers increases the delay as a result of the combinational logic complexity. A proposed way of overcoming these limitations is to use a fast stored-sequence component to replace the Σ-Δ modulator, thus generate an ideal noise shaping and control the multi-modulus frequency division.

Chapter 4

Novel Synthesiser Designs and Measured Results

This chapter presents design considerations and procedures used to develop prototype synthesiser systems in this work. The main objective of building the prototype synthesisers is to provide hardware verification of innovative low noise, fast settling fractional-*N* synthesisers as a low cost solution which can be used in GSM and DCS base stations replacing the complicated integer "ping-pong" synthesisers. A new technique of implementing multi-modulus frequency dividers is presented in detail, as an alternative solution in fractional-*N* frequency synthesis. This memory-controlled divider can be achieved by using a single FPGA which also integrates a high sampling frequency Σ-Δ modulator.

Two fractional-*N* synthesiser prototypes were successfully developed using FPGA based Σ-Δ modulators and external frequency divider, phase/frequency detector, loop filter and VCO. A 12.8 MHz crystal oscillator and a 100 MHz signal were used as the reference sources in two prototypes respectively.

4.1 Design Considerations

4.1.1 Frequency Synthesisers in Cellular Communication Systems

The Global System for Mobile communications (GSM) is the most popular cellular standard in the second generation wireless communications. It has approximately 60% of the cellular subscribers in the world with primary service of voice transmission and internet access. In the third generation wireless communications, GSM has evolved into Wideband Code Division Multiple Access (WCDMA) standard which provides greater bandwidth for voice, video and data transmission. Some of the specifications for

frequency synthesiser design in popular cellular telephony systems are listed in Table 4.1. A dual mode transceiver that incorporates both standards with smooth migration and backward compatibility, therefore, becomes very necessary. A typical transceiver arrangement is shown in Figure 4.1. Frequency synthesisers are widely used in wireless transceivers to provide precise and fine-tunable local oscillator frequencies. In the multi-standard frequency synthesiser design, hardware sharing is an important issue that mandates maximum component reusability between the two modes for low cost and power consumption.

Table 4.1 Specifications for popular cellular telephony systems.

STANDARD	TECHNOLOGY	BANDWIDTH	FREQUENCY BAND (MHZ)
GSM-900	TDMA	200 kHz	890–915 (Tx) 935–960 (Rx)
DCS-1800	TDMA	200 kHz	1710–1785 (Tx) 1805–1880 (Rx)
CDMA2000	CDMA	1.2288 MHz	flexible
UMTS	W-CDMA	5 MHz	1920–1980 (Tx) 2110–2170 (Rx)

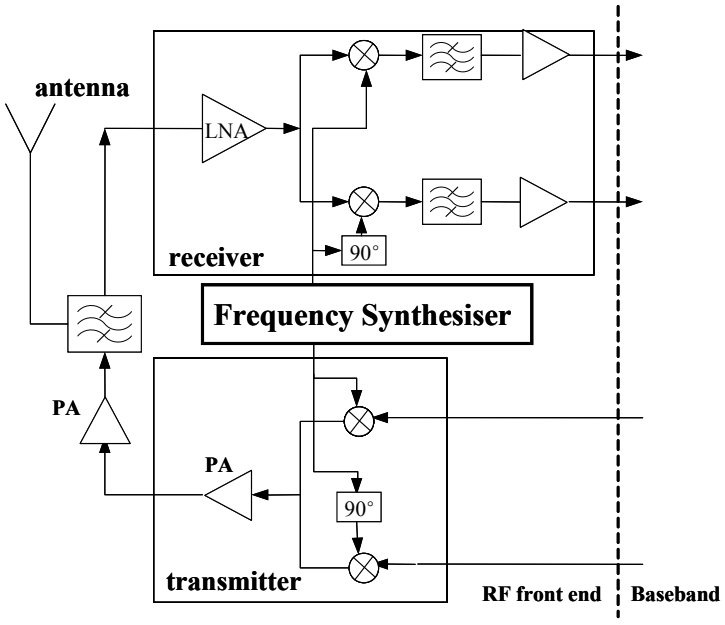


Figure 4.1 A general arrangement of GSM transceivers.

4.1.2 Synthesiser Requirements in Base Stations

In a frequency synthesiser, the VCO is a critical component for achieving low phase noise. The phase noise PSD of a resonator based VCO can be shown to be inversely proportional to the square of the quality factor (Q) of the resonator [l]. LC resonators integrated on silicon IC substrates typically have much lower Qs than those using external discrete components; thus, this often makes their noise performance unacceptable for base stations because of their critical requirement for low phase noise. The proximity of PLL blocks to each other internally on a fully integrated synthesiser solution causes undesired coupling of unwanted components onto the output spectrum. These spurious components degrade the signal to noise ratio and make it difficult to meet regulatory standards at high power. An external VCO will provide significant isolation between the PLL dividers and the VCO output, resulting in significantly cleaner output spectra. Secondly, limited by its die area in integrated circuits, the capacitance of an integrated loop filter becomes the bottleneck of PLL response and noise suppression. These reasons result in discrete implementation of frequency synthesisers in GSM/DCS base stations, rather than low cost monolithic circuits as in handsets.

Switching speed of the synthesiser is also a stringent requirement in a GSM/DCS transceiver used in a base station. In the worst case, the synthesiser needs to switch between two channels in 30.5 μs. RF system designers of time division multiple access (TDMA) based cellular systems need local oscillator frequency synthesiser blocks capable of tuning to a new channel within a small fraction of each time slot. Base stations and data transmission applications are now striving to utilise all the time slots available in each frame using a single frequency synthesiser. This push towards a "zero blind slot" solution has put stringent demands upon the radio front end LO section. For high-data-rate standards, high-speed circuit-switching data (HSCSD), general packet radio service (GPRS) and enhanced data rates for GSM evolution (EDGE), the settling time of the synthesiser is limited to an even more critical range.

Fractional-N frequency synthesisers are now widely used in mobile handsets but not in base stations. While the handset settling time and phase noise requirements are relatively relaxed, a base station synthesiser needs to settle significantly faster and with much lower phase noise. In the worst case, the base station communicates with a

different handset during every time slot, only having the guard time between slots (30.5 μs) for channel switching. High speed data standards, such as HSCSD and EDGE, require even faster switching. With a channel spacing of 200 kHz, the typical reference feedthrough requirement sets the maximum loop bandwidth to approximately 20 kHz. So a third order loop can provide 40 dB suppression on the reference spur at 200 kHz offset. These conflicting requirements call for more complex frequency generation techniques. A typical method in base stations to meet this need is the so called "ping-pong" synthesiser. The base station has two separate integer-*N* synthesisers, allowing one to switch to a new channel during a time slot, while the other one is being used. During the slot guard time, the synthesisers switch roles, and during the next slot, the other synthesiser is used. The drawbacks of this solution are obvious: two integer-*N* synthesisers are used to generate the carriers in order to tune between channels in a short time. This increases the cost, complexity and power consumption of the system. Benefiting from its wider bandwidth, a single fractional-*N* synthesiser can replace the role of the "ping-pong" synthesiser with same or faster tuning speed. However, the trade-off between bandwidth and phase noise becomes a problem. The extension of loop bandwidth may lead to higher out-of-band phase noise. This requires a fractional-*N* synthesiser with very low in-band phase noise.

The Σ-Δ based fractional interpolator, working with a frequency divider, allows programmable modulus fractional-*N* division. The switching architecture ensures that the PLL settles inside the GSM time slot guard period, removing the need for a second PLL and associated isolation switches [80]. This decreases cost, complexity, PCB area, shielding, and characterisation relative to previous "ping-pong" GSM PLL architectures.

Besides the settling time, phase noise is another important parameter that every synthesiser designer must carefully consider. Base stations have more critical requirements than handsets on the overall phase noise and spur level which will affect the performance of the whole system. The GSM specifications for phase noise and spurious masks [81] are shown in Figure 1.1.

Equation (3.29) presents that higher reference frequencies enable the use of lower prescaler ratios, with a resultant reduction in multiplied phase/frequency detector and reference noise and thus the ability to achieve lower phase noise with wider fractional

operating bandwidths. However, the speed of Σ-Δ modulators is the greatest challenge. Few designs of high frequency (> 50 MHz) Σ-Δ modulator used in fractional-*N* frequency synthesisers have been reported to date. The stored-sequence technique is a valuable method to overcome the bottleneck of low operating frequency and offers other advantages such as noise shaping optimisation.

4.2 Memory Controlled Frequency Dividers

4.2.1 General Description

The structure complexity and inefficient reusability of ripple fashion dividers limit their usage in a real circuit design. In addition, implementing such a divider by a monolithic circuit method will incur significant cascaded delays and high cost. This section introduces an alternative technique for design of a dual or multi modulus divider that is inherently suited to programmable embedded system implementation such as FPGA or CPLD that can allow convenient implementation of such a frequency divider without external hardware or integrated circuit employment [82, 83].

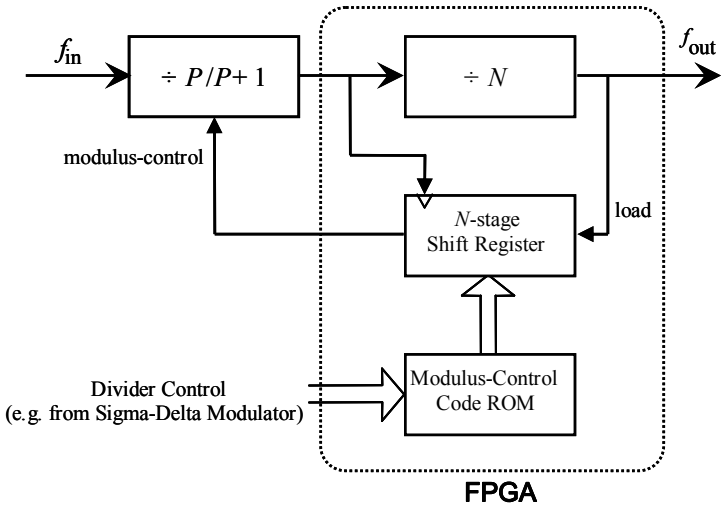


Figure 4.2 The proposed memory-controlled divider, with a division ratio of *NP* to *N*(*P*+1).

Figure 4.2 shows the basic arrangement of a dual-modulus frequency divider with use of the proposed memory-controlled divider technique. It consists of a ÷*P*/*P*+1 dual-modulus prescaler cascaded with a divide-by-*N* counter, the output of which loads a *N*-bit word from a modulus control code ROM into an *N*-stage shift register. The shift register is clocked by the ÷*P*/*P*+1 prescaler output and determines the prescaler division ratio. This prescaler output is then further divided by the fixed ratio counter to generate a lower output frequency. The total division ratio of this arrangement thus depends on the number, *n*, of logic-1 bits that are presented to the shift register in a f_{out} cycle and is adjustable over the range *NP* to *N*(*P* + 1), as follows:

$$D = N \cdot P + n \tag{4.1}$$

where $0 \le n \le N$, and hence $NP \le D \le N(P+1)$.

A simple look-up table can be used to derive the required values for the shift register control word needed to achieve a given division ratio. In terms of an FPGA or PLD implementation, all elements in the design apart from the prescaler are contained with the FPGA/PLD and so the technique presents a very convenient means of implementing a programmable high frequency divider. Furthermore, other synthesiser operations, such as Σ-Δ modulation for noise shaping, can be performed by the same FPGA or PLD thus allowing integration of these functions in one device.

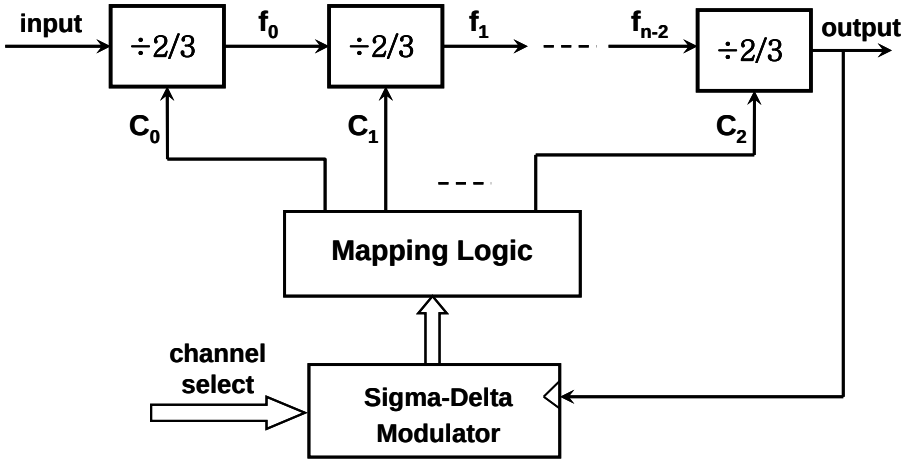


Figure 4.3 A general memory-controlled multi-modulus divider.

The divider design of Figure 4.2 does have a limited division range because its dual-modulus division can be only controlled by a single-bit Σ-Δ modulator. However this can be overcome by replacing the fixed ÷*N* counter with a variable ratio divider based on the same technique. This approach is illustrated in the following design example.

Figure 4.3 shows a general arrangement of a multi-modulus divider based on the memory-controlled technique [82, 83]. This architecture can be configured to work with variable Σ-Δ modulators and other applications. The divide-by-2/3 blocks can be replaced by any divide-by-*P*/*P*+1 block to achieve a variety of division ratios. The output of the Σ-Δ modulator stores logic signals into a series of shift registers. Each shift register is clocked by the divider output and determines its division ratio respectively. Cascading *n* divide-by-2/3 dual-modulus blocks can produce division ratio of 2*n* to 3*n*. The range of modulus values is now:

$$N_{MC} = 3^n - 2^n + 1 \tag{4.2}$$

The division ratio of this architecture is:

$$D = 2^n + M_0 \cdot 2^{n-1} + M_1 \cdot 2^{n-2} + \cdots + M_{n-1} \tag{4.3}$$

where $0 \le M_p \le 3^{n-p}$ $\left(0 \le p \le n-1\right)$.

In which $M_{n-1}, M_{n-2}, \ldots, M_0$ are divide-by-3 bit number of $C_{n-1}, C_{n-2}, \ldots, C_0$ in a period of f_{n-1} respectively. Although its modulus range is much wider than the ripple fashion prescaler, extra shift registers or ROMs are employed to control the division ratio of every block working under different frequencies. The total number of bits used in the ROM is:

$$N_{bits} = \frac{3^n - 1}{2} \tag{4.4}$$

For example, six cascaded divide-by-2/3 cells merge into a 666-modulus divider with continuous integer division ratios from 64 to 729. At least a 364-bits ROM must be used to achieve the memory-controlled division control function. All division ratios in this range can be programmed with continous integer divide values. As mentioned

before, the divide-by-2/3 block can be replaced by any divide-by-P/P+1 block, but all blocks should be the same to achieve unit increments of instantaneous division ratios. If an increment other than one is desired, the optimal architecture is to place a fixed ratio divide-by-N stage in front of the multi-modulus cells.

A comparison of this proposed technique with conventional phase switching and ripple fashion dividers is shown in Table 4.2. In comparision to ripple fashion dividers, the proposed architecture has better reusability and programmability. By eliminating high frequency feedback signals and adding a high frequency memory control element, a principle advantage of the memory controlled divider is that it efficiently uses every component. In addition, modulus repetition can be avoided by defining appropriate control signals derived from the suitable Σ-Δ modulator output sequence.

Table 4.2 Comparison of frequency dividers.

ARCHITECTURE	MODULUS	DIVISION RANGE	PROBLEM
Phase Switching	4	P — P + 3	Spurious tones
Ripple Fashion	2^{n+1} — 2^n	2^n — $2^{n+1}-1$	Adjacent feedback signals
Memory-Controlled	3^n — 2^n + 1	2^n — 3^n	Shift-register employed

4.2.2 An 18-modulus Memory-Controlled Divider

An 18-modulus divider based on the memory-controlled technique has been developed for a typical fractional-N synthesiser in GSM systems. The synthesiser is required to operate in the GSM-900 band with a 12.8 MHz reference frequency. Since synthesisers normally have high power consumption and often occupy considerable area, it is very important to limit the number of components required by the radio architecture. Thus, for GSM-900 base stations, a divider and a Σ-Δ modulator are implemented by a single FPGA.

The required output frequency of the synthesiser is f_{out} = (935 + 0.2k) MHz, where k = 0, 1, 2,…, 125. The division ratio needs to be:

$$D = \frac{f_o}{12.8} = 73.046875 + 0.015625k \tag{4.5}$$

i.e. $D = 73.046875 \sim 75$.

Assuming that a third order Σ-Δ noise shaper (modulator) with 3-bit output is used to produce noise shaping in a fractional-*N* synthesiser, the instantaneous division ratio could vary from −3 to 4 around the fractional mean division ratio. Thus, the integer division range of the multi-modulus divider is given by $D \in [70,77]$.

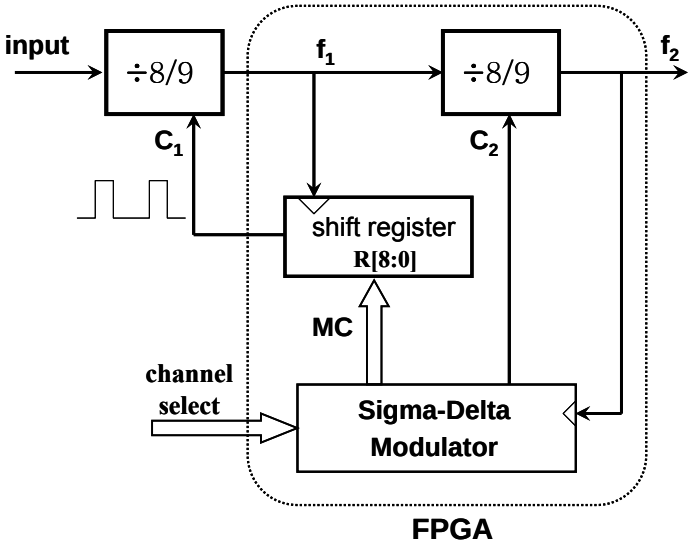


Figure 4.4 A memory-controlled 18-modulus divider suitable for GSM systems.

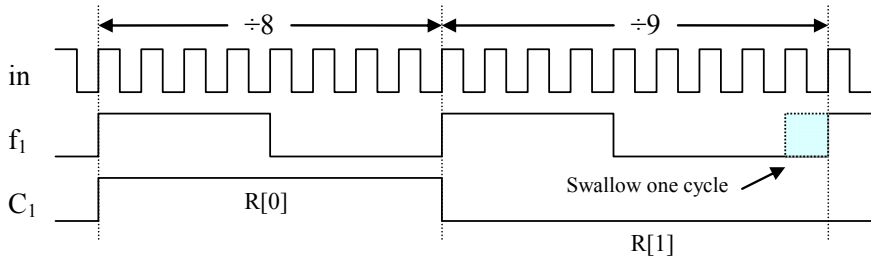


Figure 4.5 Modulus control function of the ÷8/9 block.

Figure 4.4 shows an 18-modulus memory controlled divider that is designed to satisfy this requirement. This implementation occupies about 1000 logic gates of the FPGA device XC2V1500. The high-frequency VCO output signal is divided by two cascaded divide-by-8/9 dividers. The output signal f_2 is around 12.8 MHz. It is compared with the reference frequency at the phase/frequency detector, which generates the phase

difference signal. Meanwhile, the Σ-Δ modulator is also clocked by f_2. At the rising edge of every f_2 cycles, the Σ-Δ modulator begins processing one cycle and generates two modulus control bit streams: *MC* (9-bit) and C_2 (1-bit). C_2 is directly used to control the division ratio of the second divide-by-8/9 divider. When C_2 is logic-0, f_1 is divided-by-9, which means this block swallows an extra single f_1 cycle in a complete division cycle, increasing the period of the output signal of this block by one period of f_1; when C_2 is logic-1 (high voltage), the output frequency f_2 is 8 times f_1. At the same time, a 9-bit word is loaded into a 9-stage shift register which is clocked by the divide-by-8/9 prescaler output and determines its division ratio. The total division ratio of this arrangement thus depends on the number, *n*, of logic-1 bits that are presented to the shift register and is adjustable over the range 64 to 81. A time diagram of the $\div 8/9$ modulus control function is shown in Figure 4.5. Each bit stored in the memory corresponds to a constant position signal result of f_1, for example that *R*[3] always only controls the fourth clock cycle of f_1 after each rising edge of f_2. This will reduce the complexity of the system and any output will be obtained as required. Its division ratio can be easily derived from equation (4.3):

$$D = 8 \times \left(\overline{C}_2 + 8\right) + N_{MC} \left(0 \le N_{MC} \le 8\right) \tag{4.6}$$

Suppose C_2 is low voltage and the bit stream of *MC* is 111 111 000, then N_{MC} is 3 and the first block will swallow three time cycles and the second will swallow one. The division ratio of the complete cycle will be 75.

The $\div 8/9$ divider can be implemented using four D-latches and three logic gates as shown in Figure 3.5. The component architecture and area occupation are similar to those of a divide-by-2/3 block in a conventional programmable divider. Hence the memory controlled divider will provide an approximate 50% saving on components and area even though some registers are needed. As discussed earlier, two cascaded $\div 8/9$ dividers can be merged into an 18-modulus divider, whose integer division ratio varies continuously between 64 and 81. This arrangement can synthesise all required frequencies in GSM or DCS systems if controlled by a Σ-Δ modulator with a two or more bit quantizer. If four dual modulus blocks are employed, the modulus can be extended to 180, which will satisfy a wide variety of wireless applications.

This new technique may be combined with the "stored-sequence" synthesiser approach in which pre-generated modulator bitstreams are clocked out from memory in order to allow very fast loop operation and low phase noise. This presents a very convenient, streamlined architecture allowing a single block of memory to determine both noise shaping and prescaler modulus control and adds further to the elegance of the technique in an FPGA or CPLD implementation.

4.3 FPGA Implementation of Sigma-Delta Modulators

The Field Programmable Gate Array (FPGA) is able to offer many advantages over traditional programmable devices. FPGAs are widely used to implement digital systems due to their incomparable flexibility, reconfigurability and the ease and low cost of development. They can also be used to perform multiple operations in different areas of the system. The FPGA technology is very suitable for implementation of high-speed digital Σ-Δ modulators especially in high performance fractional-*N* frequency synthesisers and many other A/D converters. Although few FPGA based Σ-Δ modulators have been reported to date, undoubtedly it will become an alternative approach to implement the digital parts in indirect fractional-*N* synthesisers including Σ-Δ modulators and multi-modulus dividers in the near future. A variety of Σ-Δ modulators can be implemeted by a single FPGA to optimise individual channels.

In a synthesiser context, the Σ-Δ modulator provides a fractional mean division ratio with low close-in phase noise at the expense of increased phase noise further from the carrier, where it may be readily suppressed by the action of the PLL loop filter. This is, of course, a very valuable technique, although it tends to suffer from a number of practical limitations:

1) Restricted operating speed versus phase noise compromise: The Σ-Δ bitstream is generated in real time and is constrained by technology limits on the speed of digital adders. Recent designs have reported operation up to 50MHz [84], though higher speeds would be preferable to improve synthesiser tuning speed and spectral purity.
2) Restriction to integer weights: To achieve relatively fast operation, the Σ-Δ loop

usually operates with integer quantizers, which can result in short limit cycles under certain conditions and gives limited design flexibility. Similarly, the adder resolution is limited by hardware constraints.

3) Non-optimal weights for each channel: The optimum weights required to minimise spectral components at the synthesiser output vary from channel to channel, a feature that would be difficult to incorporate in a fixed logic architecture.

4) Stability is not guaranteed: high order Σ-Δ architectures tend to be vulnerable to unstable operation.

The key feature of the stored-sequence technique is that the Σ-Δ logic block is replaced by a counter and a ROM which act to clock out pre-generated bitstream [85]. These are generated off-line by simulation of a given Σ-Δ loop. This approach allows the bitstreams to be individually optimised, on a channel-by-channel basis, possibly by modelling a number of entirely different Σ-Δ architectures, with no restriction to integer weights or finite resolutions. By multiplexing an 8-bit or 16-bit wide ROM, the bitstream can be produced at a very fast rate so that the limiting factor is likely to be the speed of the phase detector. Thus a very high reference frequency may be used with a commensurate reduction in phase noise [73, 74].

A further advantage of the use of a very high reference frequency is that reference sidebands are likely to be completely outside the operating band of the synthesiser. Finally, stability is not an issue since any unstable bitstreams are rejected at the simulation stage. The reference frequency should ideally be chosen so that the fractional component of the division ratio is close to 0.5 in the centre of the output frequency range, as this is likely to provide the best overall noise performance over the complete operating range. In the case of the GSM-900 base stations considered in this work, a reference frequency of 105 MHz is appropriate with a ÷8/9 prescaler in order that the mean division ratio is around 8.5 in the centre of the 890 to 915 MHz band and varies from 8.476 to 8.714 across the band. A further benefit arising from the use of such high reference frequencies is that the division ratio is very low; this results in a reduction in the multiplied phase detector and/or reference noise, for improved in-band noise performance, and also allows a high fractional bandwidth to be obtained from a fractional-*N* synthesiser based simply on a dual modulus prescaler.

The technique is particularly suitable for use in burst mode applications where, if sufficient memory is available, then an entire stored bitstream may be clocked out for each channel of operation without the need for repetition. Pre-generated bitstreams for all channels are stored in a memory, then a channel selection signal addresses a bitstream with a average value which is equivalent to the DC input. The memory requirement is a function of the burst period T and the reference frequency as follows:

$$\text{Memory required (per channel)} = T \cdot f_{ref} \tag{4.7}$$

In the case of the GSM or DCS application, the burst period is 577 μs which, from equation (4.7), requires sequences of length 60585 bits per channel and so 64 kbits of memory per channel is a convenient choice. There are 125 channels in GSM-900 and 375 channels in DCS-1800 systems, giving a total memory requirement for the synthesiser of 8 Mbytes and 24 Mbytes respectively. Since a given base station typically uses only a small fraction of the 125 or 375 channels, there is a substantial reduction in the memory requirement for any individual base station.

The Σ-Δ modulators analysed in Chapter 3 have been implemented on a Xilinx FPGA XC2V1500 with a multi-modulus frequency divider combined to merge into the digital part of a fractional-*N* synthesiser. The FPGA has a maximum RAM speed of 450 MHz in theory. To enhance the sampling frequency of the Σ-Δ modulators, the stored-sequence technique [86, 87] is employed, allowing the Σ-Δ modulators to be suitable for high frequency telecommunication and radio frequency systems. Compared with the pipelining technique, The stored-sequence approach is a more effective solution to eliminate cascaded delays in digital systems.

The input channel selection of the simulated Σ-Δ modulators is chosen as 943 of 2048 with a LSB dithering offset, $1/2^{17}$, giving a channel spacing of approximately 5 kHz. The time domain output of the Σ-Δ modulator and frequency domain noise shaping are recorded and compared under different sampling frequencies. Figure 4.6 shows the measured time domain output of an FPGA implemented single-stage Σ-Δ modulator as shown in Figure 3.27. A Xilinx FPGA XC2V1500 is used to implement Σ-Δ modulators. If the input of the third order single-stage modulator is 17-bit, this design occupies about 1500 logic gates. A digital phosphor oscilloscope Tektronix TDS5104B

is used to record measured waveforms. The upper sinusoidal waves are clock driving or sampling frequencies, which are constant frequencies generated by a low noise signal generator; the square waves are logical outputs of the Σ-Δ modulator which will be used to control the division ratio. Figure 4.6(a) presents the output signal when the sampling frequency is 1 MHz, in which the critical square wave can result in an expected noise shaping in the frequency domain. If the sampling frequency is enhanced to 10 MHz, the measured waveform, as shown in Figure 4.6(b), presents some noise on the square wave that may raise the noise floor of the noise shaping. In Figure 4.6(c), the sampling frequency is 100 MHz and the output waveform is severely distorted, which will cause concern in the frequency domain and lead to unexpected noise shaping or miscount. This is related to the performance of the FPGA component and PCB design, such as delays, signal coupling and impedance matching. A recently introduced technique, named Xilinx controlled impedance technology (XCITE), allows variable FPGA input and output impedances. XCITE eliminates the need for external termination resistors by incorporating adaptive series and parallel termination resistors on the FPGA itself [88]. The on-chip resistor values can be defined via an external pair of reference resistors. The digital implementation of this technology guarantees that the on-chip resistor values do not vary when temperature or supply voltage shifts. Figure 4.6(d) shows the measured result under the same sampling frequency as in Figure 4.6(c), but using XCITE for impedance matching. It is obvious that the output waveform is closer square with less noise and greater amplitude, leading to lower unwanted noise in frequency domain.

Figure 4.7 shows modelled and measured noise shaping of the FPGA implemented single stage Σ-Δ modulator with feedback paths. The purpose of the use of Σ-Δ modulators in fractional-*N* frequency synthesisers is to push the quantisation noise to high frequencies, giving low close-in noise. Hence the low frequency offset noise level affects the synthesiser in-band phase noise directly. Figure 4.7(a) and (b) present the modelled and measured noise shaping from 0 to $0.5f_{ref}$ frequency offset. The measurement is under the condition of a sampling frequency of 1 MHz, and the modelling is based on a MATLAB program as shown in Appendix B.1. The measured and modelled noise shaping match very well except that the discrete spurs of the measured spectrum have lower amplitude. Their low frequency offset zoom-in

comparison is shown in Figure 4.7(c) and (d). It is apparent that the measured high frequency offset noise level matches the modelled result; however the measured result shows higher close-in ($\leq 0.1 f_{ref}$) noise. This is thermal noise and random jitter in a real circuit implementation and the noise level is in the satisfactory range of lower than −95 dBm at 30 Hz resolution bandwidth. Increase of sampling or reference frequency of the Σ-Δ modulator may result in its output noise shaping suffering from higher close-in noise than desired. Figure 4.7(e) shows the measured spectrum under the condition of 100 MHz sampling frequency, which presents unacceptable close-in noise of −52 dBm. As demonstrated in the time domain, the XCITE may alleviate this problem. Figure 4.7(f) shows the measured spectrum with XCITE, now the close-in noise is 15 dB lower than that without XCITE employment. This optimised noise shaping is also used in the later closed loop developments.

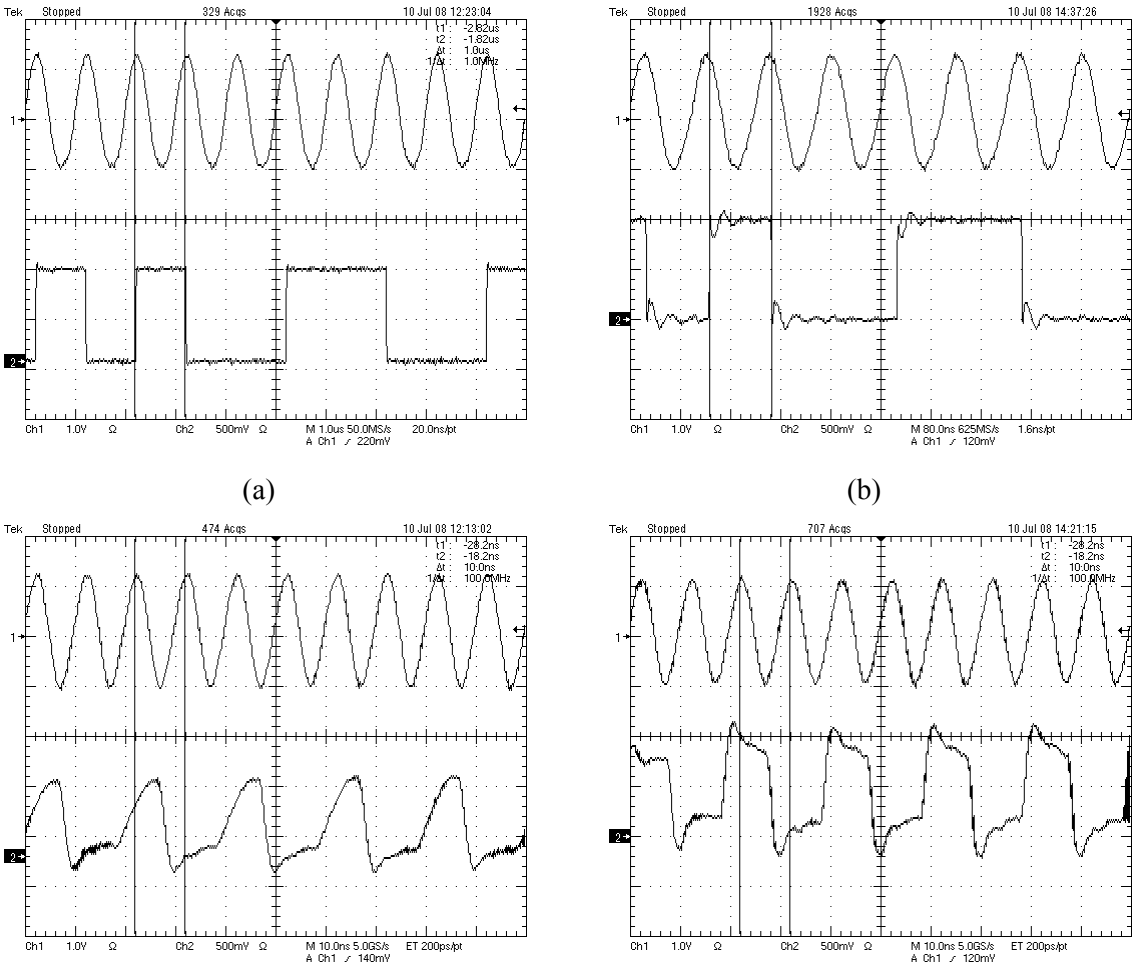


Figure 4.6 Time domain output of the FPGA implemented Σ-Δ modulator. (a) Sampling frequency: 1 MHz. (b) Sampling frequency: 10 MHz. (c) Sampling frequency: 100 MHz. (d) Sampling frequency: 100 MHz with XCITE.

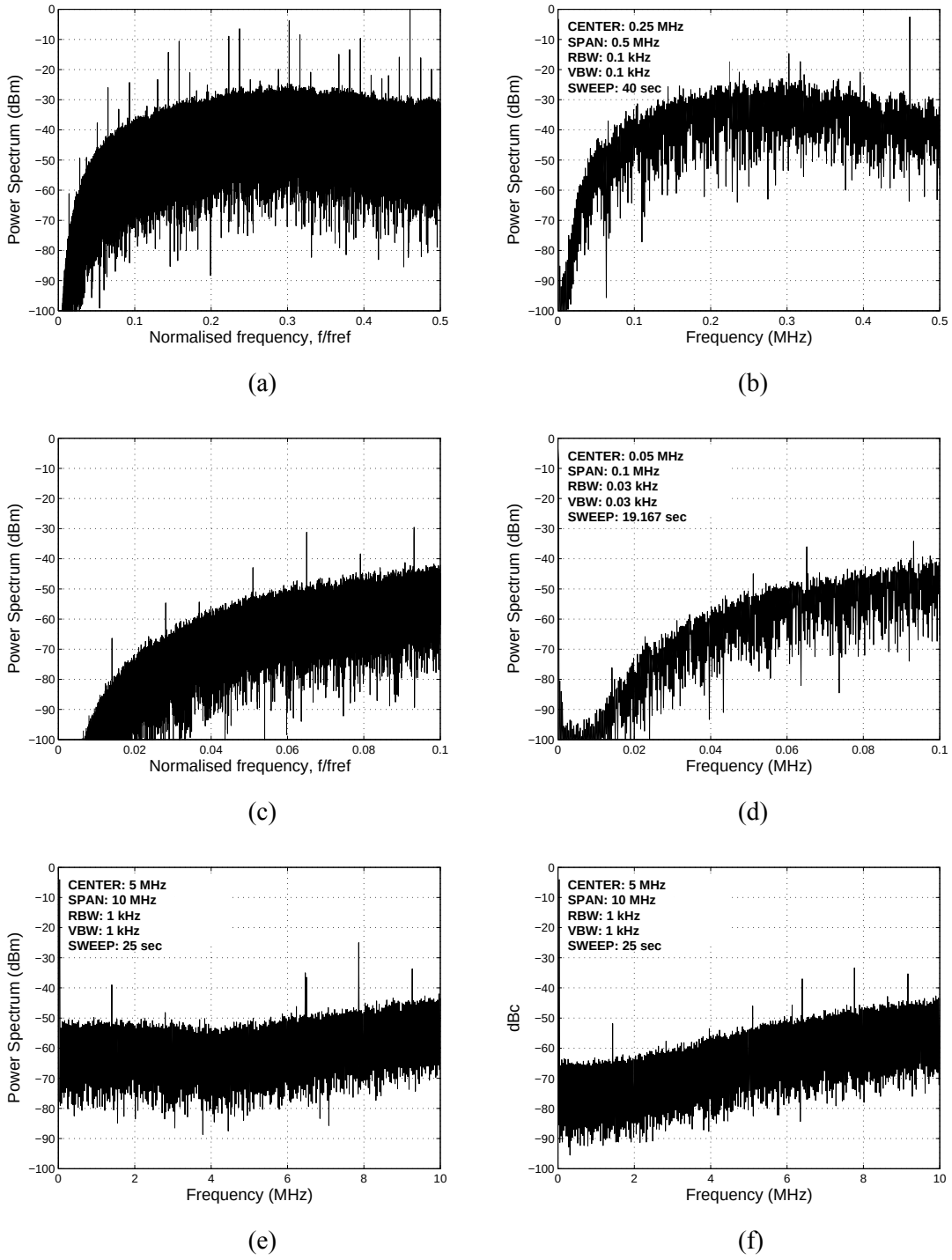


Figure 4.7 Modelled and measured noise shaping of the FPGA implemented Σ-Δ modulator. (a) Modelled noise shaping, span: $0.5f_{ref}$. (b) Measured noise shaping at 1 MHz sampling frequency, span: $0.5f_{ref}$. (c) Modelled noise shaping, span: $0.1f_{ref}$. (d) Measured noise shaping under 1 MHz sampling frequency, span: $0.1f_{ref}$. (e) Measured noise shaping at 100 MHz sampling frequency, without XCITE. (f) Measured noise shaping at 100 MHz sampling frequency, with XCITE.

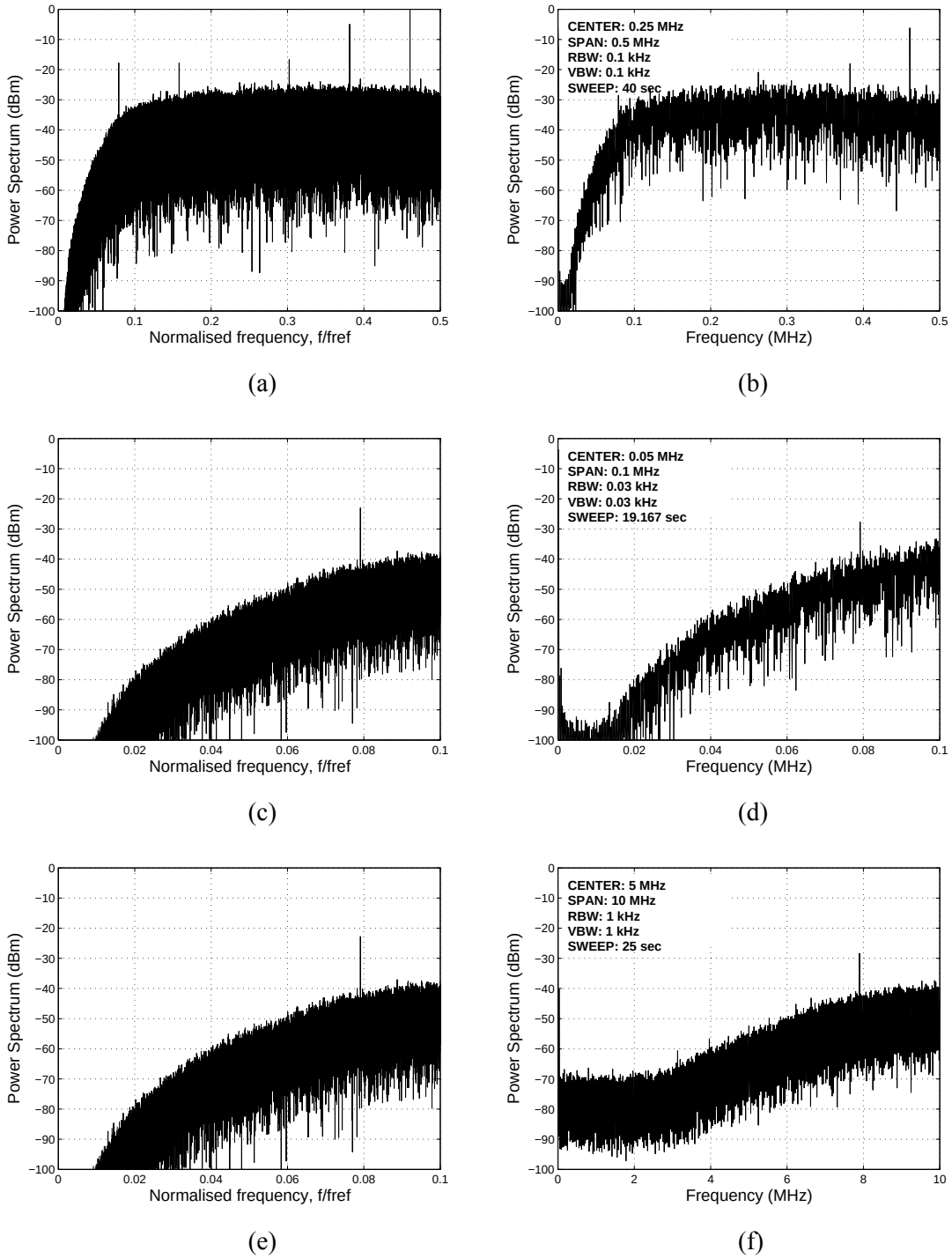


Figure 4.8 Modelled and measured noise shaping of the FPGA implemented Butterworth single-stage Σ-Δ modulator. (a) Modelled noise shaping, span: $0.5f_{ref}$. (b) Measured noise shaping at 1 MHz sampling frequency, span: $0.5f_{ref}$. (c) Modelled noise shaping, span: $0.1f_{ref}$. (d) Measured noise shaping at 1 MHz sampling frequency, span: $0.1f_{ref}$. (e) Modelled noise shaping, span: $0.1f_{ref}$. (f) Measured noise shaping at 100 MHz sampling frequency, with XCITE.

This exercise has been repeated with a different architecture of single-stage third order Σ-Δ modulator with feedforward paths. This Σ-Δ modulator utilises a Butterworth high-pass response and it should result in a different noise shaping from the single-stage feedback Σ-Δ modulator. One obvious difference is that the noise shaping presents a corner frequency where the noise floor is almost flat at higher frequency offsets. Figure 4.8 shows the modelled and measured noise shaping of this Σ-Δ modulator. The same FPGA device XC2V1500 is employed in this measurement and a spectrum analyser Agilent 8560E is used to record spectra. The modelled noise shaping, as shown in Figure 4.8(a), presents less spurious components than that of the feedback architecture, however, the measured result (Figure 4.8(b)) shows quite similar spur distribution. Figure 4.8(d) and (f) show that the quantisation noise at $0.1f_{ref}$ is about 5 dB higher than as shown in Figure 4.7(d) and (f), however, its close-in noise is 5 dB lower.

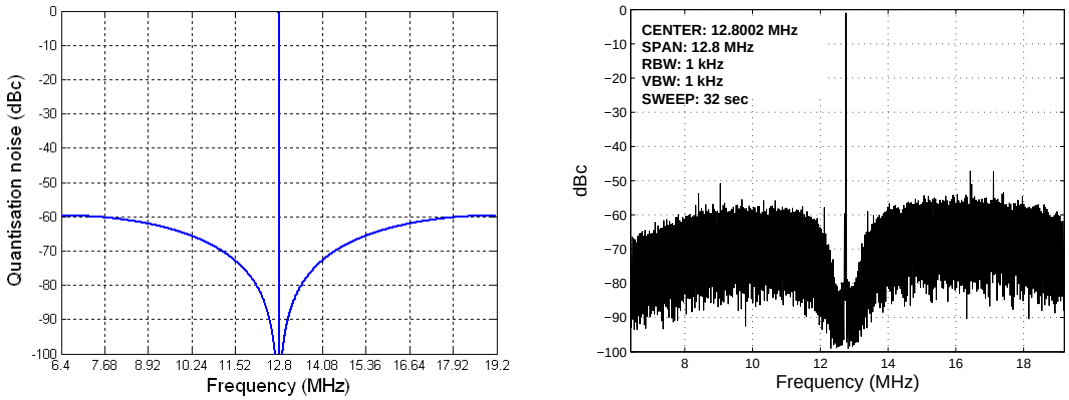


Figure 4.9 Simulated and measured quantisation noise of the MASH 2-2 Σ-Δ modulator.

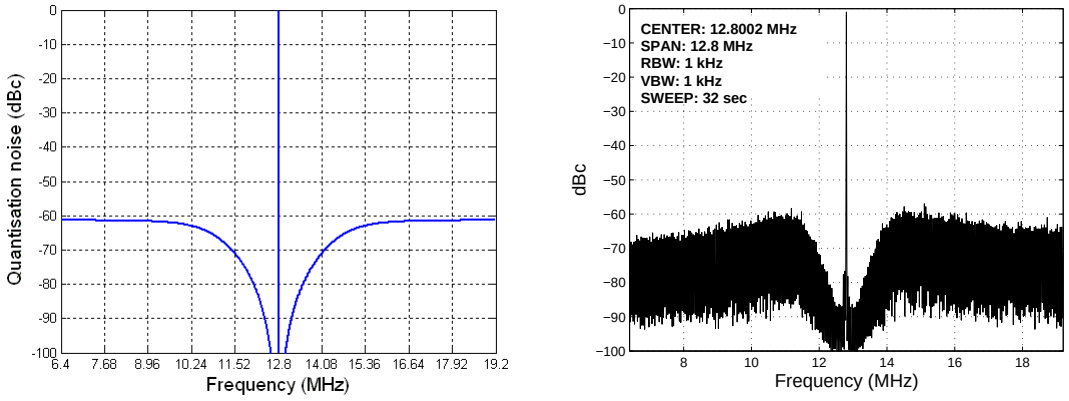


Figure 4.10 Simulated and measured quantisation noise of the third order single stage Σ-Δ modulator.

Taking advantages of the stored-sequence approach, complex Σ-Δ modulators and advanced dithering techniques, such as the small random noise method, may be easily implemented by MATLAB/SIMULINK modelling utilising a powerful PC rather than real-time FPGA processing. Furthermore, noise shaping can be generated at higher sampling frequencies compared to the quantisation noise output of a typical monolithic component. Because of the low division ratio, multi-bit Σ-Δ modulators such as MASH are not suitable in these high reference frequency designs. However, there are many other applications that may require a relatively low reference frequency and high division ratio. In these systems, Σ-Δ modulators can also be directly implemented by real-time FPGA processing, in conjunction with an integrated multi-modulus frequency divider as illustrated.

A 3-bit (6-level) output MASH 2-2 Σ-Δ modulator and a single-stage third order Σ-Δ modulator with a 3-bit quantizer are developed by direct implementation of an FPGA. Because multi-bit noise shaping can not be directly monitored in frequency domain, to sense the quantisation noise, frequency divider output spectra are recorded. The input frequency is 940.3 MHz, and the fractional division ratio is 73.46. As a result, the divided frequency is about 12.8 MHz.

Figure 4.9 shows the open loop results of the prototype with MASH 2-2 Σ-Δ modulator. This real-time modulator uses about 3000 logic gate when implemented by XC2V1500. The divider output centre frequency is around 12.8 MHz, and quantisation noise is pushed to higher frequency offsets, leaving the low close-in noise floor. The results from the frequency divider with a third order single stage feedforward Σ-Δ modulator are illustrated in Figure 4.10. The Σ-Δ modulator includes a 3-bit (8-level) quantizer, but its output only occupies four levels at individual channels. The cut-off frequency of the spectrum is about 2 MHz from the signal, which is the same as the simulated result in Figure 3.23. The simulated results are generated by NTFs and it is not possible to present spur distributions and details because the quantisation process is not considered.

Four FPGA based Σ-Δ modulators have been implemented to suppress the in-band noise of the fractional-*N* frequency synthesiser. Benefiting from their high sampling frequencies, the Σ-Δ modulators will significantly reduce the noise and dithering spurs present in such synthesisers, enhance the dynamic range and lead to better overall performance. By using a reference frequency of at least 100 MHz, with 5 kHz

frequency resolution, the in-band phase noise and the spur performance of the proposed Σ-Δ modulators meet the requirements of most telecommunication applications including GSM and DCS.

4.4 Low Reference Frequency Fractional-N Synthesiser

The fractional-*N* synthesiser design process can be broken into three parts as shown in Figure 4.11, in which apart from the analogue components of the phase-locked loop, the multi-modulus frequency divider and the FPGA component used to implement a Σ-Δ modulator. To satisfy the low noise requirement of the synthesiser, every single component must have good noise and speed performance. Furthermore, power dissipation, impedance matching and layout optimisations also affect the performance dramatically.

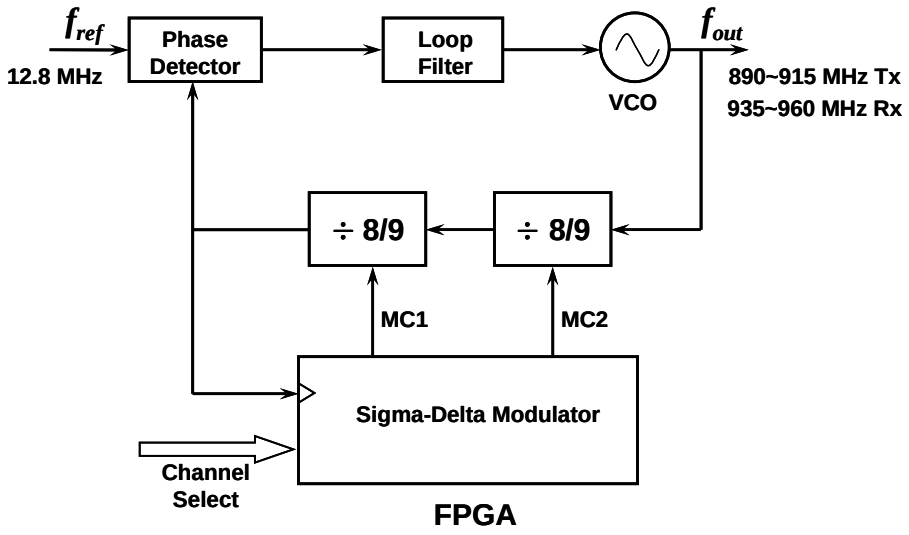


Figure 4.11 Block diagram of an implemented high division ratio fractional-*N* synthesiser.

To generate a stable high frequency signal, every PLL synthesiser needs a relatively low frequency reference source. Because the noise of the reference source is directly transferred to the output without any filtering process, the requirements on its stability and phase noise are stringent. High performance oven controlled crystal oscillators (OCXOs) are the best choice because of their extremely low close-in phase noise and outstanding stability. These oscillators employ crystal oven to maintain quartz crystal at

a constant temperature, in order to prevent changes in the frequency due to variations in ambient temperature. However, their high cost and large dimensions are not suitable for laboratory testing. Therefore, an alternative low noise temperature controlled crystal oscillator (TCXO) C-MAC CFPS-9000 [89] is chosen as a reference source in the high division ratio fractional-*N* synthesiser design.

A standard low phase noise VCO type CLV1025E manufactured by Z-Communications is selected. This VCO was chosen as it has −112 dBc/Hz phase noise at 10 kHz offset, which is the lowest of any off the shelf unit available to cover the GSM-900 frequency band. An attenuator and buffer amplifiers are used to provide isolation of the VCO output. This prevents frequency pulling and any resulting increase in the synthesiser phase noise. The type HP MSA-0986 MMIC buffer amplifier has 7.2 dB of gain from 0.5 to 3 GHz and a reverse gain of −40 dB. Figure 4.12 shows a photograph of the RF section implemented on discrete printed circuits boards, in order to prevent signal coupling between adjacent components and signal tracks.

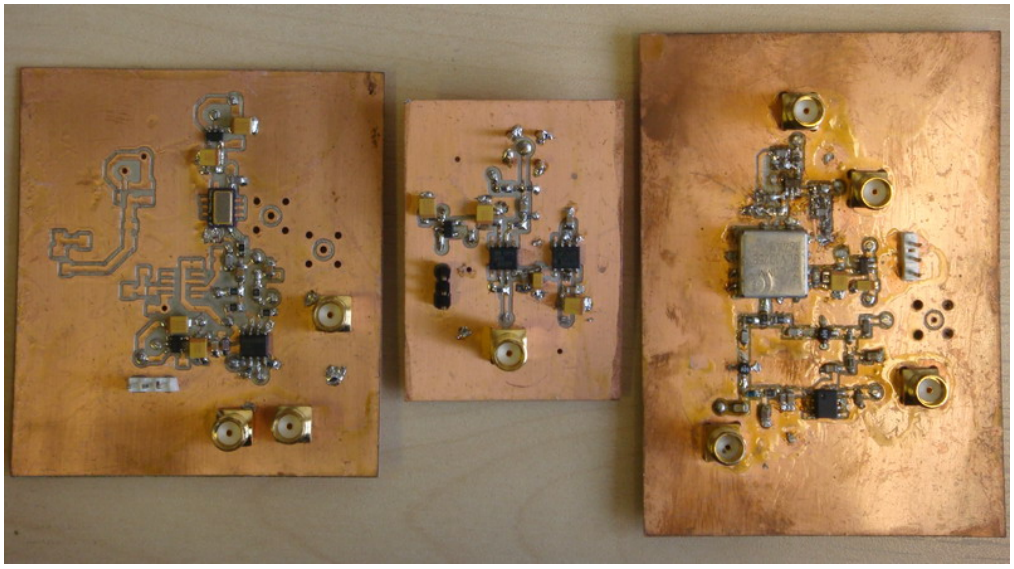


Figure 4.12 RF section of a fractional-*N* synthesiser implemented on discrete PCBs.

The most complicated and important part of the synthesiser is the digital module: a Σ-Δ modulator and a frequency divider. In this synthesiser design, the Σ-Δ modulator is implemented by an FPGA Xilinx XC2V1500, which integrates over one million logical gates and can achieve as high as 450 MHz toggling frequency in theory.

The GSM-900 transceiver must continuously cover the frequency range between 935 MHz and 960 MHz. If a 12.8 MHz reference source is used, the division ratio can be derived from equation (4.5), i.e. 73.04625 ~ 75. As illustrated in chapter 3, the MASH 1-1-1 Σ-Δ modulator has 8-level output from −3 to 4, which demands a 9-modulus divider. The divider fracture should have continuous modulus from 70 to 78. An 18-modulus divider as illustrated in chapter 3 has been implemented to satisfy the requirement. Meanwhile, it can also interface with any other 4-level and 2-level output Σ-Δ modulators.

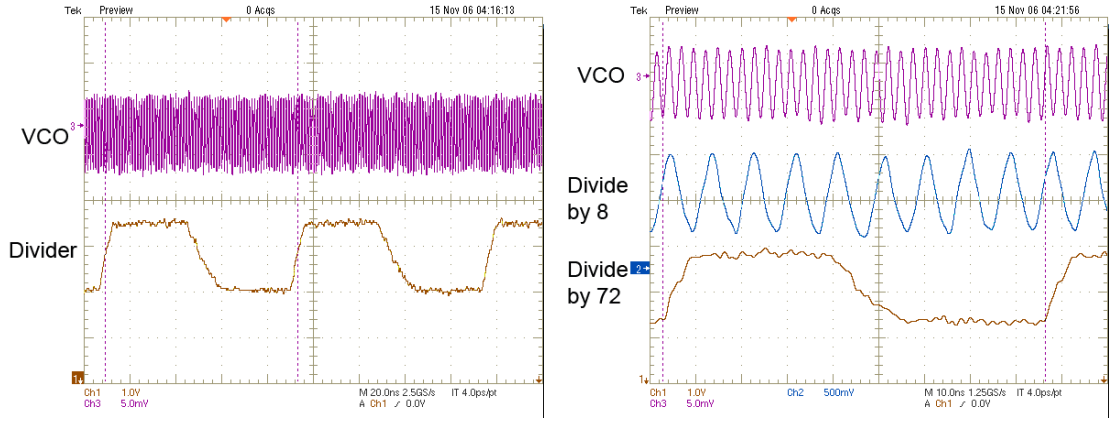


Figure 4.13 Time domain outputs of the VCO and frequency divider.

The measured integer division output waveforms are shown in Figure 4.13. The frequency divider is implemented by cascading two 8/9 dual-modulus prescalers. A standard type MC12026AD made by On Semiconductor is selected because of its simple architecture and low noise. In fact the second 8/9 prescaler can also be implemented by the FPGA together with a Σ-Δ modulator. The digital output is reliable at 100 MHz sampling frequency without missed counts. However, it is found that the phase noise of the FPGA output is not as low as the external prescaler. The close-in noise from the output of the frequency divider is VCO output without any filtering, so the requirement of low noise is critical to the output of the frequency divider. Figure 4.14 shows the measured spectra of the synthesiser at integer divide-by-72 mode. The reference frequency is 12.8 MHz, so the output frequency is 921.6 MHz. The significant spurs at 355 kHz offset from the carrier are the dominant noise of the FPGA evaluation board. The noise level of other integer division ratios is within 2 dB range of this measured results and shows similar phase noise characteristic.

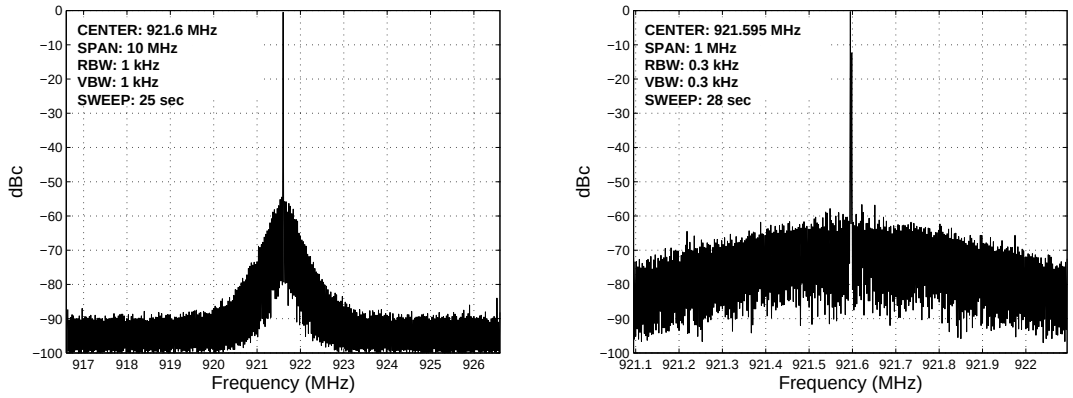


Figure 4.14 Measured spectra of the integer synthesiser with 10 MHz span (left) and 1 MHz span (right).

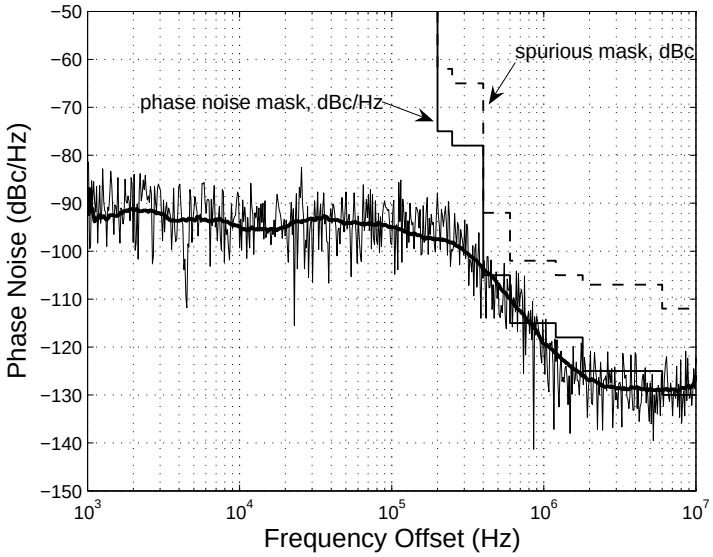


Figure 4.15 Measured phase noise of the integer synthesiser.

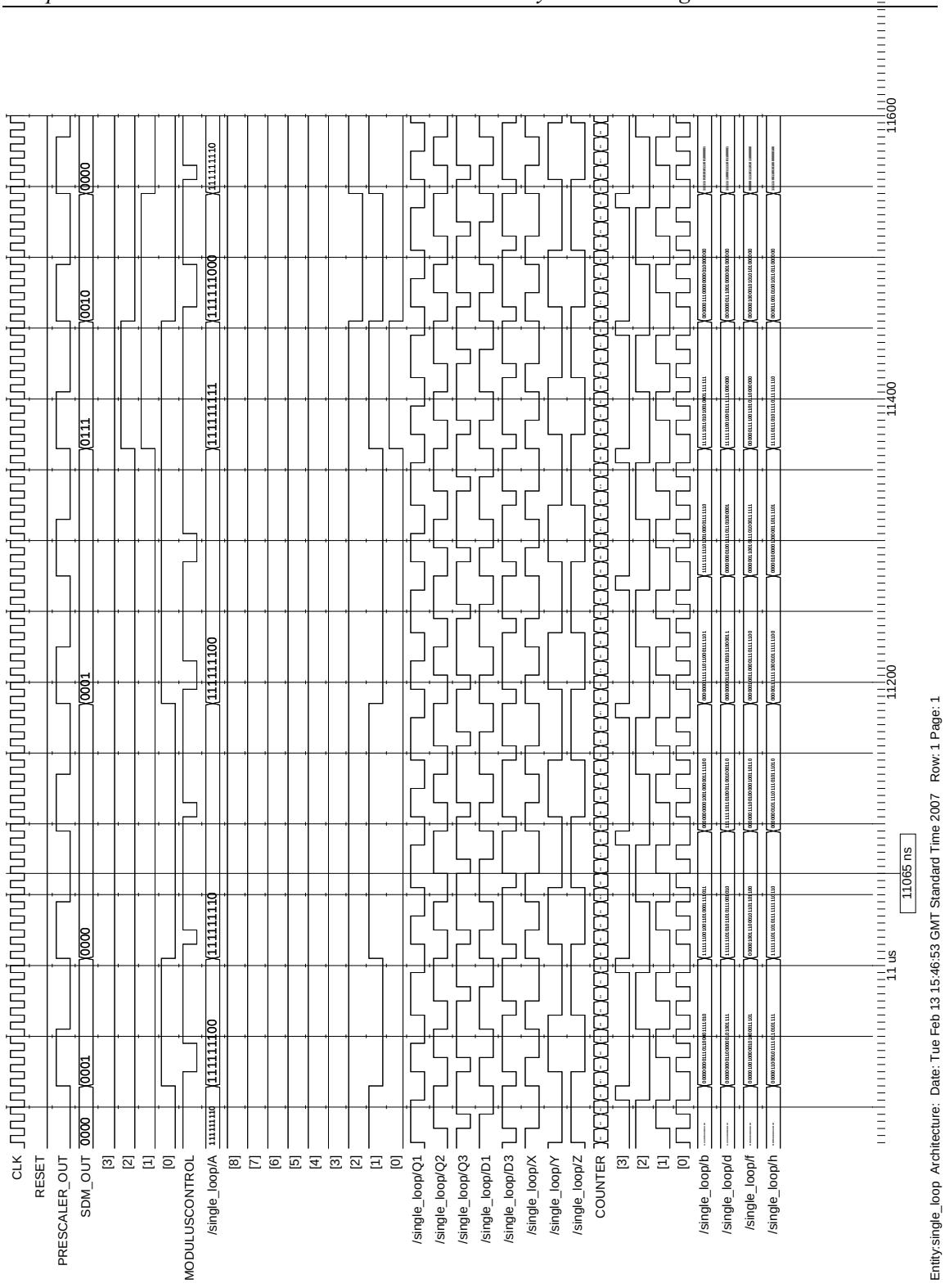


Figure 4.16 FPGA simulations of the Σ-Δ modulator and modulus control.

Phase noise and spur level are the most important parameters of a synthesiser, which reflect the spectral purity performance. Figure 4.15 shows these two parameters at divide by 72 mode. The phase noise measurements throughout this work are taken by Agilent 85671A phase noise utility. The measured phase noise is −93 dBc/Hz and

−114 dBc /Hz at 1 kHz and 600 kHz offset respectively, and the spur level is below −58 dBc.

A Σ-Δ modulator (shown in Figure 3.24) is implemented by the FPGA XC2V1500 interface with a cascaded 18-modulus divider. The Σ-Δ modulator has 4-level output which allows the second 8/9 divider to divide by 9 constantly. The frequency divider divides the VCO input signal by 72, 73, 74 and 75, with an average value between 73 and 74. Figures 4.16 and 4.17 show the simulated and measured results. It is evident that the division values of the first prescaler is 8 or 9 for the modulus control of logic-1 or logic-0, respectively.

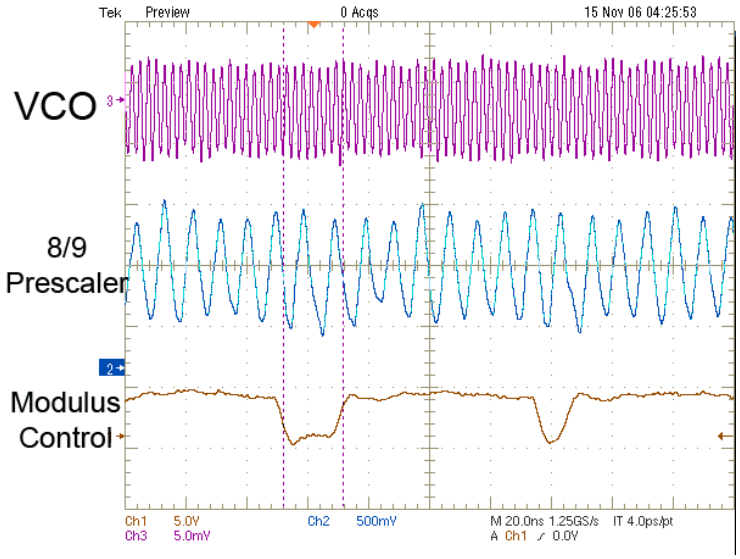


Figure 4.17 Measured output waveforms of VCO, 8/9 prescaler and modulus control signals.

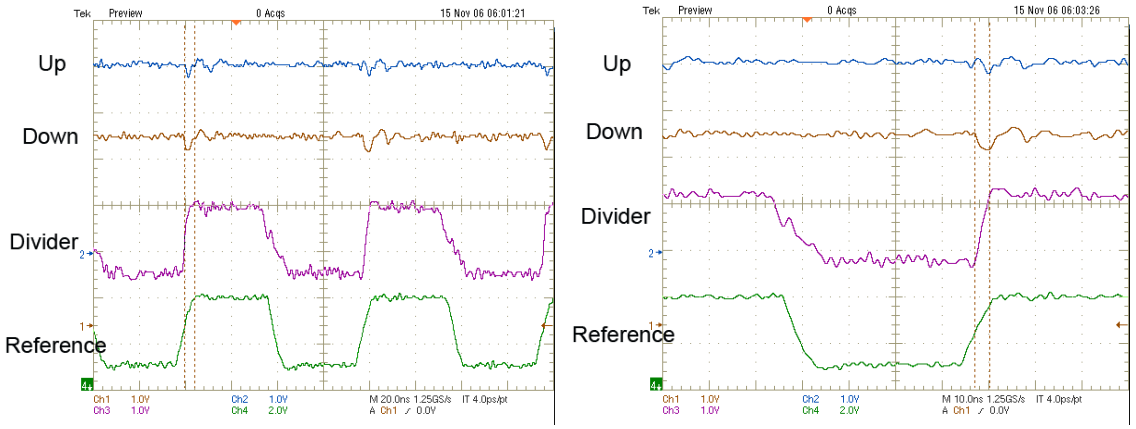


Figure 4.18 Measured input and output signals of the PFD in a locked loop.

Figure 4.18 shows the measured results of the PFD in a closed locked loop. The differential outputs carrying tiny pulses are the phase errors, which are converted to a voltage control signal by a suitable low pass loop filter. It adjusts the VCO to generate an expected stable frequency and also decides its phase noise level.

The frequency domain performance of each component is more important since some low amplitude noise is not measurable in the time domain. The measured noise shaping of the FPGA implemented Σ-Δ modulator is shown in Figure 4.19. These spectra are measured under a stable sampling frequency of 12.8 MHz equal to the reference frequency of the synthesiser. The FPGA generates a smooth noise shaping except that there is a high spur at 355 kHz frequency offset which is induced by the FPGA evaluation board because of signal coupling and non-ideal impedance matching.

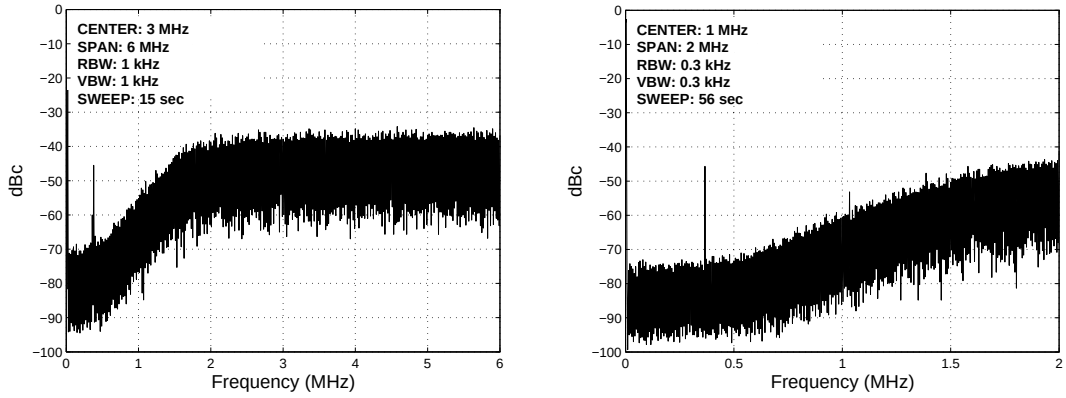


Figure 4.19 Measured noise shaping of the FPGA implemented Σ-Δ modulator.

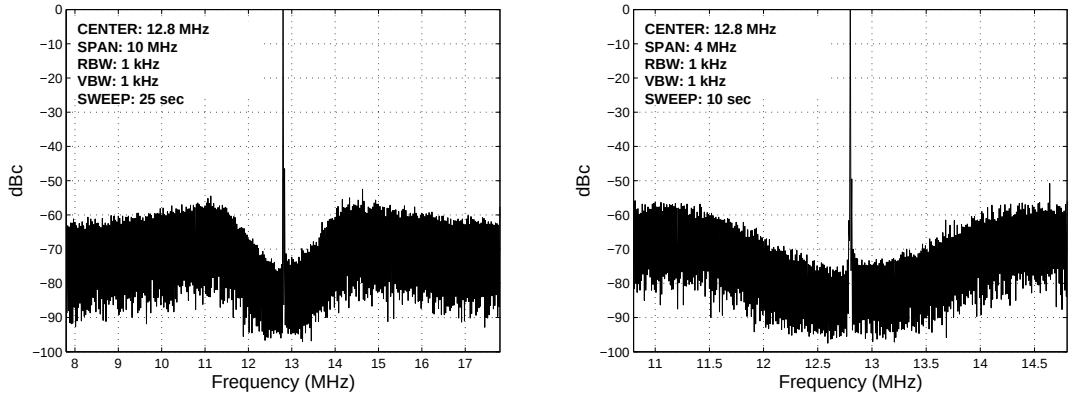


Figure 4.20 Measured output spectra of the frequency divider.

Figure 4.20 presents the measured output spectra of the frequency divider with a 940.3 MHz input frequency and an average division ratio of 73.46. It presents low close-in noise after the Σ-Δ modulator pushing the quantisation noise far from the signal. The outstanding quantisation noise at high frequency offsets will be suppressed by a low-pass loop filter in a closed loop.

The implemented fractional-*N* frequency synthesiser is tested when the fractionality of the Σ-Δ modulator is an example of 0.46. The output frequency is 73.46 times the reference frequency (12.8 MHz), 940.288 MHz, as shown in Figure 4.21. Figure 4.22 shows the measured phase noise, which is about −90 dBc/Hz from 1 kHz to 600 kHz offset.

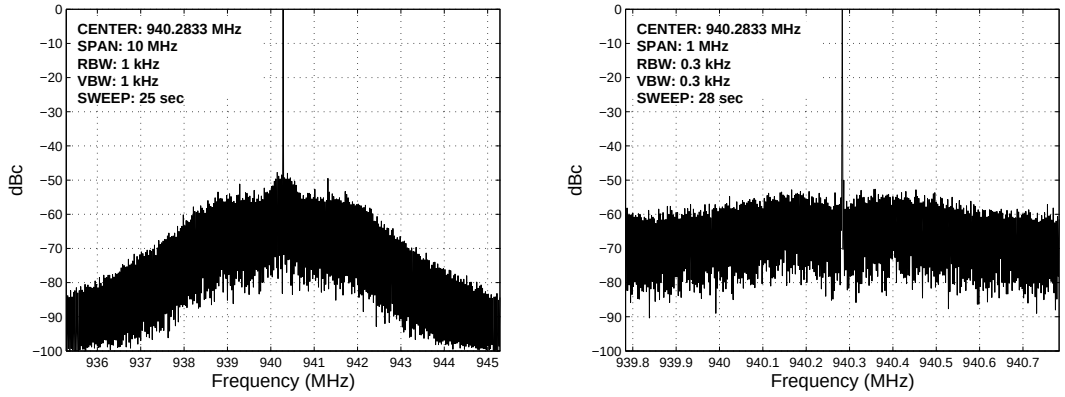


Figure 4.21 Measured spectra of the fractional-*N* synthesiser with 10 MHz span (left) and 1 MHz span (right).

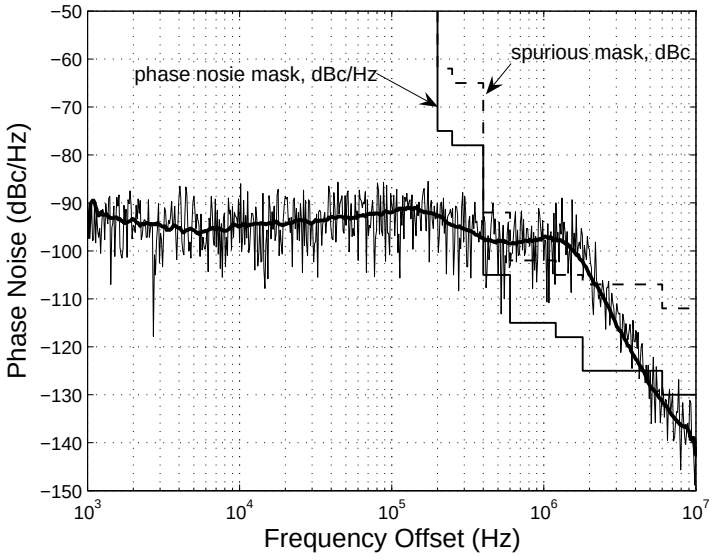


Figure 4.22 Measured phase noise of the fractional-*N* synthesiser.

Compared with an integer-*N* synthesiser, the phase noise does not decline from the loop natural frequency of about 250 kHz. The reason is that both the Σ-Δ modulator and the loop filter are third order. Hence the low pass loop filter response is a mirror of the quantisation noise characteristic, as shown in Figure 4.23 which displays simulated phase noise contribution of the Σ-Δ modulator and loop filter. The loop filter response slope is −40 dB/decade, and the high pass Σ-Δ noise shaping slope is 40 dB/decade. The phase noise should begin to decline until the corner frequency of the Σ-Δ modulator, reaches about 1.2 MHz offset, as presented in Figure 4.20. The phase noise characteristic can be re-shaped by using at least one order higher loop filter than the Σ-Δ modulator, indicating that using a second order Σ-Δ modulator or a fourth order loop filter.

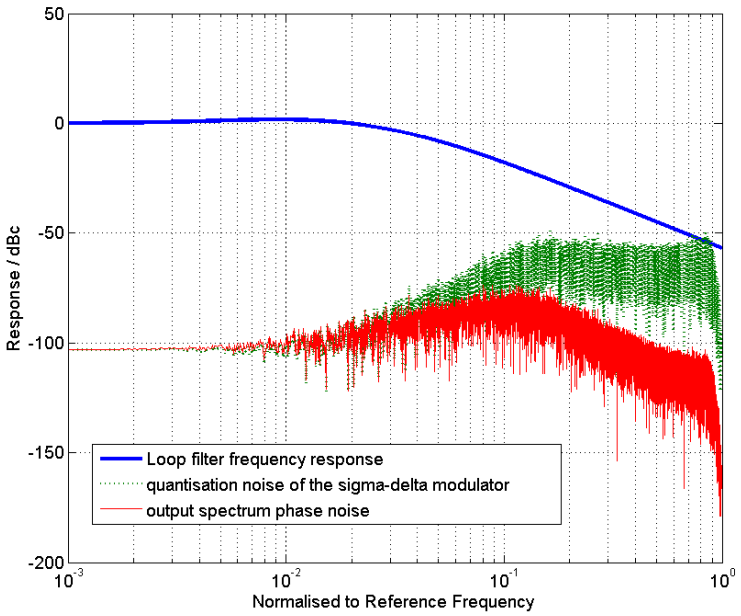


Figure 4.23 Simulated quantisation noise contribution to the synthesiser.

Because of the inverse relationship between phase noise and reference frequency as shown in equation (3.29), applications with higher reference frequencies would lead to lower PFD noise at the loop output. A substantial improvement in phase noise is thus possible by using a higher reference frequency. In addition, reference sidebands are normally completely outside the operating band of the synthesiser, leaving a clean in-band spectrum without reference spurs.

4.5 High Reference Frequency Fractional-N Synthesiser

Producing a lower phase noise synthesiser without the penalty of suppressing its bandwidth leads to a direct method of challenging the reference frequency, meaning that it demands the digital control block working at a sampling frequency as high as possible [90]. This is an easier way to obtain low in-band noise fractional-*N* synthesiser rather than refining the PLL architecture by introducing additional complicated circuitry. The design process and prototype architecture of the RF section are quite similar to the low reference frequency system (Appendix A). Its circuit diagram is shown in Figure 4.24 and a corresponding PCB photograph is displayed in Figure 4.25. A low noise signal generator HP 8642B is utilised to provide reference source for this synthesiser. The high output frequency of the divider results in challenges concerned with the FPGA speed. An extremely high frequency programmable divider type CENTELLAX UXM15P is used in this work because of the ideal division ratio and low phase noise, allowing a high reference frequency implementation to be tested to see the benefits on the Σ-Δ noise shaping. A further advantage of using a very high reference frequency is that reference sidebands are likely to be completely outside the operating band of the synthesier, which can be effectively suppressed by the low-pass loop filter.

The divider UXM15P has a quoted toggle frequency of 15 GHz at multi-modulus division mode with continuous integer divisions ratios from 4 to 9. Its input and output levels are the usual PECL standard with a swing of 1100 mV centred on 3.6 V and a similar AC coupling arrangement is used to that for the PFD. The SSB phase noise of the divider is −130 dBc/Hz at 10 Hz offset and −153 dBc/Hz at 10 kHz offset, which means that the divider will provide a very clean signal to the PFD and prompt to low noise performance in this application.

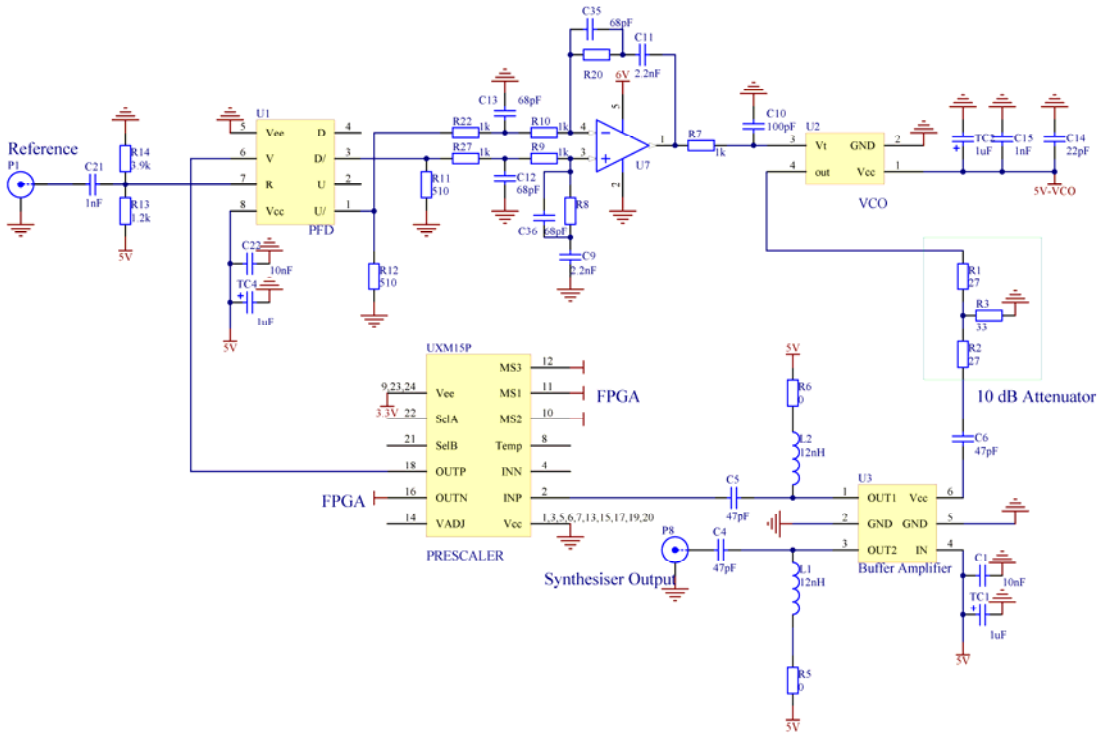


Figure 4.24 Circuit diagram of the implemented synthesiser.

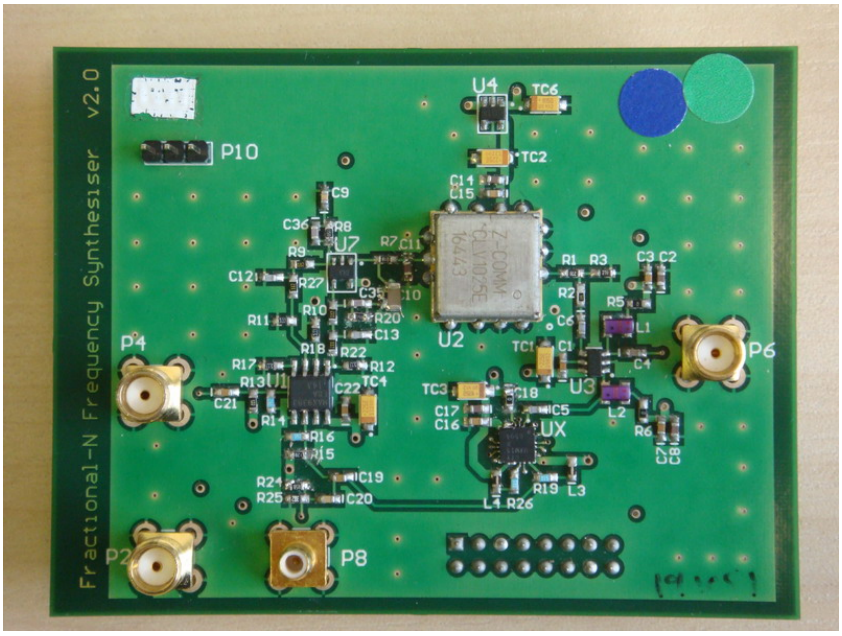


Figure 4.25 RF section of the high reference frequency fractional-*N* synthesiser.

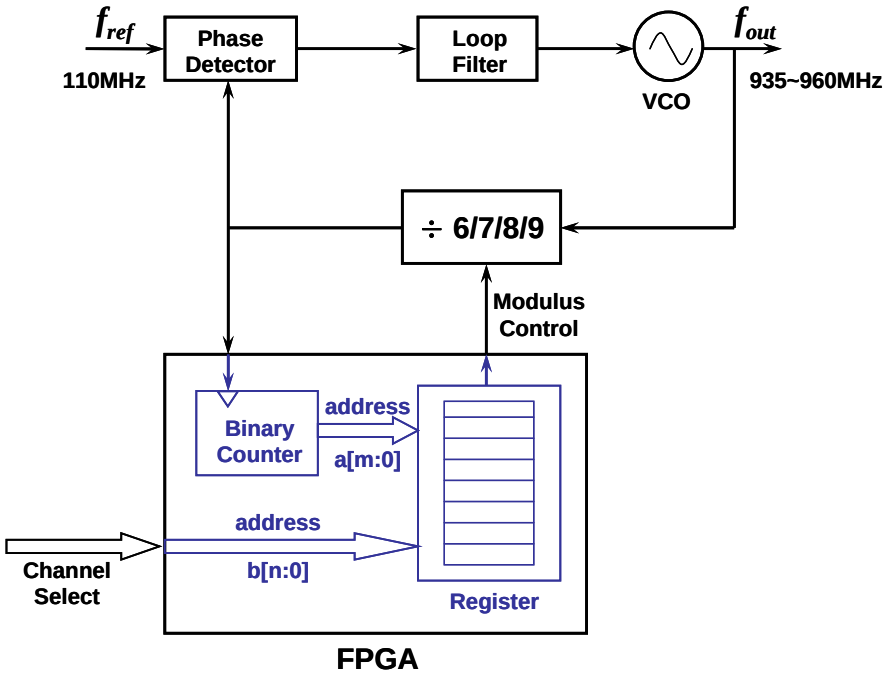


Figure 4.26 Block diagram of a stored-sequence fractional-*N* frequency synthesiser.

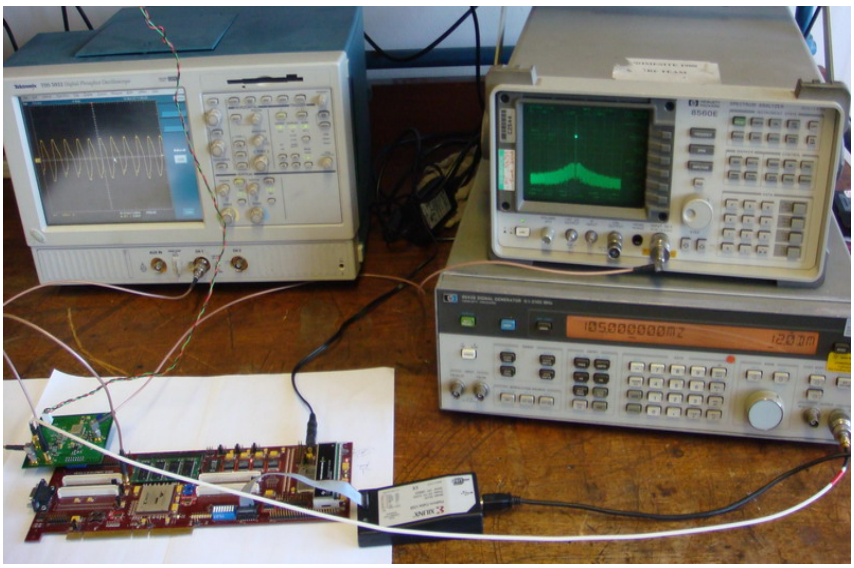


Figure 4.27 Experimental setup of the synthesiser measurement.

The Σ-Δ modulator is clocked by the divider output frequency. In low division ratio, high reference frequency synthesisers, the speed of the Σ-Δ modulator becomes a bottleneck of the system. The measured results reflect that Σ-Δ modulators directly implemented by an FPGA can work up to around 80 MHz depending on the architecture complexity. However, significant delays are unavoidable and they will eventually cause modulus control miscount. The stored-sequence technique [86, 87] is a valid method to

break the bottleneck of Σ-Δ modulator working speed. Its block diagram is shown in Figure 4.26 and the experimental setup is shown in Figure 4.27. The FPGA downloads a pre-generated program from a PC by a JTAG cable, then controls the loop to generate an accurate frequency. The spectrum is monitored by a spectrum analyser HP 8560E and the phase noise characteristics are measured by its built in Agilent 85671A phase noise utility.

The key feature of the stored-sequence architecture is that the Σ-Δ logic block is replaced by a counter and a ROM which act to clock out pre-generated Σ-Δ (or other) bitstreams. These bitstreams are generated off-line by simulation of a given Σ-Δ modulator. This approach allows the bitstreams to be individually optimised, on a channel-by-channel basis, possibly by modelling a number of entirely different Σ-Δ architectures, with no restriction to finite input resolutions.

The low division ratio allows suitable reference frequency to be chosen so the fractional component of the division ratio is close to 0.5 in the centre of the output frequency range, as this is likely to provide the best overall noise performance over the complete operating range.

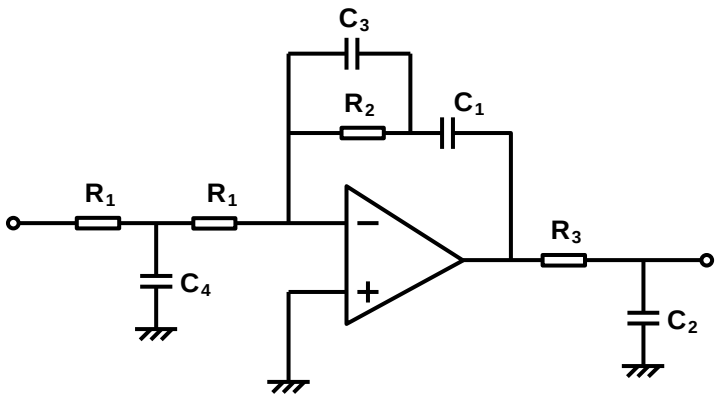


Figure 4.28 Enhanced loop filter design.

The enhanced loop filter design is as shown in Figure 4.28. Two first order RC filters (R_1, C_4 and R_3, C_2) are added to the third order type II loop filter to suppress op-amp noise and synthesiser out of band noise. The input resistor is splitted into two of equal value and then introducing a further pole into the transfer function. The extra thus introduced pole will degrade the phase margin of the loop filter by about 5°, which is in the permission range of the filter. The response of R_1, C_4 filtering is:

$$H_1(s) = \frac{\omega_1}{s + \omega_1} = \frac{1}{s \cdot R_1 \cdot C_4 + 1} \tag{4.8}$$

where $\omega_1 = \frac{1}{R_1 \cdot C_4}$, ω_1 is the cut-off frequency of the first order low pass filter. The value $\omega > 10\,\omega_n$ normally be used to ensure the stability of the system. R_3 and C_2 introduce an additional first order filter,

$$H_3(s) = \frac{1}{s \cdot R_3 \cdot C_2 + 1} \tag{4.9}$$

If $\omega_o = \frac{1}{R_3 \cdot C_2} = 20\omega_n$, as a normal value usually used in real circuit designs, natural frequency is $\omega_n = 1.57 \times 10^6$ rads/s, and other parameters of this filter are N = 7.5, R_1 = 1.1 kΩ, C_2 = 200 pF. This enhanced loop filter presents the same response as typical third order type II loops at low frequencies. The objective of this first order filter between loop filter and VCO is to provide even greater loop suppression at frequencies higher than the loop filter natural frequency. The transfer function of this filter at high frequencies is

$$G(s) = -\frac{1}{R_1} \cdot \frac{1}{sC_4R_1 + 2} \cdot \left(\frac{R_2}{sC_3R_2 + 1} + \frac{1}{sC_1} \right) \cdot \frac{1}{sC_2R_3 + 1} \tag{4.10}$$

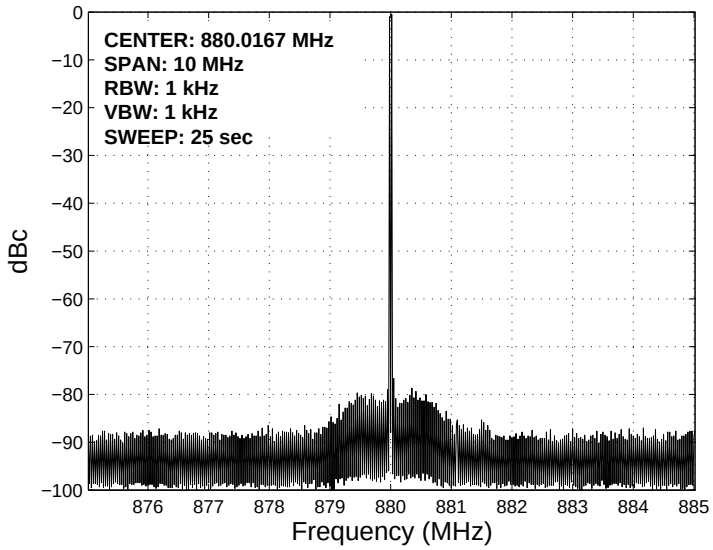


Figure 4.29 Measured spectrum of the synthesiser at integer mode.

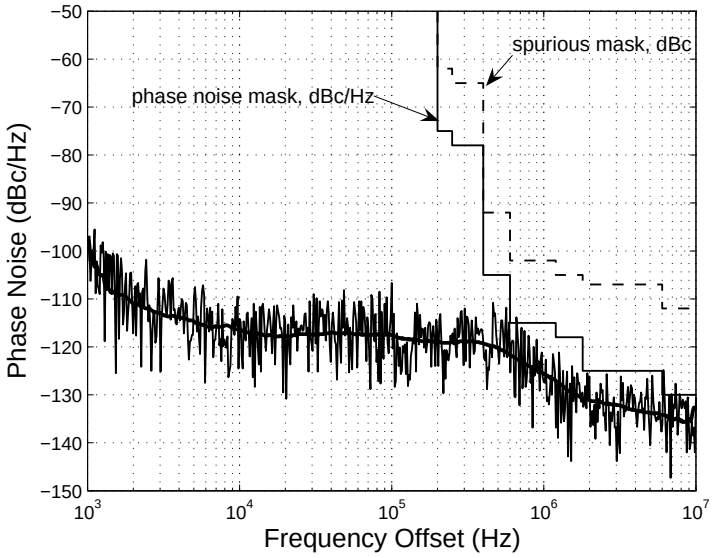


Figure 4.30 Measured phase noise of the synthesiser at integer mode.

The prototype is first tested under integer mode with 105 MHz reference frequency and the division ratio is 8. The output spectrum is without the contribution of Σ-Δ noise shaping and its central frequency is 840 MHz, as shown in Figure 4.29. Both the phase noise and spur level are within the satisfactory range, and the measured results are shown in Figure 4.30. The phase noise is −118 dBc/Hz at 10 kHz offset and −129 dBc/Hz at 1 MHz offset. No spur higher than −80 dBc over 10 kHz offset is visible.

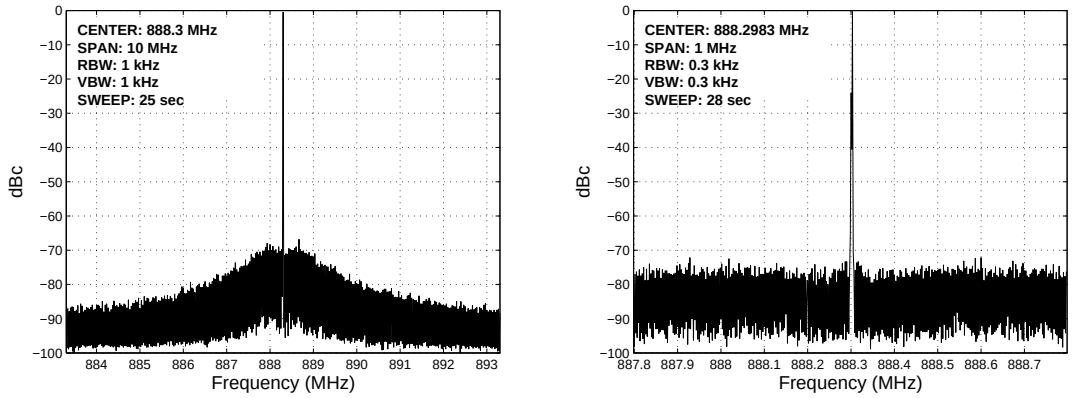


Figure 4.31 Measured fractional-*N* synthesiser output spectra.

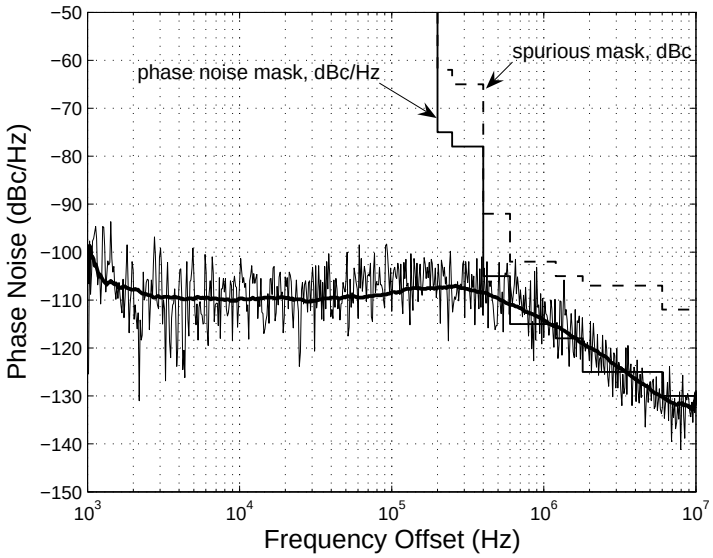


Figure 4.32 Measured phase noise of the fractional-*N* frequency synthesiser.

A second order and a third order single stage Σ-Δ modulators are simulated by MATLAB with an input fractionality of $943/2048+2^{-15}$. The modulators have been simulated 65536 samples to represent a cycle of the modulator dithering sequence without quantisation noise spectral leakage. The sequences are pre-stored in the internal memories of an FPGA, and clocked by the output of the frequency divider. Finer resolution Σ-Δ modulator input and longer sequences are obvious methods to evaluate noise shaping performance close to DC, but additional memories are necessary to store more pre-generated bitstreams.

If a 105 MHz reference frequency is employed, with an average division ratio of 8.46, the output spectrum is centred at 888.3 MHz. Figure 4.31 shows the measured spectrum

of the fractional-*N* synthesiser with a second order single-stage Σ-Δ modulator, and the VCO output frequency matches predicted result very well. Figure 4.32 shows the measured phase noise characteristic and spurious performance of the synthesiser working at the same channel/frequency. It is apparent that the cut-off frequency of the PLL response is about 250 kHz and the measured in-band phase noise is about −110 dBc/Hz.

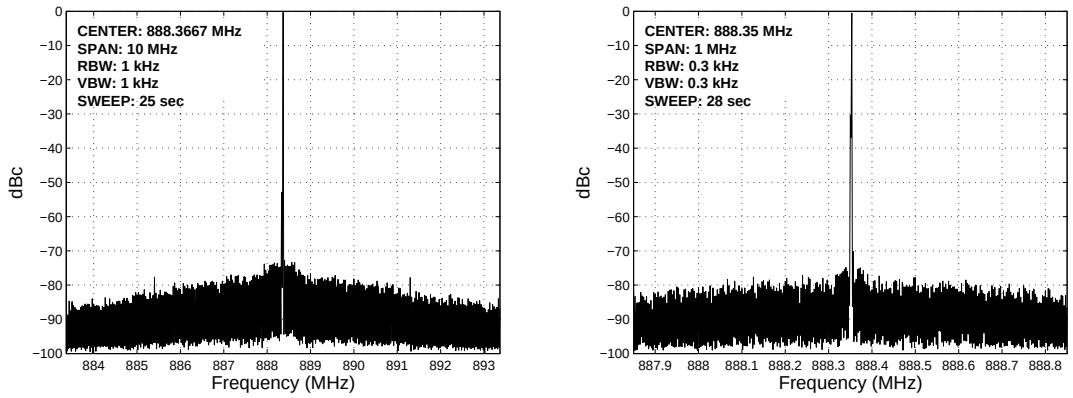


Figure 4.33 Measured fractional-*N* synthesiser output spectra.

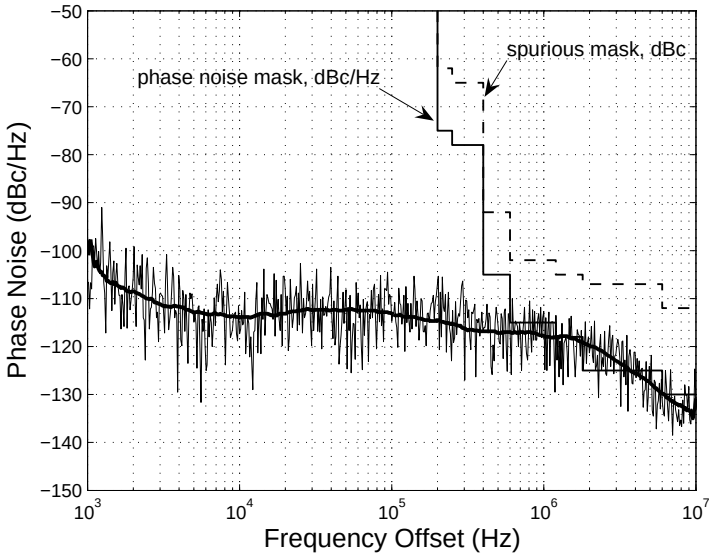


Figure 4.34 Measured phase noise of the fractional-*N* frequency synthesiser.

Table 4.2 Summary of Measured Performance.

PARAMETER	VALUE
VCO Gain	29 MHz/V
PFD Gain	0.159 V/rad
Bandwidth	265 kHz
Output Frequency Range	820 – 975 MHz
Reference Frequency	105 MHz
Minumun Frequency Resolution	< 100 Hz
In-band Phase Noise	–113 dBc/Hz
Switching Time	20 μs

Figure 4.33 shows the measured spectrum of the fractional-*N* synthesiser with a third order single stage Σ-Δ modulator, under the same conditions. Benefiting from the higher order high pass response of the Σ-Δ modulator, the close-in noise is further suppressed. Figure 4.34 shows the measured phase noise characteristic and spurious performance of this synthesiser, its in-band phase noise is about −113 dBc/Hz. However, it is quite difficult to find a cut-off frequency around 250 kHz offset and the noise floor exceeds the mask between 1.8 MHz and 4.5 MHz offsets. This is because that both the loop filter and the Σ-Δ modulator are third order, which results in inadequate suppression of noise floor at natural frequency offset. This demands a loop filter at least one order higher than the Σ-Δ modulator to effectively suppress phase noise beyond the natural frequency. A series of measured results show that, in the worst case, the synthesiser switches between any two channels in 20 μs. The specifications of this synthesiser is summarised in Table 4.2, which meet the requirments of GSM system listed in Table 1.1. The competitive phase noise and smooth spectra of the synthesiser can satisfy almost all RF system requirements, such as GSM/DCS, WiFi, WiMax. In addition, no additional circuitry is necessary to be applied to suppress noise, making a relatively simple architecture that can be implemented by a single FPGA and fundamental RF components, including a VCO, a loop filter, a PFD and a frequnecy divider. To demonstrate the quality of the presented fractional-*N* synthesiser, this work is compared to previously published fractional-*N* synthesisers in Table 4.3. A widely

used power-frequency-normalised (PFN) figure of merit (FOM) defined by Ham [91] is used.

$$PFN = 10\log\left[\frac{kT}{P}\left(\frac{f_o}{f_{off}}\right)\right] - L(f_{off}) \quad \text{(dB)} \tag{4.11}$$

where phase noise of a synthesiser measured at an offset f_{off} from a carrier at f_o is proportional to f_o^2 and inversely proportional to f_{off}^2 as well as power dissipated in the synthesiser P. PFN is unitless figure of merit expressed in dB and a larger PFN corresponds to a better synthesiser.

Table 4.3 Comparison of the presented Fractional-*N* synthesiser with recently published fractioanl-*N* synthesisers.

	[92]	**[93]**	**[94]**	**[95]**	**[96]**	**THIS WORK**
Implementation	Discrete	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	Discrete	Discrete
f_o	2.4 GHz	2.4 GHz	1.8 GHz	1.06 GHz	2.1 GHz	960 MHz
f_{ref} (MHz)	48	12	14.33	17.1	35	105
f_c (kHz)	460	730	400	35	200	250
Σ-Δ	3rd-order	2nd-order	3rd-order	3rd-order	3rd-order	3rd-order
In-band (dBc/Hz)	−96	−101	−98	−90	−103	−113
Spurs (dBc)	−66	-	-	−70	−55	−75
Settling (μs)	-	35	-	200	< 20	~8
FOM (dB)	−3.65	−1.03	−0.91	−30.32	−0.92	12.01

Benefiting from its low phase noise at 10 kHz offset, the designed synthesiser in this thesis has largest PFN, over 12 dB larger than other synthesisers. The power consumption of this synthesiser, about 280 mW, is much higher than the others. However, their phase noise are not at the same level which makes so different PFNs. This low noise synthesiser can be used in wireless base stations and some other

applications in which other fractional-*N* synthesiser designs are not able to satisfy low noise requirments.

It is worth noting that improper isolation of the PCB or components may result in some discrete spurs with a specify frequency separation related to the sequence repetition period. The main reason of causing these extra spurs is that the modulus control signal is phase modulated before being transmitted to the divider, which may raise the noise shaping level and affect the synthesiser output. However, the simulated noise shaping shows that the low frequency spurs are suppressed by the PLL response and are of very low amplitude that should not raise the in-band noise at all.

This work suggests that a stable amplitude, low noise and low distortion signal is important when it is used to control a frequency divider. This is because the noise carried by the modulus control signal is coupled onto the output of the divider and is transmitted to the synthesiser output without filtering, which means that the divider can not be considered as a simple digital component. The digital signal waveform distortion can be eliminated by introducing a comparator or buffer amplifier between the stored-sequence output and the modulus control input of the frequency divider, filtering the phase modulation effect and generating a signal with stable amplitude.

Chapter 5

Coupling and Intermodulation-Induced Spurs and Their Suppression

Although a low noise fractional-*N* synthesiser has been developed which shows smooth and continuous spectra on most channels as presented in chapter 4, a particular set of discrete spurious components, often referred as *fractional spurs*, emerge on some particular channels of the synthesiser and degrade its spectral purity. These spurious components are introduced, at least in part, by the modulation of the loop divider ratio and so various approaches have been employed to reduce such spurs, firstly analogue cancellation methods [97] and more recently the application of noise-shaping techniques such as Σ-Δ modulation. However, it is often the case that the close-in spur levels of fractional-*N* synthesisers are higher than desired, which is one of their major disadvantages in comparison to integer synthesisers. To date, these spurious components have, almost without exception, been solely attributed to the operation of the modulator and hence attempts at improving performance have concentrated on refining the design of the modulator. In recent work, we have reported an alternative natural mechanism [98-101], which results from the sampling of two non-harmonically related frequency components that are necessarily present in such synthesisers. This recently found mechanism is able to produce a family of spurs at exactly the same frequencies as these fractional spurs. This finding may be highly significant as it offers an explanation for the disappointing discrete spur performance so often observed in these synthesisers and a possible means of improving such performance.

The aim of this work is to investigate the exact role of this newly-discovered mechanism in the generation of fractional spurs. An analytic model has been developed to predict the potential intermodulation components resulting from the non-sampled, non-harmonically-related frequencies present in such a synthesiser and a numerical

model is further developed to determine the likely amplitude distribution of these components in a probable circuit scenario. The results from these models are then validated against experimental data for a number of synthesiser configurations, to determine both the presence and distribution of the predicted components and their likely significance in practical systems. An innovative phase compensation technique is then introduced to suppress at least part of these fractional spurs – in particular the most dominant sidebands. A generic module is successfully developed by coupling a small amount of controlled amplitude and phase VCO signal onto the phase/frequency detector input to cancel-out the potential intermodulation effect. The measured results demonstrate that the proposed technique can effectively suppress close-in sideband spurs and is therefore capable of enhancing spectral purity.

5.1 The Intermodulation Effect – General Description

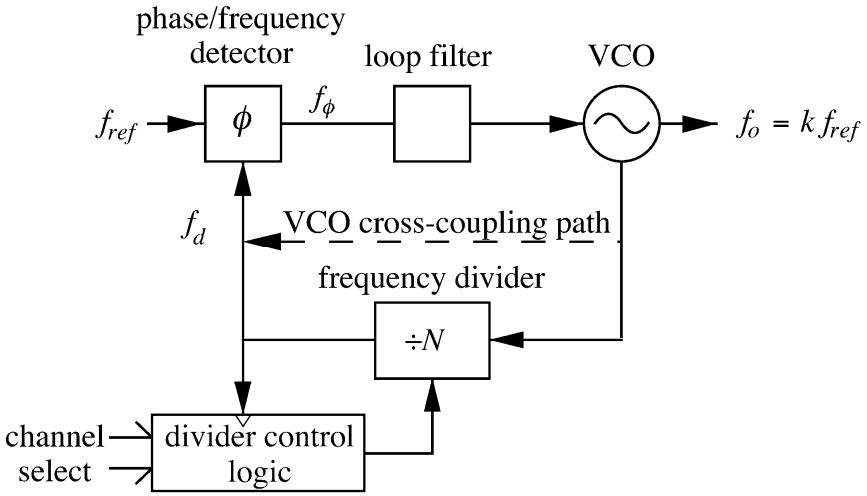


Figure 5.1 General form of a fractional-*N* frequency synthesiser, showing a VCO cross-coupling path.

Figure 5.1 shows the general arrangement of a fractional-*N* frequency synthesiser in which the output frequency is a non-integer multiple, k, of the reference frequency, f_{ref}, by means of a feedback path comprising a variable ratio frequency divider and associated control logic. This logic has the primary aim of achieving a fractional mean division ratio, k, by careful control of the divider over a range of integer values. Techniques such as Σ-Δ noise shaping have been developed to shape the quantisation

noise due to divider switching in order to reduce the noise in the vicinity of the fundamental component of the divider output, and so reduce the synthesiser close-in phase noise and discrete spurious components.

It is clear that there are two principal frequencies in this system: f_{ref} and kf_{ref}. If these are simultaneously present at any point in the loop then intermodulation may result. There are three possible points where intermodulation between the reference frequency and the VCO frequency may occur and degrade the synthesiser spectral purity: the frequency divider input, the PFD input and the VCO tuning input. The cross-coupling effects at both the VCO input and the divider input have been proven to mainly give rise to reference spurs, but contribute very little to the in-band noise [100]. The reference spurs can be effectively suppressed by the low-pass loop filter of the synthesiser. Previous research shows that the cross-coupling from the VCO output to the phase-detector input makes a major contribution to discrete spurs [101] and this is illustrated in Figure 5.1. For this case, where signals of fundamental frequency f_{ref} and kf_{ref} are simultaneously present at the phase detector input, the potential intermodulation frequencies [102] are thus given by

$$f_d = f_{ref}\left(m \pm kn\right) = f_{ref}\left(m \pm n\left(N + \alpha\right)\right) \tag{5.1}$$

where m and n are integers and $(N + \alpha) = k$ is the division ratio, with N the integer and α the fractional component, the so-called *fractionality*. These intermodulation products are presented to a phase/frequency detector, commonly used in PLL synthesisers [103], which acts as a reasonable approximation to an impulse sampler at the reference frequency and thus aliases all frequency components to the range $[-f_{ref}/2 \;\; f_{ref}/2]$. This aliasing process may be represented by the following expression which gives the aliased intermodulation frequencies appearing at the phase detector output.

$$f_\phi = f_{ref}\left[\frac{f_d}{f_{ref}} - \text{round}\left(\frac{f_d}{f_{ref}}\right)\right] \equiv f_{ref}\left[m \pm n(N+\alpha) - \text{round}\left(m \pm n(N+\alpha)\right)\right] \tag{5.2}$$

where the "round" function rounds to the nearest integer. Now, since $m \pm nN$ is always an integer and f_ϕ is bound (by sampling) to the range $\pm f_{ref}/2$, then equation (5.2) reduces to

$$f_\phi = f_{ref}\left[n\alpha - \text{round}(n\alpha)\right] \tag{5.3}$$

where the dependence on m and N is lost in the aliasing process and so the potential intermodulation frequencies are purely a function of the fractionality, α. These intermodulation components are present at the phase detector output and are thus capable of modulating the VCO and producing discrete spurious components on the synthesiser output. Consideration of equation (5.2) leads to the conclusion that a number, p, of intermodulation products exist, uniformly distributed over the range $[-f_{ref}/2 \;\; f_{ref}/2]$ as given by the minimum integer value of p satisfying

$$p\alpha = \text{integer} \tag{5.4}$$

with corresponding frequency separation

$$\Delta f = f_{ref} / p \tag{5.5}$$

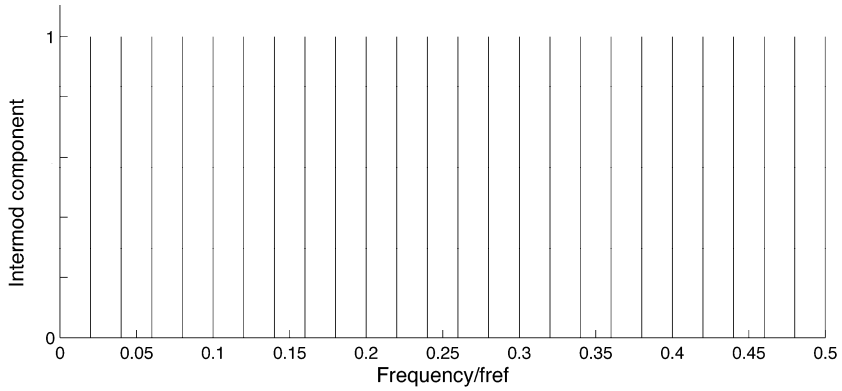


Figure 5.2 Potential components in a fractional-*N* synthesiser due to VCO/reference frequency intermodulation, with 0.46 fractionality.

Inspection of equations (5.4) and (5.5) reveals that, in the worst case, these components may have frequency separations equal to the desired channel spacing, which is a situation identical to an integer frequency synthesiser. As an example, taking a fractionality, a, of 0.46 it is found, from (5.4) and (5.5), that there are 50 potential intermodulation frequencies, separated by $f_{ref}/50$ and uniformly distributed between $-f_{ref}/2$ and $f_{ref}/2$, as shown in Figure 5.2. This analysis has demonstrated the potential

frequency components that may be produced by this mechanism, but is unable to predict their amplitudes or likely significance; however these matters are addressed in the following section.

5.2 Spur Distribution Analysis and Amplitude Prediction

5.2.1 Numerical Simulation

Referring again to Figure 5.1, a simple scenario is for a small amount of the VCO signal to cross-couple onto the divider output and/or either phase detector input. A certain amount of such cross-coupling is virtually inevitable in practice through a variety of paths such as cross-talk between PCB tracks, power supply coupling and leakage paths in the frequency divider. Considering, for simplicity, coupling onto the fundamental component of the divider output, which is at the reference frequency in a locked loop, then the effect of adding a smaller signal originating from the VCO of relative amplitude C and relative frequency k is to introduce timing jitter which can be readily quantified, as shown in the rather exaggerated illustration of Figure 5.3. It is clear that this timing jitter sequence repeats at the lowest common multiple of the reference and VCO periods, an identical conclusion to that of equation (5.4). Referring to Figure 5.3, it is evident that the timing jitter, Δt_n, at each sampling instant, n, can be deduced by solving the following equation

$$\sin\left(2\pi\Delta t_n / T_{ref}\right) + C\sin\left[2\pi k\left(n + \frac{\Delta t_n}{T_{ref}}\right)\right] = 0 \tag{5.6}$$

Writing the phase jitter at sampling instant n as $\phi_n = 2\pi\Delta t_n/T_{\text{ref}}$, then equation (5.6) becomes

$$\sin\phi_n = -C\sin\left(k\phi_n + 2\pi kn\right) \tag{5.7}$$

This expression may be solved iteratively, using Newton's iteration method with an estimated initial value [104]:

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \tag{5.8}$$

This method can find the phase jitter sequence over a complete cycle of duration pT_{ref} comprising p values for ϕ_n. It can be shown that the peak phase jitter value (assuming $k >> 1$) is in fact equal to C. An example of such a phase jitter sequence is given in Figure 5.4, for a division ratio, k, of 90.46 and a VCO cross-coupling ratio, C, of 0.01 or −40 dB. There is clearly a cyclic variation in phase, repeating every 50 reference periods, with a particularly strong fourth harmonic component at 0.08 times the reference frequency. The peak phase deviation is equal to 10 mrads, which seems rather small, but since this is magnified by the loop gain, k, within the PLL loop filter bandwidth then it may have a considerable effect at the synthesiser output.

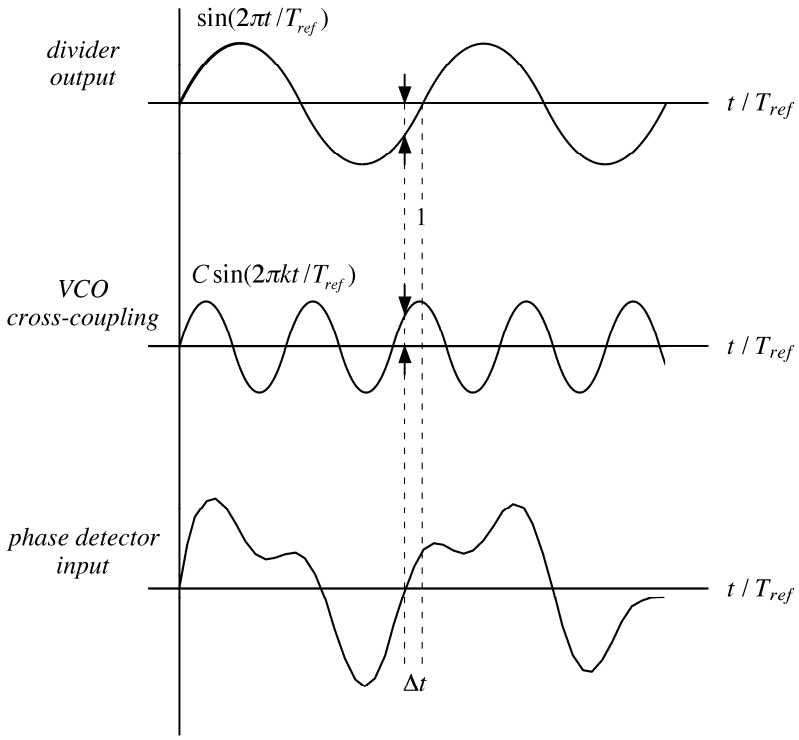


Figure 5.3 Illustration of the effect of VCO cross-coupling onto the phase detector input.

By means of a Fourier series expansion, the complex amplitudes, Φ_v, of the p frequency components of this phase jitter sequence may be readily found as follows

$$\Phi_v \,|_{v=1}^{p} = \frac{1}{p}\sum_{n=1}^{p}\phi_n \exp\left(-j\frac{2\pi nv}{p}\right) \tag{5.9}$$

This result gives the phase jitter frequency components referred to the phase detector due to the proposed VCO cross-coupling and sampling mechanism. The spurious component distribution on the VCO output is obtained by applying the PLL closed-loop response, which of course takes account of the multiplication factor *k* of the frequency divider and the loop filter characteristic. A fractional-*N* frequency synthesiser for DCS-1800 base station application is considered by way of example, including a third order type II loop filter, to deduce the spurious component distribution on the VCO output. The simulation is set up as an ideal linearised PLL model, and all noise sources other than the intermodulation components are assumed to be zero.

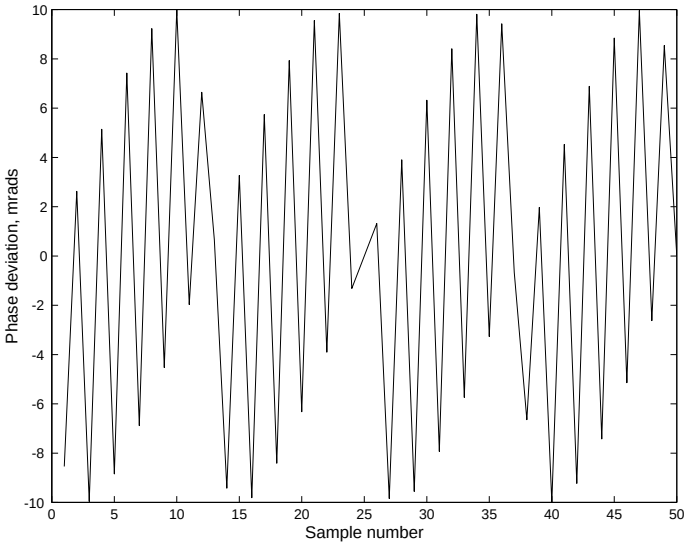
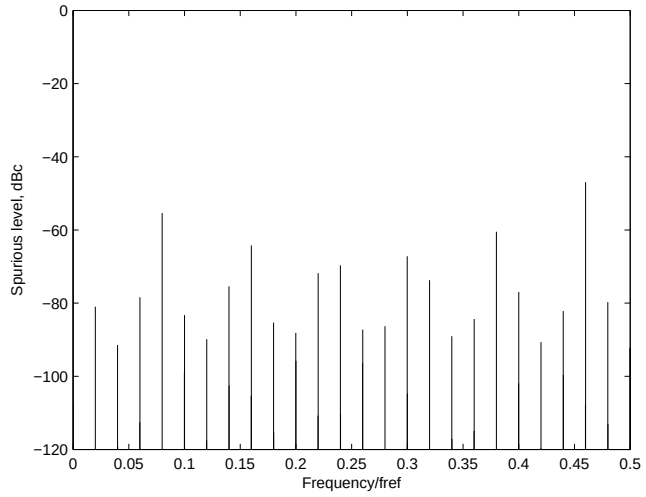


Figure 5.4 Modelled phase jitter resulting from −40 dB VCO cross-coupling with 90.46 divider ratio.

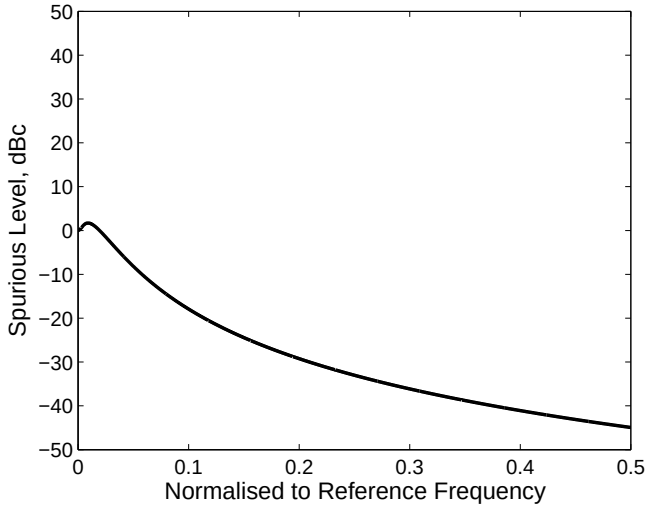
The simulation starts with a division ratio of 90.46 and a reference frequency of 20 MHz, resulting in VCO output frequency around 1809.2 MHz. The spur distribution is shown in Figure 5.5, including the PLL response with a 250 kHz natural frequency loop filter. It is obvious that there are 50 spurious components equally distributed within the 20 MHz reference frequency with a frequency interval of $0.02f_{ref}$. Figure 5.5 indicates the result for a DCS application with a VCO cross-coupling ratio, *C*, of −40 dB. It is clear, by comparison with Figure 5.2, that spurious components exist at all of the frequencies identified in the previous analysis − with spacing of $0.02f_{ref}$ or

400 kHz and with the largest component at $0.08f_{ref}$ or 1.6 MHz offset from carrier, as suspected from Figure 5.4. Their amplitudes are very variable as might be expected, not least due to the action of the loop filter, but they are highly significant, lying between −113 dBc and −38 dBc.

In Figure 5.6 the modelling is repeated but with the VCO cross-coupling reduced to −60 dB. The spur distribution is now very different with just two significant spurs at levels of −75 dBc and −77 dBc, which are still large enough to be measurable and possibly cause concern. Since coupling from the VCO to the phase detector inputs can occur in a practical circuit through a variety of paths then it is clear that the effect considered here is likely to be an important cause of fractional-*N* spurious components in many situations. The level of these components is dependent on the division ratio, and so synthesisers with lower reference frequencies are more susceptible to this behaviour. It is important to appreciate that, since the mechanism considered here occurs outside the frequency divider, then the vulnerability of fractional-*N* synthesisers to this phenomenon applies regardless of the purity of the modulator and the overall fractional-spur distribution will be the vector combination of the components described here and the modulator-borne components.



(a)



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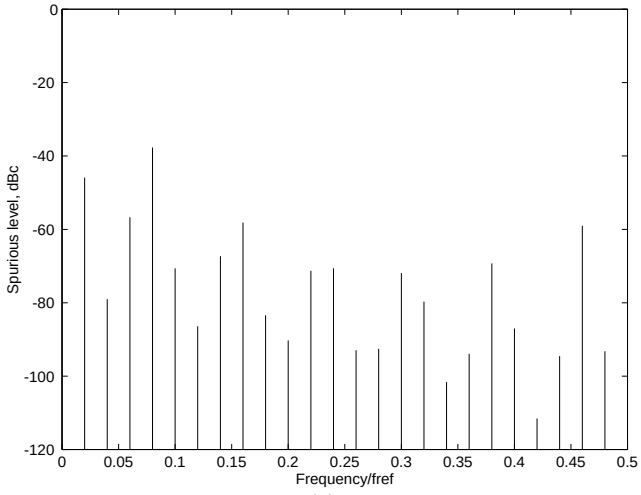


(c)

Figure 5.5 Numerically-predicted spurious components due to −40 dB VCO-phase detector cross-coupling in a fractional-*N* synthesiser; output frequency = 1809.2 MHz, reference frequency = 20 MHz, loop natural frequency = 250 kHz. (a) Spur distribution at phase detector input. (b) PLL response. (c) Spur distribution at synthesiser output.

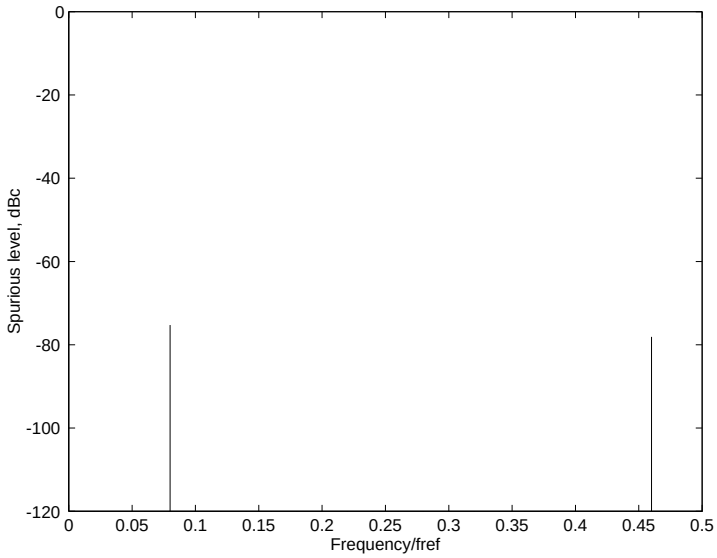


Figure 5.6 Numerically-predicted spurious components due to VCO-phase detector cross-coupling in a fractional-*N* synthesiser; output frequency = 1809.2 MHz, reference frequency = 20 MHz, loop natural frequency = 250 kHz, VCO cross-coupling = –60 dB.

5.2.2 Analytic Method

For relatively low levels of cross-coupling, the method described in section 5.2.1 can be approximated to an analytic expression for the phase jitter, as follows.

If $C << 1$, an approximate solution of equation (5.7) may be attempted in which ϕ_n is expressed as a series in powers of C, given by

$$\phi_n = Cp_n + C^2 q_n + C^3 r_n + \ldots \tag{5.10}$$

Each side of equation (5.7) may be expanded as a series in powers of C and the coefficients in the resulting equation may be equated. Using the Maclaurin series for the sine and cosine functions results in the following expressions:

$$\begin{aligned} \sin\phi_n &= \sin\left(Cp_n + C^2 q_n + C^3 r_n + \ldots\right) \\ &= \left(Cp_n + C^2 q_n + C^3 r_n + \ldots\right) - \frac{1}{3!}\left(Cp_n + C^2 q_n + C^3 r_n + \ldots\right)^3 + \ldots \\ &= Cp_n + C^2 q_n + C^3\left(r_n - \frac{1}{6}p_n{}^3\right) + \ldots \end{aligned} \tag{5.11}$$

and

$$\begin{aligned}
&C\sin\left(k\phi_n + 2\pi kn\right) \\
&= C\left[\sin\left(kCp_n + kC^2q_n + ...\right)\cos\left(2\pi kn\right) + \cos\left(kCp_n + kC^2q_n + ...\right)\sin\left(2\pi kn\right)\right] \\
&= C\left[\left(kCp_n + kC^2q_n + ...\right)\cos\left(2\pi kn\right) + \left(1 - \frac{1}{2}k^2C^2{p_n}^2 + ...\right)\sin\left(2\pi kn\right)\right] \\
&= C\sin\left(2\pi kn\right) + kC^2p_n\cos\left(2\pi kn\right) + C^3\left(kq_n\cos\left(2\pi kn\right) - \frac{1}{2}k^2{p_n}^2\sin\left(2\pi kn\right)\right) + ..
\end{aligned} \tag{5.12}$$

Substituting equations (5.11) and (5.12) into equation (5.7) and equating terms of the same order on each side, working up to order C^3, gives

$$p_n = -\sin\left(2\pi kn\right) \tag{5.13}$$

$$q_n = -kp_n\cos\left(2\pi kn\right) \tag{5.14}$$

and

$$r_n - \frac{1}{6}{p_n}^3 = -kq_n\cos\left(2\pi kn\right) + \frac{1}{2}k^2{p_n}^2\sin\left(2\pi kn\right) \tag{5.15}$$

By substituting for p_n in equation (5.14) and for p_n and q_n in equation (5.15), after some algebra and use of trigonometric identities, it is found that

$$q_n = \frac{1}{2}k\sin\left(4\pi kn\right) \tag{5.16}$$

and that

$$r_n = \frac{1}{8}\left(k^2 - 1\right)\sin\left(2\pi kn\right) - \frac{1}{24}\left(9k^2 - 1\right)\sin\left(6\pi kn\right) \tag{5.17}$$

Thus, from equations (5.7), (5.13), (5.16) and (5.17), it is apparent that ϕ_n is approximated by the Fourier series

$$\phi_n = -C\sin\left(2\pi kn\right) + \frac{1}{2}C^2k\sin\left(4\pi kn\right) - \frac{1}{24}C^3\left(9k^2 - 1\right)\sin\left(6\pi kn\right) \tag{5.18}$$

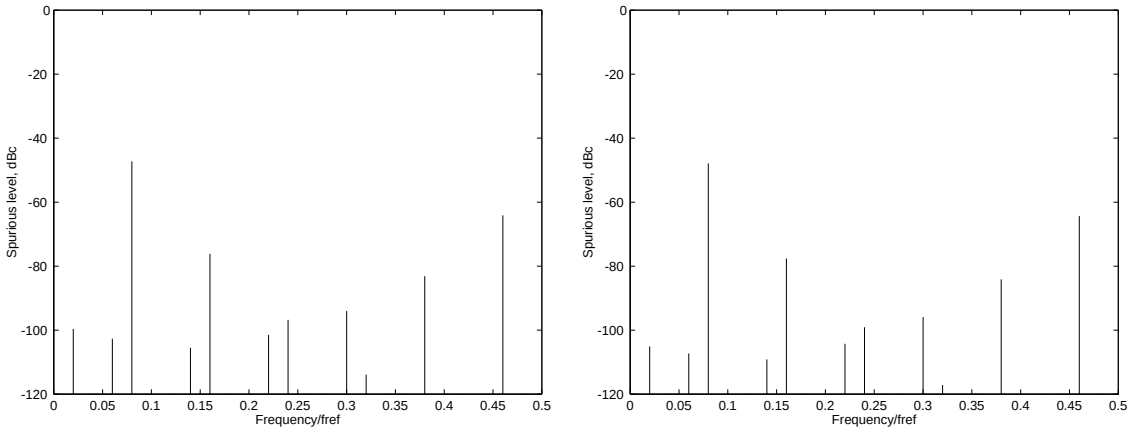
to order C^3, where lower-order correction to the $\sin(2\pi kn)$ term has been neglected. This expansion is in fact a series in powers of kC, so that this product should satisfy $kC << 1$ to obtain an accurate approximation.

The expansion in equation (5.18) can of course be extended (with increasing algebraic complexity) to include terms with higher powers of C. A further simplification can be made by noting that at each order of C the terms with the highest powers of k dominate if $k >> 1$. Retaining only such terms, it is found that the coefficients of $\sin(2m\pi kn)$ for $m = 1, 2,\ldots$ in ϕ_n follow a remarkably simple formula and so equation (5.18) may be simplified to the following result for the phase jitter sequence

$$\phi_n \approx -C\sum_{m=1}^{\infty}\frac{(-mCk/2)^{m-1}}{m!}\sin(2m\pi kn) \tag{5.19}$$

The series in equation (5.18) converges if $Ck < 2/e \approx 0.736$, giving an upper bound on Ck for this approach to be valid.

The analytic method described here is an alternative to the numerical method given in section 5.2.1 and avoids the need for an iterative technique to find the phase jitter at the phase detector input. Figure 5.7 shows a comparison of results derived using both analytic and numerical approaches, with the analytic method being in the valid range ($C = 0.005$ and $Ck = 0.45$). The two methods yield very similar results in terms of both the frequency and distribution of spurious components, although the analytic technique tends to slightly overestimate the value of some of the smaller spurs. The two methods predict the peak spurious level, in this example, to an agreement of within 0.6 dB. This shows that the analytic method described here is a viable alternative for low to moderate degrees of VCO cross-coupling and/or synthesisers with low division ratios.



(a) (b)

Figure 5.7 Comparison of analytic (a) and numerical (b) predicted spurious components due to VCO-phase detector cross-coupling in a fractional-*N* synthesiser; output frequency = 1809.2 MHz, reference frequency = 20 MHz, loop natural frequency = 250 kHz, VCO cross-coupling = −46 dB.

5.2.3 Stability Threshold

At very high VCO cross-coupling levels it is possible for the loop to lose lock. The explanation is apparent from Figure 5.8, which shows the case of a sufficiently high degree of VCO cross-coupling to cause an additional pair of zero-crossings in the combined signal. In a PLL context, this would cause false triggering of the phase-frequency detector and hence large phase errors in the loop. The threshold at which this event occurs may be found by considering a cross-coupling ratio, C, which is just sufficient to cause an additional zero-crossing at time t_1. At this point the sum of the reference signal and the cross-coupled VCO signal is zero, and the slope of the sum is also zero, giving

$$\begin{cases} \sin\left(2\pi f_{ref} t_0\right) + C\sin\left(2\pi f_{ref} t_0 + \phi_0\right) = 0 \\ 2\pi f_{ref}\cos\left(2\pi f_{ref} t_0\right) + 2\pi f_{ref} C\cos\left(2\pi f_{ref} t_0 + \phi_0\right) = 0 \end{cases} \tag{5.20}$$

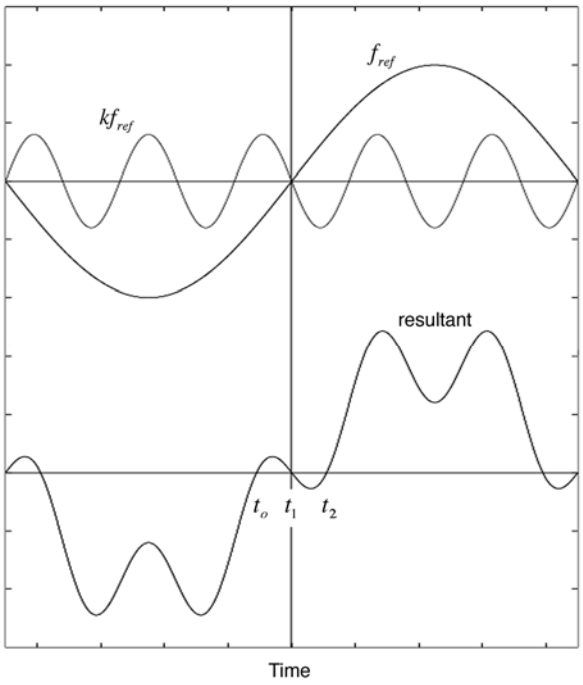


Figure 5.8 Illustration of excessive VCO-to-phase detector cross-coupling leading to loop instability.

By squaring both sides of equation (5.20) and eliminating $\sin(2\pi f_{ref}t_0)$, this condition reduces to

$$1-k^2C^2\cos^2(2\pi kf_{ref}t_0+\phi_0)=C^2\sin^2(2\pi kf_{ref}t_0+\phi_0) \tag{5.21}$$

Substituting $\sin^2(2\pi\, kf_{ref}t_0 + \phi_0)$ with $1-\cos^2(2\pi\, kf_{ref}t_0 + \phi_0)$, gives

$$C^2+(k^2-1)C^2\cos^2(2\pi kf_{ref}t_0+\phi_0)=1 \tag{5.22}$$

The most demanding constraint on the coupling ratio exists when $\cos(2\pi kf_{ref}t_0 + \phi_0) = 1$, from which it is apparent that to avoid instability the following very simple condition is necessary

$$Ck \le 1 \tag{5.23}$$

and this defines the stability threshold; if Ck should exceed 1 then instability would result. However, in the range of $e/2 \le Ck \le 1$, the synthesiser has stable output although cross-coupling spurs are very high (higher than −20 dBc), and the analytic method is no longer valid to predict spur distributions.

5.3 Comparison with Modelled and Measured Results

A typical single-stage third order feedback Σ-Δ modulator, as shown in Figure 3.27, is used to control the divider of a fractional-*N* synthesiser. The input value, ranging from 0 to 1, sets the mean division ratio and hence the fractional component of division ratio, α. This modulator, with weights of $A = -8$ and $B = -16$, has been modelled [86], using MATLAB, in conjunction with a PLL frequency synthesiser containing a third order loop filter and with the same parameters as the DCS application considered in Figures 5.6 and 5.7. The resulting SSB phase noise profile, shown in Figure 5.9, exhibits a noise characteristic typical of a synthesiser of this kind, with high-pass noise shaping close to the carrier tempered by the low-pass loop response, along with clear evidence of discrete fractional spurs. By comparison with Figure 5.6, describing the spurious components resulting from the new mechanism proposed in this chapter, it is evident that the fractional spurs exist at exactly the same frequencies (i. e. uniformly spaced by $0.02f_{ref}$) and furthermore their distributions are also quite similar, which is not necessarily to be expected as the two results are produced by entirely different mechanisms. This suggests that the spurs produced by the VCO cross-coupling and sampling mechanism are virtually indistinguishable from those produced by a typical Σ-Δ modulator and, hence, it would be very easy to wrongly attribute such spurs to the modulator. The magnitude of the fractional spurs produced by the Σ-Δ modulator is actually slightly less in this instance than that predicted of −40 dB VCO cross-coupling, suggesting that this degree of VCO-to-phase detector cross-coupling would significantly degrade performance.

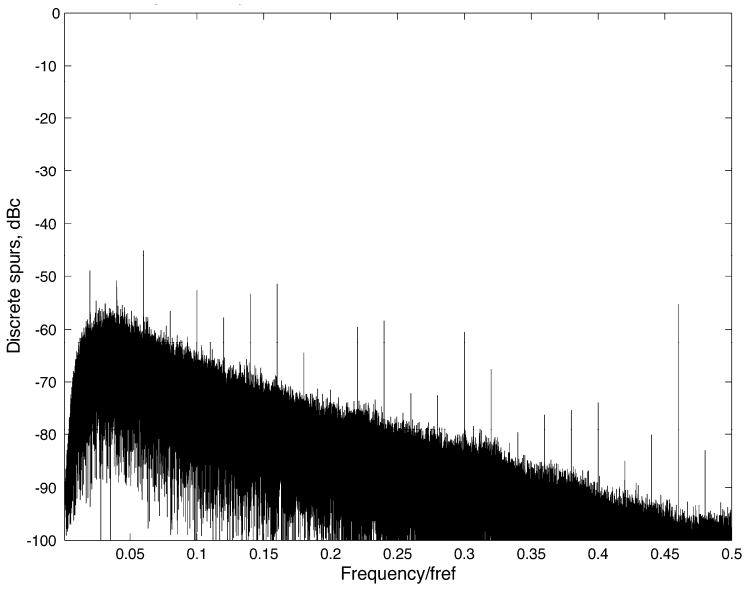
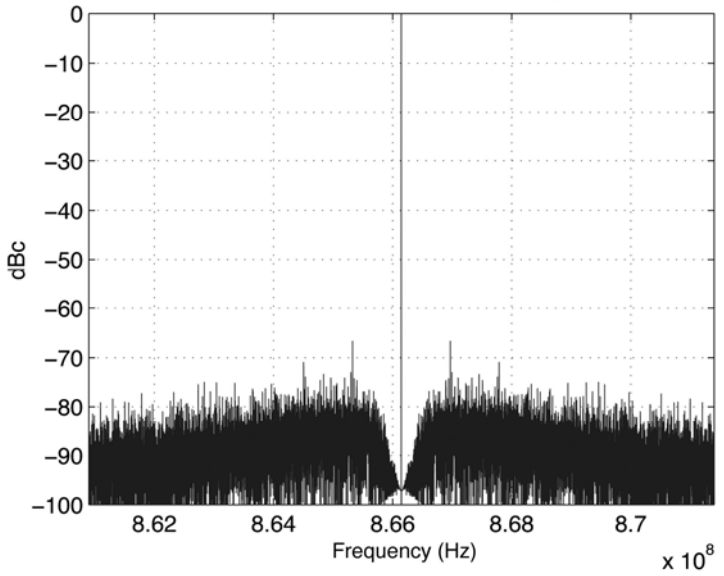


Figure 5.9 Numerically-modelled VCO phase noise profile for a fractional-*N* synthesiser, output frequency = 1809.2 MHz, reference frequency = 20 MHz, loop natural frequency = 250 kHz, no VCO cross-coupling.

In order to determine whether VCO-to-phase detector cross-coupling produces the effects suggested by our modelling an experiment has been conducted with a test synthesiser arrangement in which a controlled amount of VCO signal is coupled onto the phase detector input, in a very similar manner to that depicted in Figure 5.1, and the resulting VCO spectra recorded by a spectrum analyser. The synthesiser used in these measurements is the same as in section 4.4, with a 250 kHz third order loop filter, a reference frequency of 105 MHz and operation around 890 MHz, corresponding to a particularly low division ratio of approximately 8.5. Figures 5.10 to 5.14 show the outcome of these measurements.

Figure 5.10 gives the simulated and measured spectra with an output frequency of 866.1475 MHz, corresponding to 255/1024 fractionality. The simulated result, in Figure 5.10(a), takes account only of noise contributions from Σ-Δ modulator noise and loop filter behaviour. Thermal noise and flicker noise are not taken into consideration because they are not relevant to the effect considered here. This is why the measured spectrum, in contrast to the modelled result, exhibits a "skirt" effect close the carrier. The modelled result shows one or two visible discrete spurs at −66 dBc and −72 dBc. The corresponding measured result shows a very similar phase noise profile though with rather higher close-in spurs having a maximum value of −48 dBc at 410 kHz offset.



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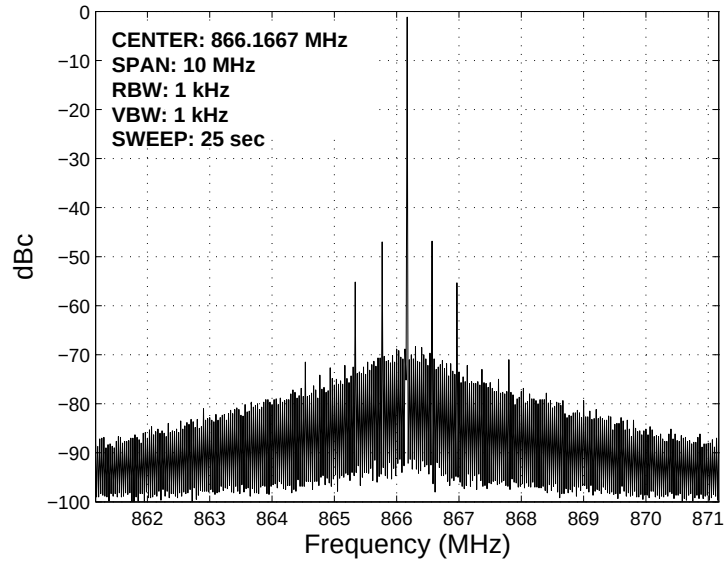
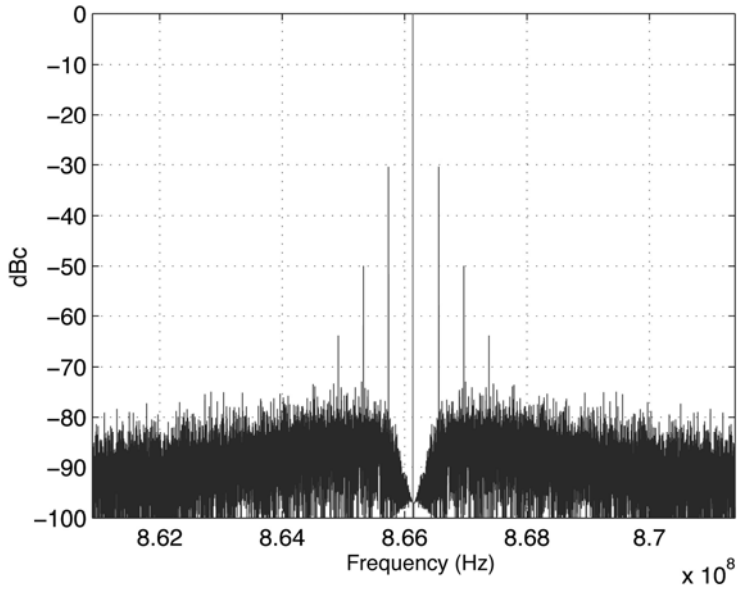


(b)

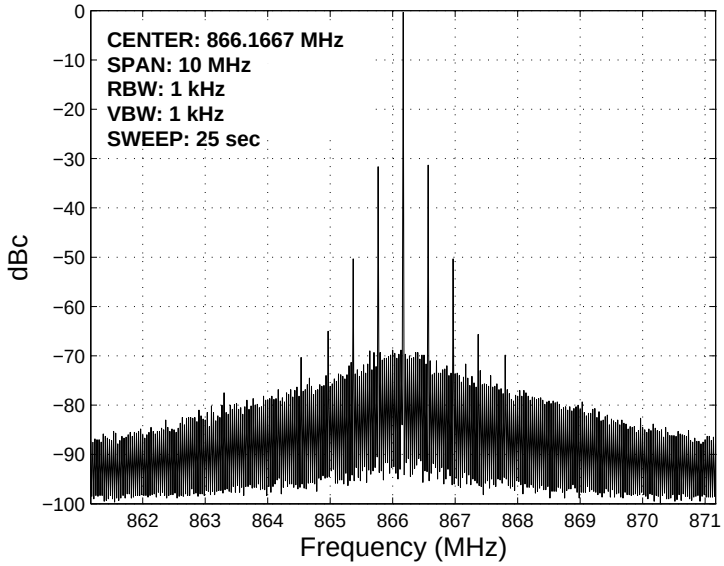
Figure 5.10 Modelled (a) and measured (b) spectra of a fractional-*N* synthesiser with 255/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency; no external applied VCO cross-coupling.

Figure 5.11(a) shows the modelled synthesiser output spectrum, again with 255/1024 fractionality, but now with −20 dB VCO-to-phase detector cross-coupling using the numerical model described in equations (5.7) and (5.9). The result is now very different showing that this cross-coupling is predicted to produce three pairs of significant sidebands, spaced uniformly by 410 kHz, of amplitudes −31 dBc, −50 dBc and −64 dBc. The experimental results performed under the same conditions with the test synthesiser,

Figure 5.11(b), show a remarkably similar distribution with three discernible pairs of sidebands spaced by 410 kHz, of amplitudes −32 dBc, −51 dBc and −66 dBc.

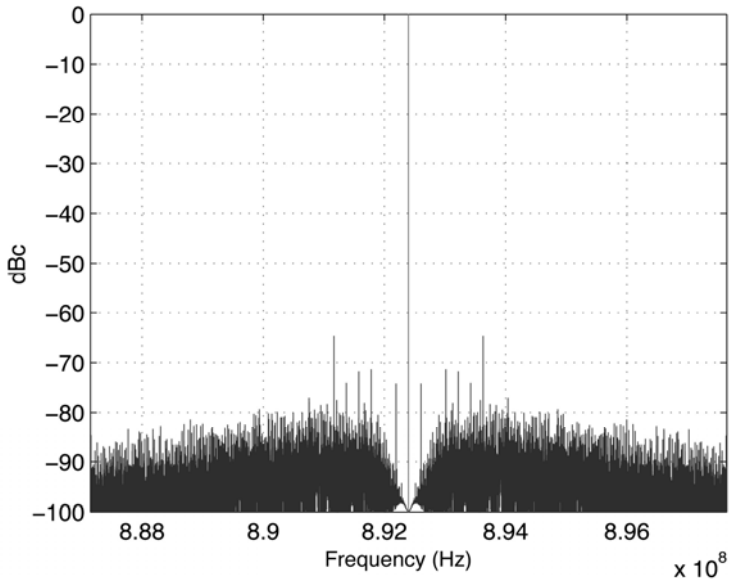


(a)

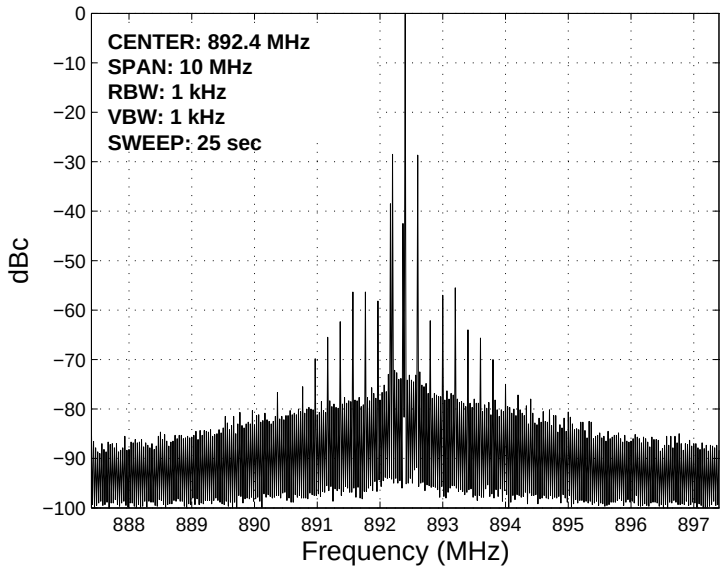


(b)

Figure 5.11 Modelled (a) and measured (b) spectra of a fractional-*N* synthesiser with 255/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency; –20 dB external VCO cross-coupling.



(a)

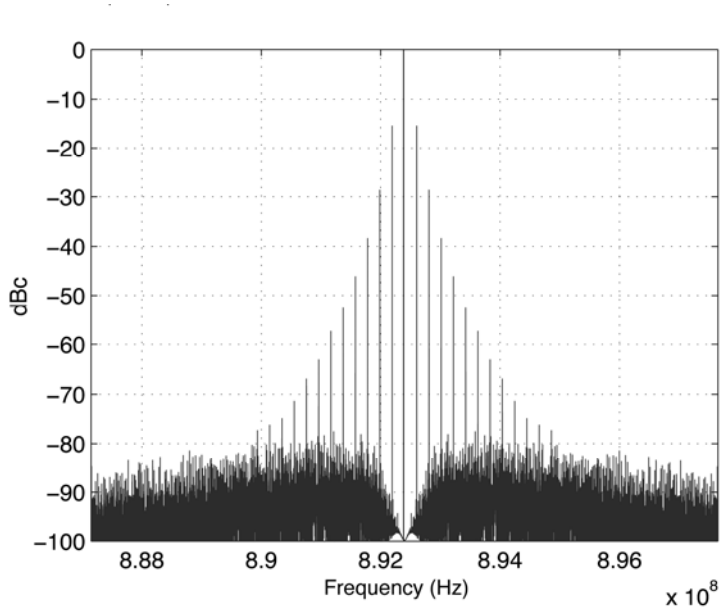


(b)

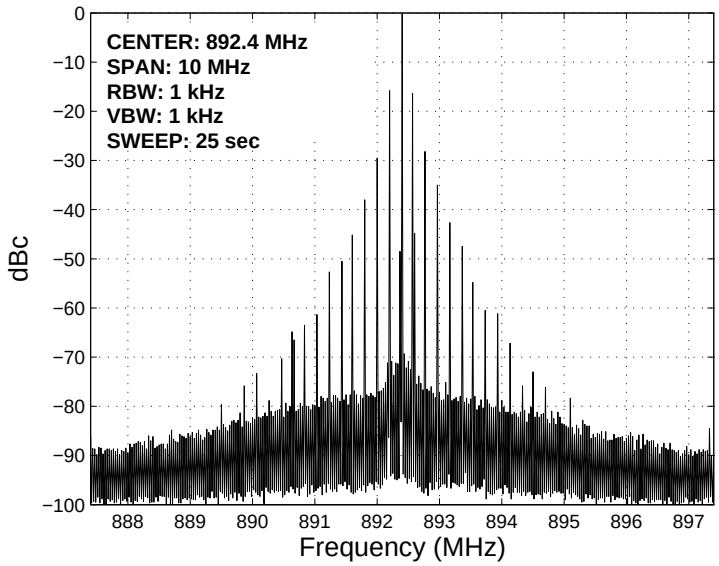
Figure 5.12 Modelled (a) and measured (b) spectra of a fractional-*N* synthesiser with 511/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency; no external applied VCO cross-coupling.

This exercise has been repeated with a variety of cross-coupling ratios and fractionalities. Figures 5.12 and 5.13 show the results for a synthesiser output frequency of 892.3975 MHz, corresponding to 511/1024 fractionality. In the absence of VCO-to-phase detector cross-coupling (Figure 5.12) the modelled result suggests low sideband levels of −65 dBc and below whereas the measured result shows some high close-in sidebands of −28 dBc at 205 kHz offset. However, with −19 dB VCO cross-

coupling (Figure 5.13) both modelled and measured results bear a striking resemblance with many pairs of large sidebands, the first four having predicted amplitudes of −15 dBc, −28 dBc, −38 dBc and −46 dBc, respectively, with the corresponding experimentally-measured values of −16 dBc, −28 dBc, −35 dBc and −43 dBc, spaced by 205 kHz, showing close agreement.



(a)



(b)

Figure 5.13 Modelled (a) and measured (b) spectra of a fractional-*N* synthesiser with 511/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency; −19 dB external VCO cross-coupling.

These results provide very strong evidence that, apart from the pulse-swallowing effect, potential cross-coupling paths cause intermodulation effects in the loop and resulting in the generation of discrete spurs that could, of course, cause significant adjacent-channel interference. The mechanism introduced here − VCO-to-phase detector cross-coupling (and subsequent sampling at the phase detector) − is able to produce significant and closely-spaced discrete spurs, of a very similar nature to fractional spurs. A possible explanation for the high experimentally-measured spurs in the absence of cross-coupling is that they are produced by the inherent, unintended, VCO cross-coupling taking place within the circuit itself and it is indeed this inherent vulnerability of fractional-*N* frequency synthesisers that this chapter is seeking to explore. Techniques for suppressing pulse-swallowing-born spurs, such as interpolation and Σ-Δ modulation, are not valid for suppressing these intermodulation-induced spurs.

5.4 Spur Suppression Techniques and Measured Results

There are a number of possibilities for controlling fractional spurs resulting from this mechanism. The most obvious is to prevent the two different frequencies from appearing at any single point in the synthesiser. The intermodulation effect can be reduced by good supply decoupling in conjunction with high-pass filtering between the VCO and frequency divider and low-pass filtering between the frequency divider and phase detector and careful attention to signal levels. Because the intermodulation effect occurs in multiple cross-coupling paths, complete removal of the potential for cross-coupling in the system is impossible. However, a new technique involving phase compensated cross-coupling is proposed to at least partially cancel-out the leakage path.

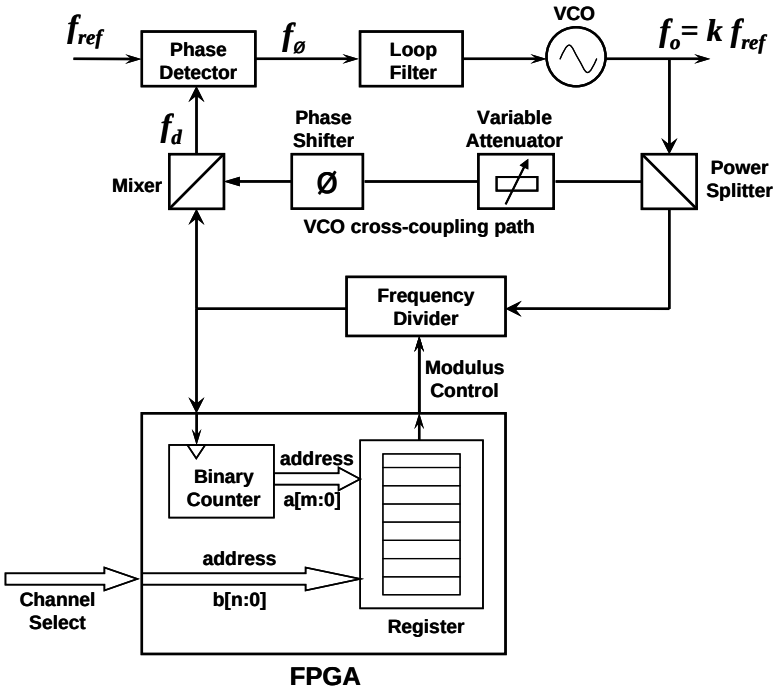


Figure 5.14 The architecture of a fractional-*N* frequency synthesiser with phase compensation technique.

The VCO and reference frequency signals combine quite naturally in synthesisers due to a variety of cross-coupling paths, including direct signal coupling through components, such as the frequency divider, PCB tracks and through supply and ground lines. Hence it is very difficult to model the intermodulation effect by software simulation. A test circuit based on the former measurement is developed, as shown in Figure 5.14, in which the intermodulation effect can be seen as a vector combination of signals with the same frequency and different phases. Our earlier measurements involved the coupling of a controlled amplitude and phase VCO signal onto the phase detector input to mimic the cross-coupling inherent in any real circuit. Supposing this cross-coupling can be described by the signal $C_1\sin(2\pi kt/T_{ref}+\phi_1)$ with amplitude C_1 and phase delay ϕ_1 relative to the VCO output; then an off-chip cross-coupling signal $C_2\sin(2\pi kt/T_{ref}+\phi_2)$ may be applied to cancel the intermodulation effect. When these vectors have similar amplitude and opposite phase then their combination will result in a nulling of the coupling and hence intermodulation effect. The combination of these vectors is

$$V = C_1 \sin\left(2\pi kt / T_{ref} + \phi_1\right) - C_2 \sin\left(2\pi kt / T_{ref} + \phi_2\right) = C \sin\left(2\pi kt / T_{ref} + \phi\right) \qquad (5.24)$$

where

$$C = \sqrt{C_1^{\,2} + C_2^{\,2} - 2C_1C_2\cos\Delta\phi} \quad (\Delta\phi = \phi_2 - \phi_1) \tag{5.25}$$

$$\phi = \arctan\left(\frac{C_1\sin\phi_1 - C_2\sin\phi_2}{C_1\cos\phi_1 - C_2\cos\phi_2}\right) \tag{5.26}$$

and the amplitude of the resultant is given by

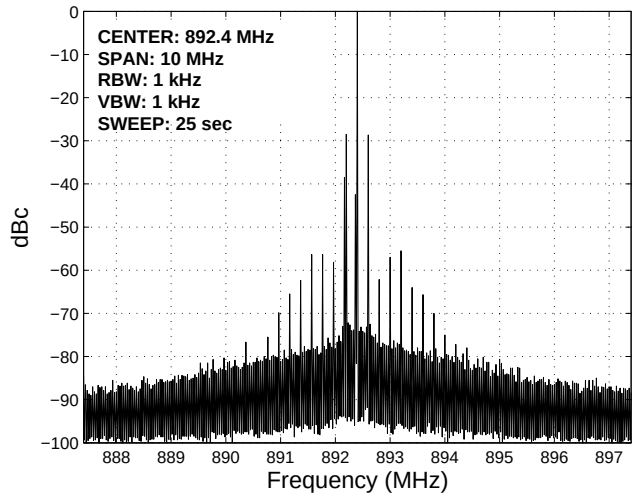
$$|V|_{dB} = 20\log_{10}\left(\sqrt{C_1^{\,2} + C_2^{\,2} - 2C_1C_2\cos\Delta\phi}\right) \tag{5.27}$$

The spectra resulting from different levels of cross-coupling were recorded and compared with predictions in order to validate the theory. The amplitude of the intermodulation-cancelling path is controlled by a variable attenuator and the phase is monitored by a network analyser. The level of coupling is measured by the recorded VCO output on a spectrum analyser. Figures 5.15 and 5.16 show the measured spectra with the proposed technique. A −23 dB cross-coupling signal with appropriate phase compensation is finally chosen to achieve the lowest fractional spurs. Figure 5.15 shows the measured spectrum with 511/1024 fractionality. The first pair of fractional spurs is suppressed to −45 dBc at 205 kHz offset, which is 18 dB lower than direct measured results without the phase compensation technique as shown in Figure 5.15(a). Although the proposed compensation technique reduces the first pair of sideband spurs, it increases the subsequent spurs. This is because of imperfect cancellation due to the limited amplitude and phase step sizes in the cancelling path. As a result, a new vector with lower amplitude is introduced, forming a new series of discrete spurs, some of which may have higher amplitudes. This effect may be eliminated if attenuators and phase shifters with finer resolution are employed. Figure 5.15(b) presents the spectrum with the lowest first pair of dominating spurs at 205 kHz offset. These spurious components are also expected to be further suppressed if an external cross-coupling path with finer resolution is used. The recorded results show that if the amplitude of the external cross-coupling is −23 dB ± 1 dB, and the phase is adjusted to ±5° resolution, then spur reduction of at least 12 dB is obtained, which means in this case that the first pair of spurs at 205 kHz offset are reduced to around −40 dBc. Figure 5.15(c) shows

the measured spectrum with the same fractionality, −24 dB cross-coupling with about 5° phase shift relative to the measurement setup used in Figure 5.15(b).

Figure 5.16 shows the measured spectrum with 255/1024 fractionality. Compared to the spectrum measured without the proposed technique, the first pair of spurs is suppressed by around 17 dB, to −64 dBc at 410 kHz offset when −23 dB phase compensation cross-coupling is applied. The second pair of spurs are also suppressed to −64 dBc, by about 11 dB at 820 kHz offset.

Figure 5.17 shows the measured close-in spur level (at 205 kHz offset) when different cross-coupling parameters are applied, on this occasion with 511/1024 fractionality. The straight line indicates dominant sideband spur level in the absence of external cross-coupling. Figure 5.18 shows the spur levels for a synthesiser output with 255/1024 fractionality. It is evident that the first pair of spurs at 410 kHz offset is suppressed to −64 dBc when a −23 dB VCO cross-coupling is used with carefully chosen phase delay. This provides convincing evidence not only of the existence of the cross-coupling mechanism but of a technique that significantly suppresses the effect, at least for the dominant fractional spurs.



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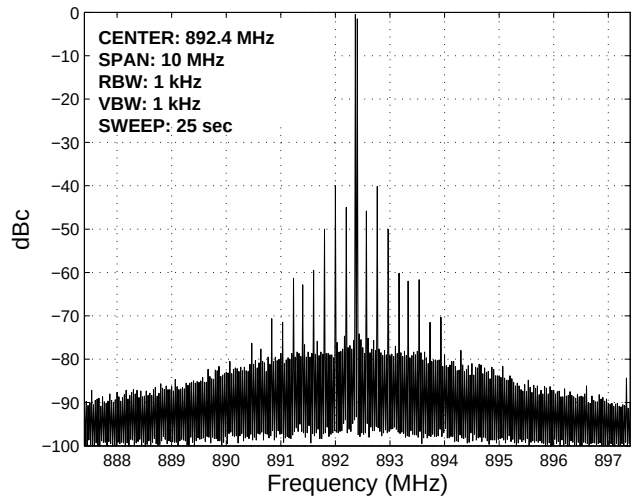

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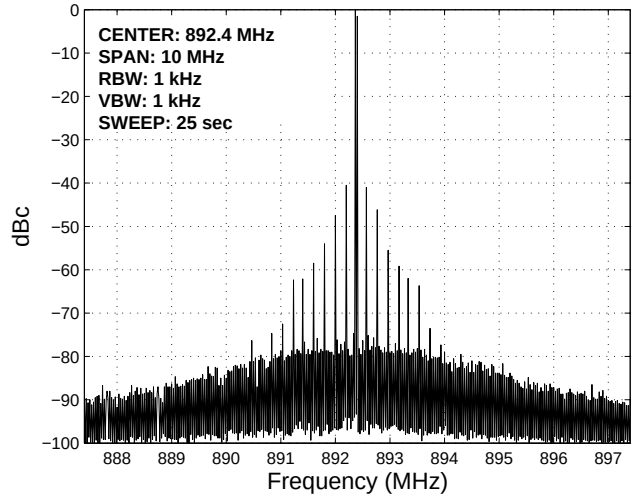
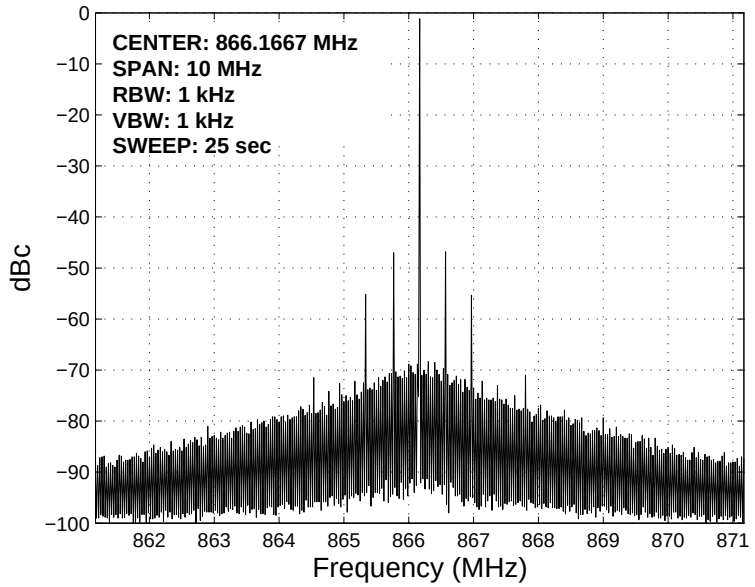


(c)

Figure 5.15 Measured spectrum of a fractional-*N* synthesiser with 511/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency. (a) No external applied cross-coupling. (b) Controlled amplitude (−23 dB) and phase cross-coupling. (c) −24 dB cross-coupling with 5° phase shift relative to the measurement in (b).



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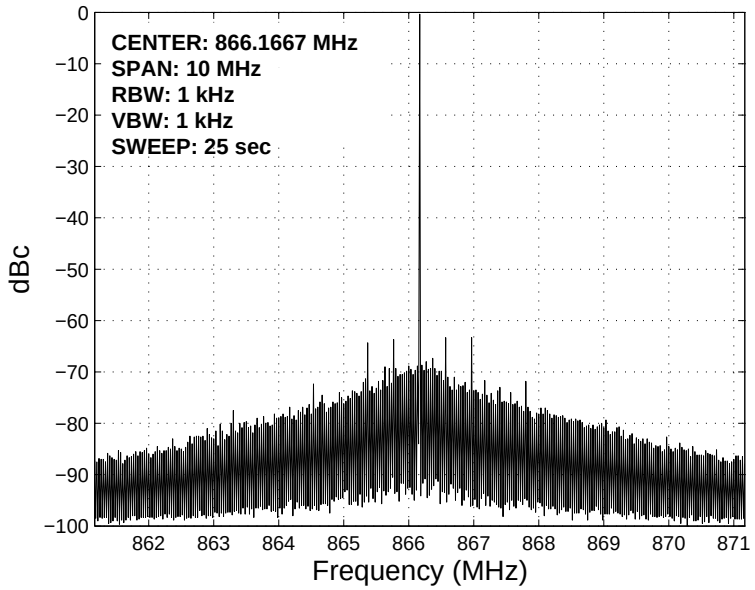


(b)

Figure 5.16 Measured spectrum of a fractional-*N* synthesiser with 255/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency. (a) No external applied cross-coupling. (b) Controlled amplitude and phase cross-coupling.

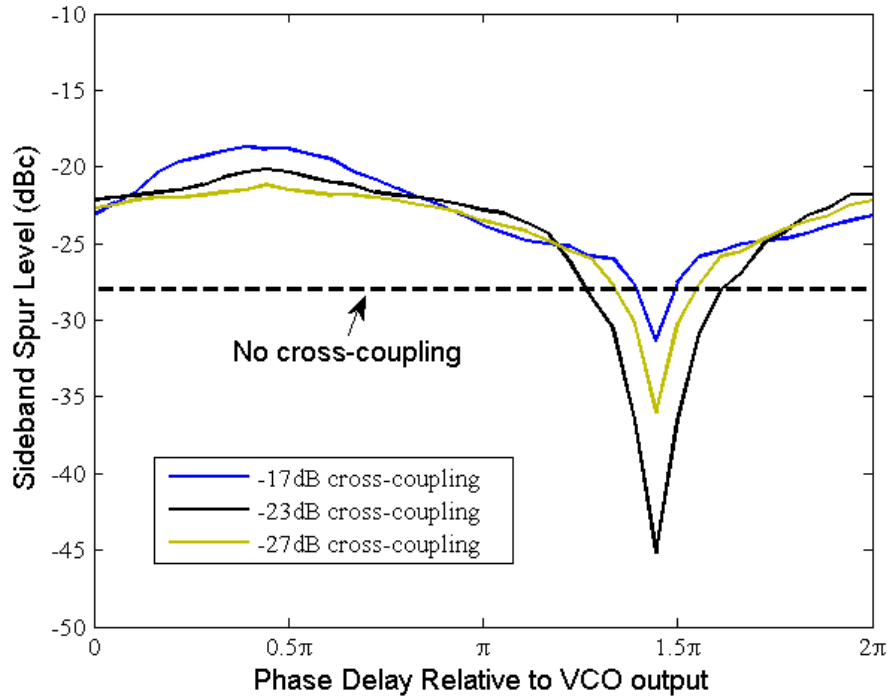


Figure 5.17 Measured sideband spur level versus a controlled amplitude and phase cross-coupling, with 511/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency.

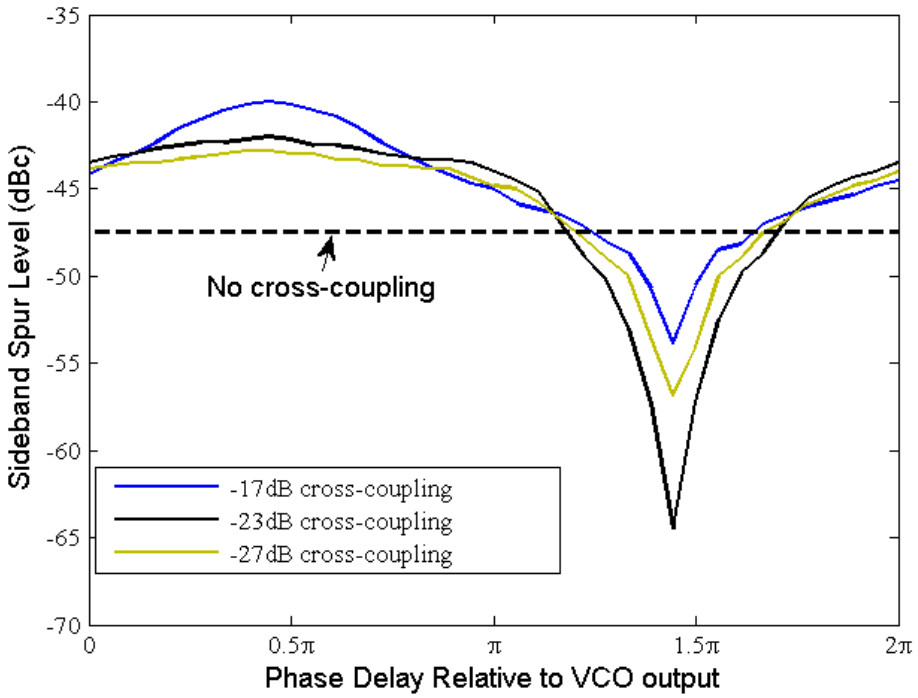


Figure 5.18 Measured sideband spur level versus a controlled amplitude and phase cross-coupling, with 255/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency.

5.5 Summary

A recently-reported new phenomenon in fractional-*N* frequency synthesisers has been presented the convincing experimental validation, which is capable of producing a family of close-in spurious components of similar form to the well-known fractional spurs usually attributed solely to modulator operation. The mechanism is based on small degrees of cross-coupling and/or intermodulation and subsequent phase detector aliasing of the non-harmonically related components necessarily present in such synthesisers.

Numerical and analytic modelling has been developed to predict the amplitudes and frequencies of the components produced by this process, demonstrating that modest degrees of VCO-to-phase detector cross-coupling can produce substantial effects. These predictions have subsequently been validated against experimental results obtained from a synthesiser measurement arrangement in which a controlled amplitude of VCO signal is cross-coupled to the phase detector input. The measured results have shown good agreement with predictions.

Finally, for the first time an experiment has been successfully conducted, attempting to cancel the VCO to phase detector cross-coupling responsible for this phenomenon. It is evident that a substantial reduction in fractional spurs is possible using an open-loop analogue technique that is entirely separate from the modulator. The measured results show that these spurious components exist and furthermore may be effectively suppressed, by some 18 dB, with appropriate adjustment of the amplitude and phase of the cancelling path. This new technique is suitable for almost all fractional-*N* synthesisers and may have real value in reducing the level of fractional spurs and thus improving spectral purity. It may also be implemented digitally by pre-distortion of the modulator waveform thus offering a more convenient and flexible means of improving spectral purity. This technique is described in detail in chapter 6.

Chapter 6

Pre-Distortion Sigma-Delta Noise Shaping

6.1 Introduction

Single-bit Σ-Δ modulators are widely employed in fractional-*N* synthesisers because of their simplicity and ease of interface with frequency dividers; however, these modulators tend to suffer from a particular set of discrete spurious tones [105, 106], the so-called *fractional spurs*. These spurs are produced largely by the restricted limit cycle associated with Σ-Δ modulators, often resulting in a significant number of close-in fractional spurs at measurable levels. The generation of these spectral components may be enhanced by practical circuit artifacts due to cross-coupling and modulation in the synthesiser circuit as illustrated in Chapter 5. Indeed, on certain channels, inadequate randomisation of the Σ-Δ modulator results in limit cycles which may sometimes produce unacceptable levels of discrete spurious components. This discrete spur generation often creates a performance limit, particularly in single-bit Σ-Δ modulator designs.

This work proposes a new technique for effectively suppressing spurious components caused by any possible reason in Σ-Δ fractional-*N* synthesisers, without the detrimental affects of the dithering, and other techniques that are often used to address this issue. The new technique is based on pre-distorting the modulator inputs by the addition of a series of small sinusoidal signals in anti-phase with the principal spurious components, as found perhaps by direct measurement of the synthesiser output. The technique described here is based on a stored-sequence architecture [86, 87] in which the noise-shaped bitstream is generated and optimised offline and then stored in a fast memory and used to control the dual-modulus divider on the basis of a separate stored bitstream for each channel frequency. This technique lends itself very well to the incorporation of a compensation scheme such as that described here. A synthesiser based on the proposed technique has been successfully developed, with the architecture shown in

Figure 6.1. This new technique is particularly suited to FPGA or CPLD implementation to achieve superior noise shaping, providing better performance than conventional CMOS Σ-Δ modulators.

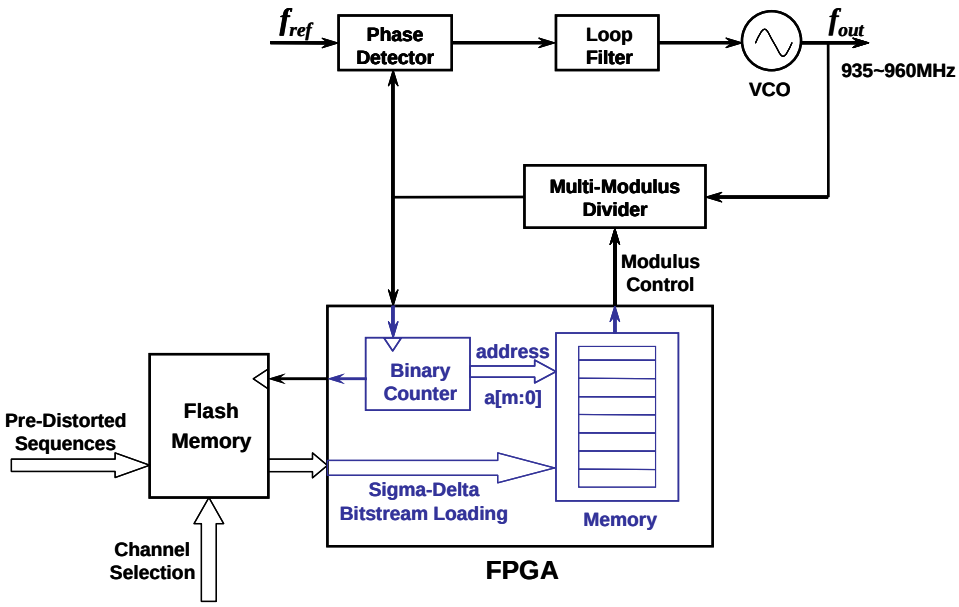


Figure 6.1 Proposed pre-distortion stored-sequence Σ-Δ fractional-*N* synthesiser.

6.2 Noise Shaping and Spurious Component Analysis

Analysis of equations (5.1-5.5) reveals that, the VCO output spectra may contain a set of discrete spurious components spaced by Δf, which for certain fractionalities may be identical to those obtained with an integer frequency synthesiser. As an example, taking a fractionality, α, of 511/1024 it is found, from equation (5.4) that p = 1024 and, from equation (5.5) that the resulting fractional spurs are separated by $f_{ref}/1024$ and uniformly distributed between $-f_{ref}/2$ and $f_{ref}/2$. This analysis demonstrates the potential spurious components that may be produced, and further simulations [99] predict the exact distributions for particular modulators, fractionalites and circuit conditions.

The purpose of Σ-Δ fractional-*N* synthesis is to shape the quantisation noise caused by divider switching (quantisation) so that the in-band phase noise is improved at the expense of out-of-band phase noise. The Σ-Δ modulator provides a bitstream with the desired mean value for a given channel, which is equal to the DC value applied at its

input. The DC input signal is translated by the modulator to a varying output signal (between logic 0 and logic 1 in the case of a 1-bit device) with a mean value identical to the DC input value but with a high-pass shaped noise spectrum, by virtue of the multiple integrators in the negative feedback loop, as shown in Figure 3.27. A classic third order single-bit Σ-Δ modulator based on a feedback topology is employed as a platform for pre-distortion technique validation. A modulator of this kind using a single-bit quantizer offers a simple and convenient synthesiser implementation, using a dual-modulus divider, but tends to suffer from tonal behaviour leading to relatively large discrete spurious components at some of the frequencies described by equation (5.5). These fractional spurious components degrade the spectral purity of fractional-*N* synthesisers and present a major limitation to the approach.

The frequency domain signal transfer function and noise transfer function of this modulator are shown in Figure 3.28. It is clear that the signal transfer function presents a low-pass frequency response whilst the noise transfer function is a high-pass response that, in effect, pushes quantisation noise to higher frequencies. With a uniform white noise assumption, the error signal $e(x)$ introduced by the quantizer has equal probability of lying between $-\Delta/2$ and $\Delta/2$, where Δ is the quantizer step.

$$e(x) = \begin{cases} \Delta - x & x \geq \Delta/2 \\ x & x \leq \Delta \end{cases} \tag{6.1}$$

The Fourier transform of a single period of $e(x)$ is given by

$$Q_{iF}(\omega) = \int_0^{\Delta/2} -x \cdot e^{-j\omega x} dx + \int_{\Delta/2}^{\Delta} (\Delta - x) \cdot e^{-j\omega x} dx \tag{6.2}$$

The Fourier transform of the periodic $e(x)$ is given by

$$Q_i(\omega) = \omega_o \cdot \sum_{n=-\infty}^{\infty} Q_{iF}(\omega) \cdot \delta(\omega - \omega_o) \tag{6.3}$$

where $\omega_o = \dfrac{2\pi}{\Delta}$.

From equations (6.2) and (6.3), the quantisation noise can be expressed as

$$Q_i(\omega) = j\frac{\Delta}{2\pi} \cdot \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \frac{(-1)^{n+1}}{n} \cdot \delta\left(\omega - \frac{2\pi n}{\Delta}\right) \tag{6.4}$$

The mean square quantisation error is thus given by

$$Q^2 = \left(\frac{\Delta}{2\pi}\right)^2 \cdot \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \frac{1}{n^2} = \frac{\Delta^2}{12} \tag{6.5}$$

The frequency domain noise shaping function of the Σ-Δ modulator is approximated by [46, 107]

$$N(f) = \Delta\sqrt{\frac{1}{12 f_{ref}}}\left|H_{NTF}(f)\right| \tag{6.6}$$

and the theoretical PSD can be calculated by

$$P(f) = \frac{\Delta^2}{12 f_{ref}}\left|H_{NTF}(f)\right|^2 \tag{6.7}$$

It is evident that the existence of this pattern noise poses a serious problem to the use of Σ-Δ modulators in frequency synthesis, where spectral purity is of utmost importance. Single-bit Σ-Δ modulators are particularly vulnerable to pattern noise because of their limited quantizer values (0 or 1) and tonal behaviour, often with highly repetitive, finite limit cycles as illustrated in Figure 6.2. In order to mitigate the problem of spurious component generation, caused by modulator pattern noise in fractional-*N* synthesis, two approaches have emerged. The first involves replacing the single-bit quantizer with a multi-bit topology, perhaps enhanced by the use of a higher order Σ-Δ modulator [108]. With multi-bit quantisation, the output can span multiple values, such that the modulator data stream is further randomised and quantisation noise becomes whiter. This can reduce the level of spurious tones, though not eliminate them, but the architecture of the Σ-Δ modulator and frequency divider are rather more complicated. In addition, cascaded delays limit the achievable sampling speed and cause higher in-band synthesiser phase noise.

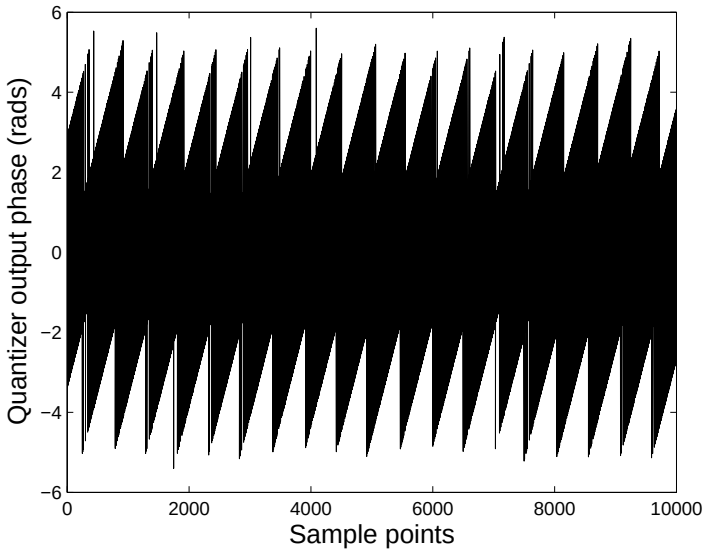


Figure 6.2 Modelled phase jitter of third-order single-bit Σ-Δ modulator with 511/1024 input.

The second approach is to introduce a dithering signal [109-111] by adding a second signal to the input DC signal of the modulator. In some systems, the dithering signal is later removed by filtering or by subtraction from the output (subtractive dithering). The dithering method has long been used for the purpose of smoothing the noise spectrum and for making the noise spectrum independent or less dependent on the input signal level. The PSD of the quantisation error in a Σ-Δ modulator with DC inputs consists of discrete spurious components. It is evident that proper dithering will remove or reduce the spurs as it does in uniform quantisation.

Least significant bit (LSB) and small pseudo-random noise are common dithering signals added onto the input DC signal of the modulator. The LSB method introduces a small DC offset to the modulator input to extend limit cycles, as a small DC offset can increase the denominator p in equation (5.5) A small amount of white noise can also be used to randomise the quantizer noise. In practice a pseudo-random noise source having a rectangular pulse density function (rPDF) is commonly used. With suitable design, this can extend the repetition length of bitstreams and suppress the discrete spurious components of the quantisation noise. The dithering signal must contain low level energy in the signal band, otherwise it may significantly increase the synthesiser phase noise floor. As a result, the modulator input is no longer a constant DC signal and the spurious tones in the output spectrum are, effectively, whitened and thus suppressed. This method is now widely used in synthesiser circuit and system designs as an

effective method to obtain whitened continous spectra. Figure 6.3 shows a comparison of the modelled dithering effect on noise shaping of a single-bit feedback Σ-Δ modulator. When the Σ-Δ modulator input is a DC signal corresponding to a fractionality of 511/1024, without any dithering effect, the quantisation noise power concentrates on a series of discrete spurs uniformly spaced by $0.000488f_{ref}$. After adding a LSB dithering signal of $1/2^{14}$, the quantisation noise power is separated on more discrete components and the noise floor is effectively suppressed, as shown in Figure 6.3(b). Figure 6.3(d) presents the modelled result of the dithering effect by adding a small pseudo-random noise-dithering signal, which is able to further whiten the noise shaping and leads to lower spurious components.

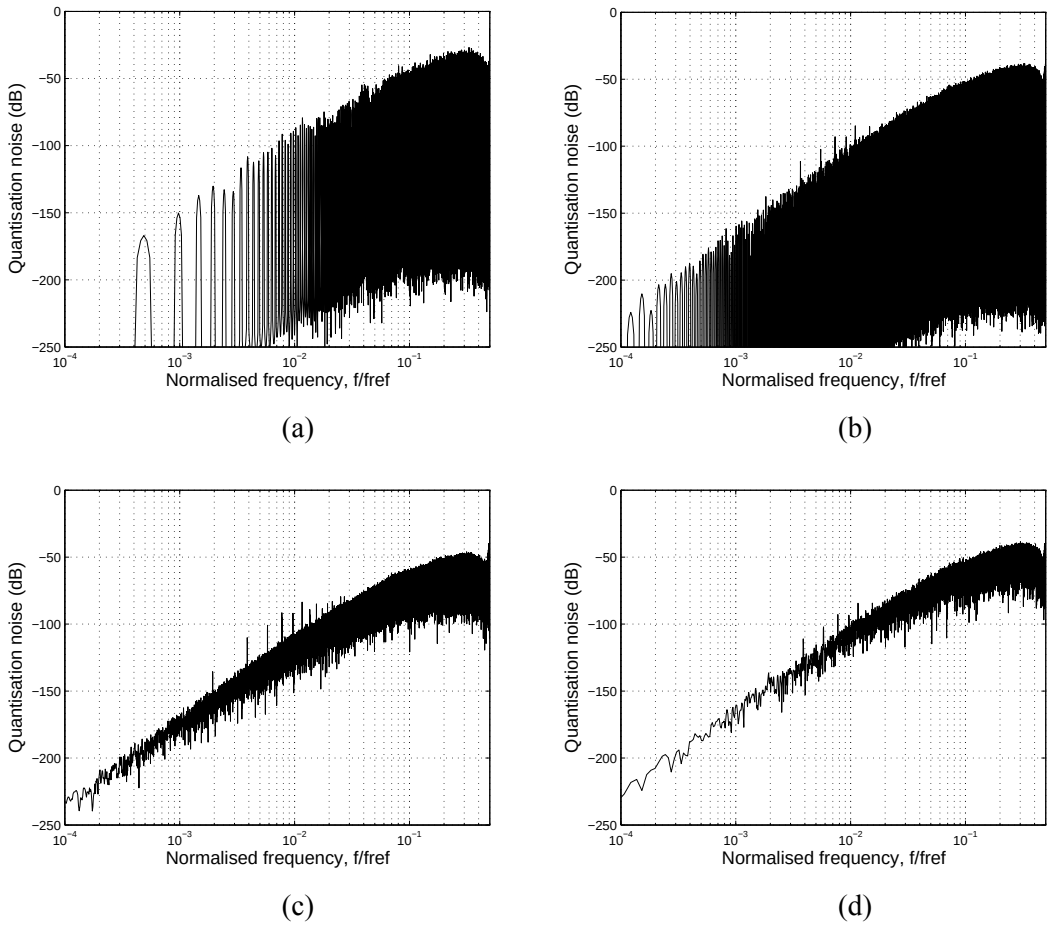


Figure 6.3 Modelled dithering effect of a third-order single-bit Σ-Δ modulator with 511/1024 input. (a) No dithering. (b) LSB dithering of $1/2^{14}$. (c) LSB dithering of $1/2^{17}$. (d) Small pseudo-random noise dithering.

6.3 The Proposed Technique

A key issue with the dithering approach often used in Σ-Δ modulators is that the dithering signal can only extend the sequence length, but not directly suppress pattern noise and associated discrete spurious components. As a result, pattern noise and associated fractional spurs are still present although discrete spur amplitudes are slightly reduced. The proposed technique differs from prior dithering techniques by adding to the DC input of the Σ-Δ modulator a set of pre-distortion sinusoids, designed to cancel specific troublesome discrete spurs. These small amplitude pre-distortion signals can be used not just to cancel spurs resulting from modulator behaviour but from any other mechanisms occurring in the circuit, thus offering a direct and effective technique to enhance synthesiser spectral purity. The modulator input signal is thus augmented by a set of sinusoidal pre-distortion components with a DC bias equal to the desired channel selection value [112], as illustrated in Figure 6.4 for the case of 511/1024 fractionality.

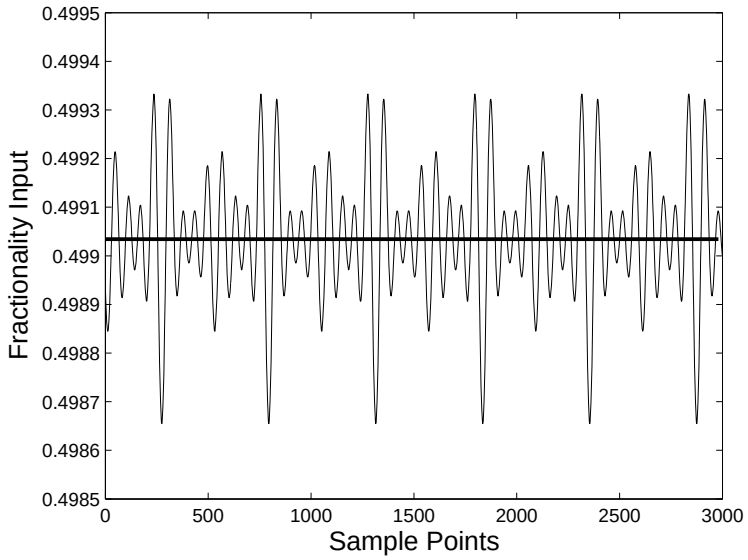


Figure 6.4 Input of a Σ-Δ modulator with and without pre-distortion signals, fractionality = 511/1024.

The parameters of the necessary cancelling components can be found from experimental measurement of a given synthesiser or may be estimated from basic theory. In the latter case, from [99], a given fractional spur can be described by the presence at the Σ-Δ modulator output of a signal $C_1 \sin(\omega_1 t + \phi_1)$; hence a pre-distortion signal

$-C_2\sin(\omega_1 t + \phi_2)$ may be generated at this point to cancel the dominant spur. When these two vectors have similar amplitudes and are close to anti-phase then their combination will result in a nulling of the spurious tone. For instance, if the compensating component is matched to within 1 dB in amplitude and 5° in phase then, from equation (5.27), the offending spurious component will be attenuated by 32.6 dB. From equation (3.18) the signal transfer frequency response is:

$$H_{STF}(\omega) = \frac{e^{j3\omega/f_{ref}}}{e^{j3\omega/f_{ref}} + (A+B-2)e^{j2\omega/f_{ref}} - (A+2B-3)e^{j\omega/f_{ref}} + (B-1)} \tag{6.8}$$

which allows the parameters of each modulator pre-distortion component, applied to the modulator input, to be calculated in order to cancel a given spurious component. This, of course, assumes that the modulator behaves in a linear fashion, which is reasonable under small signal conditions though in general its behaviour will be nonlinear due to the action of the quantizer. Since the modulator signal transfer function has a low pass characteristic, higher offset frequency pre-distortion signals require higher pre-distortion signal amplitudes which may suffer from non-linear affects in the modulator. A numerical method may therefore be preferable to optimise the pre-distortion components in order to successfully mitigate the fractional spurs.

This technique may be difficult to implement with traditional CMOS digital blocks which are normally used to realise the modulator function in such synthesisers, because multiple sinusoidal signals with appropriate frequency, amplitude and phase are difficult to process at high speed in real time and apply to the input of the Σ-Δ modulator. FPGA or CPLD solutions using the stored-sequence approach offer a more convenient means of realising the circuit hardware.

6.4 Experimental Setup and Results

An experiment has been devised to evaluate the proposed technique, as shown in Figure 6.5, based on the stored-sequence method [86, 87] which is implemented by an FPGA. The noise shaping bitstreams are generated offline by MATLAB/SIMULINK or HP-ADS. These bitstreams have an average value as required for a given channel

frequency and fractionality, but initially without the addition of any pre-distortion signals. These pre-generated bitstreams are stored in a flash memory, and clocked out by FPGA to control the division ratio. The synthesiser output is monitored by a spectrum analyser and the results are recorded via a GPIB interface.

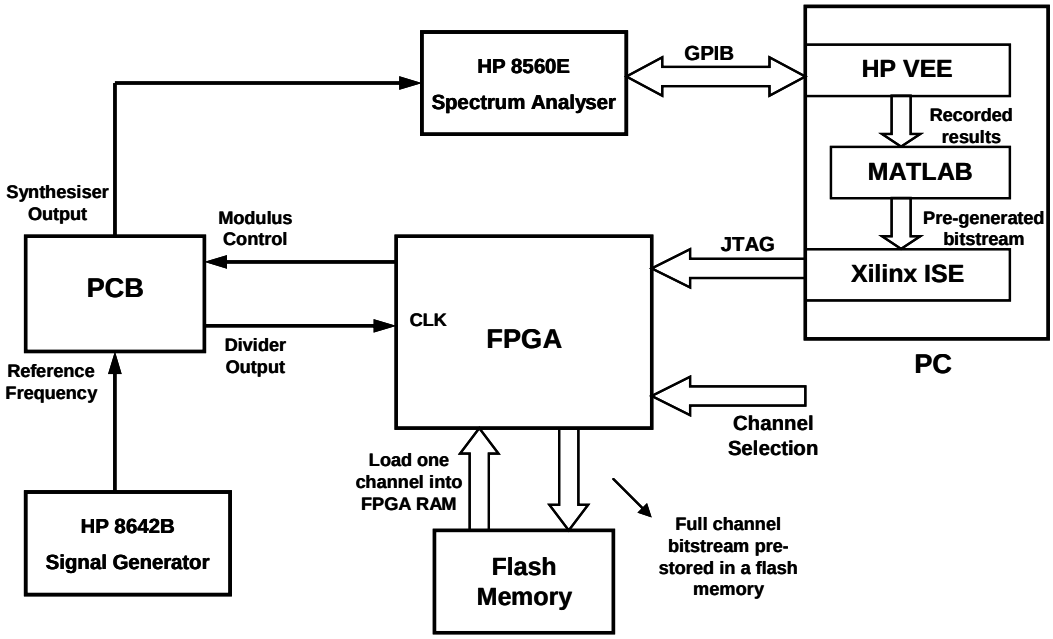
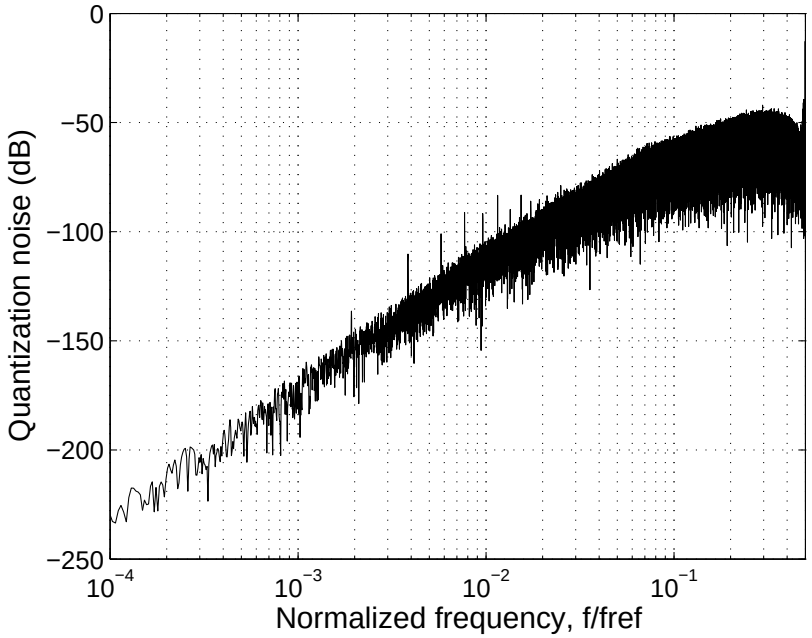
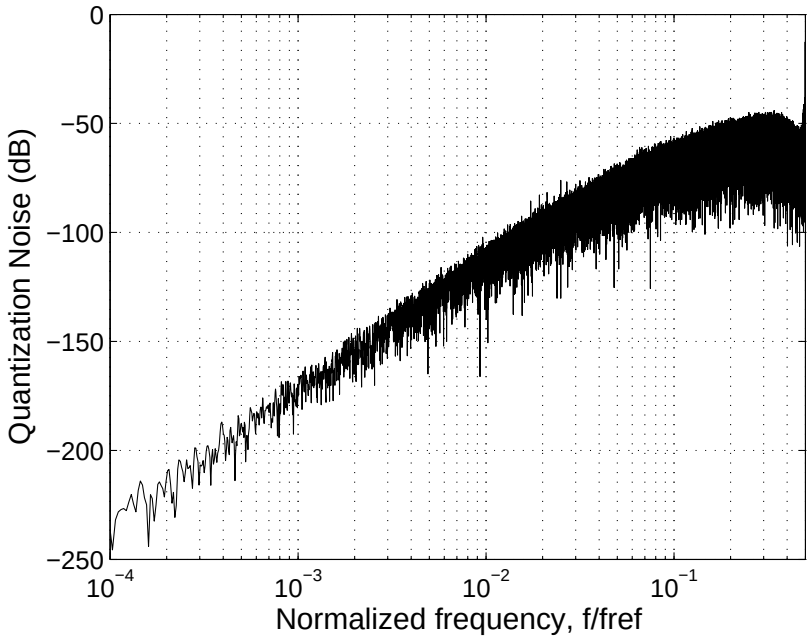


Figure 6.5 Experimental setup of the pre-distortion synthesiser measurement.

The proposed architecture, as shown in Figure 6.1, leverages the complicated CMOS Σ-Δ modulator design which is used to implement the digital block in the traditional fractional-*N* synthesiser. It, instead, utilises an FPGA module to obtain a high speed logical signal controlling the dual-modulus frequency divider. The optimised bitstreams are generated off-line, covering 373 channels of the DCS-1800 division control sequences. These are stored in a ROM to replace the usual CMOS digital block and the bitstreams are clocked out at high speed by the FPGA to control the divider, with an average division ratio commensurate with the desired output frequency. The synthesiser prototype contains a ÷8/9 dual-modulus divider and a third order active loop filter with 250 kHz natural frequency.



(a)



(b)

Figure 6.6 Modelled quantisation noise PSD of a Σ-Δ modulator with 511/1024 fractionality, without (a) and with (b) the proposed pre-distortion technique.

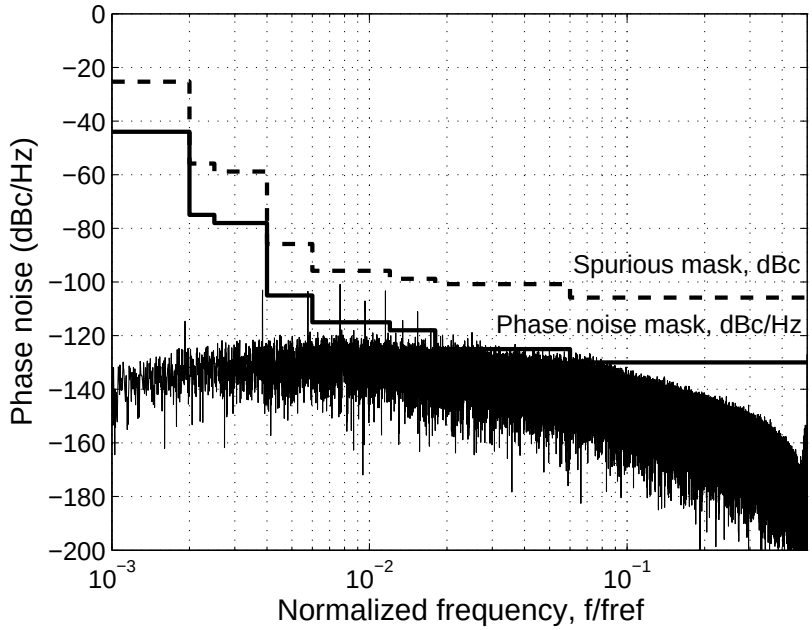
Discrete spur performance with a single-bit Σ-Δ modulator shows a marked variation with fractionality and modulator parameters. For instance, with 511/1024 fractionality and feedback weights of A = 8, B = 16, the Matlab-modelled modulator SSB power spectral density shows particularly high fractional spurs. Referring to Figure 6.6(a), the

modulator output exhibits a noise characteristic typical of a modulator of this kind, with high-pass noise shaping pushing the quantisation noise far from the carrier, but with evidence of high level discrete fractional spurs at frequency offsets of $0.00195f_{ref}$, $0.00391f_{ref}$, and $0.00586f_{ref}$, uniformly spaced by $f_{ref}/512$ as predicted. If a 105 MHz reference frequency is chosen to drive the synthesiser which is the same as modulator sampling frequency, and the natural frequency is 250 kHz, the first spur is at 205 kHz frequency offset, which is within the PLL filter pass band and so cannot be suppressed by PLL loop action. The other spurs are also sufficiently large and close-in to produce spurious tones in the synthesiser output that may cause concern. Figure 6.7(a) shows the modelled phase noise and spurious performance of a complete synthesiser, without pre-distortion, based on the same modulator parameters. The division ratio of the synthesiser is set to 8 + 511/1024 and a third order loop filter with 250 kHz natural frequency is used. There are some eight significant spurs spread from $0.00195f_{ref}$ to $0.01563f_{ref}$, with a similar quantisation noise distribution as that shown in Figure 6.6(a).

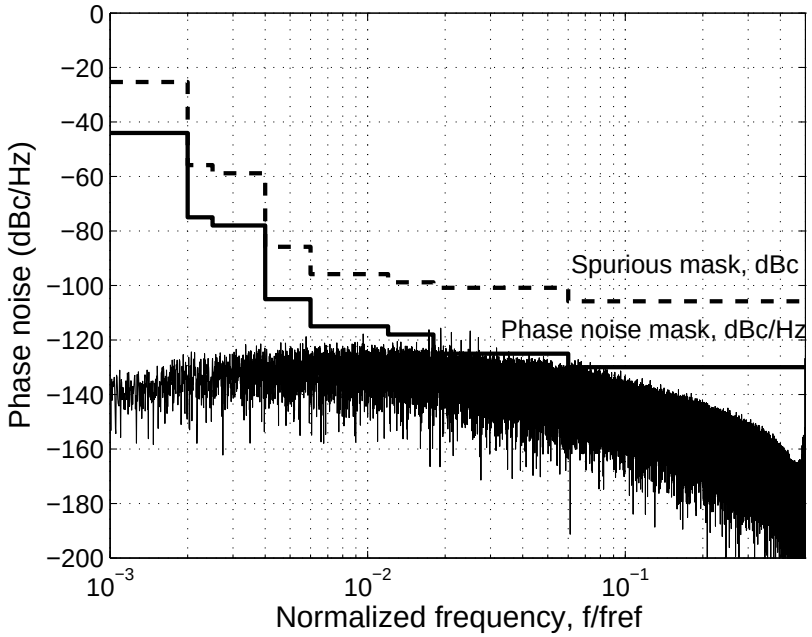
To reduce spurious component levels, a set of eight sinusoidal pre-distortion signals were applied to the modulator input. They are with the same frequency offsets, same magnitudes and oppsite phases as the discrete spurious components. As illustrated in Figure 6.4, the DC input is augmented by these pre-distortion signals, which are predicted by equations (5.25) and (5.26). Figure 6.6(b) and Figure 6.7(b) show the modelled modulator and synthesiser spectra after the pre-distortion signals are added, showing a marked reduction in spur levels. From Figure 6.6(b) it is clear that the discrete spurs are effectively reduced and are now buried in the noise floor, with no measurable change in the noise floor. There are several small spurs spread between $0.017f_{ref}$ and $0.027f_{ref}$, with the same spacing as the frequency resolution. These unwanted components are generated by digital sequence truncation and quantisation noise leakage. Their amplitudes, however, are much lower than the original troublesome spurs and do not cause any practical problem.

In order to validate the proposed pre-distortion technique in a practical synthesiser, an experiment has been conducted with a test synthesiser arrangement in which pre-distorted Σ-Δ noise shaping sequences are stored in an external flash memory. As a dithering effect to randomise the output cycle of the Σ-Δ modulator, introduction of the pre-distortion technique will extend the sequence cycle and the data size is no-longer

suitable for the FPGA integrated memory. Full channels of bitstreams are pre-stored in the flash memory and a single channel bitstream is loaded into FPGA memory when the channel selection signal is changed. The synthesiser used in these measurements is based on a third order feedback Σ-Δ topology, as shown in Figure 3.27, and the outcome of these measurements is given in Figures 6.8 and 6.9.

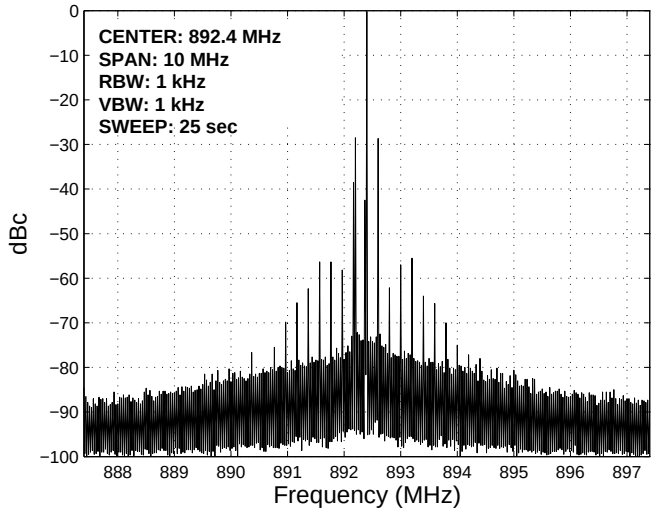


(a)

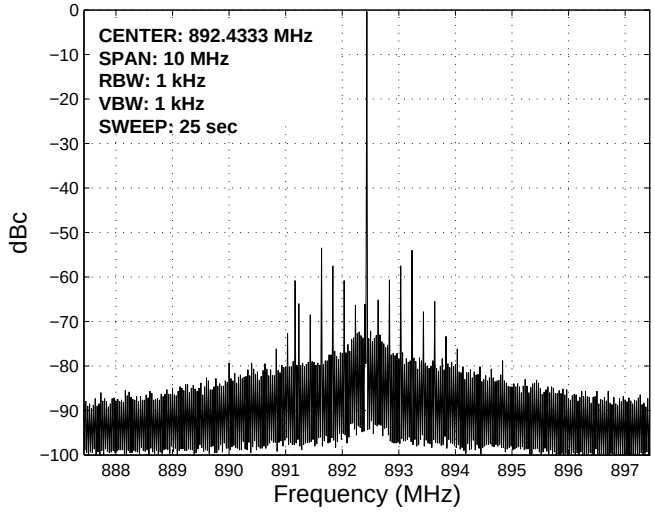


(b)

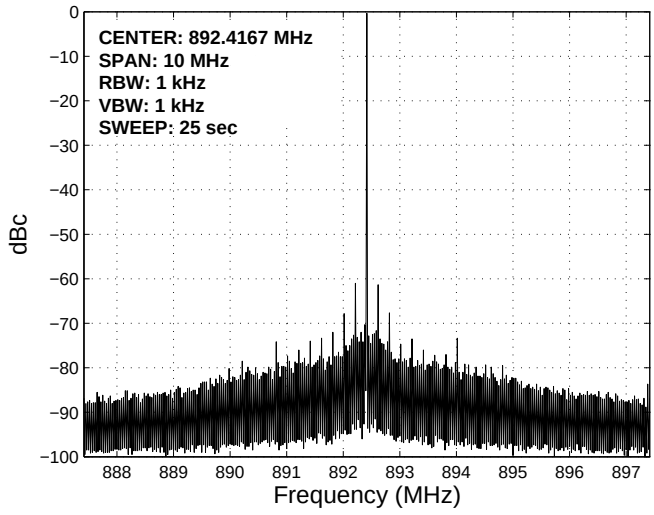
Figure 6.7 Modelled phase noise of a fractional-*N* synthesiser with 511/1024 fractionality, 100 kHz loop natural frequency, without (a) and with (b) proposed pre-distortion technique.



(a)



(b)

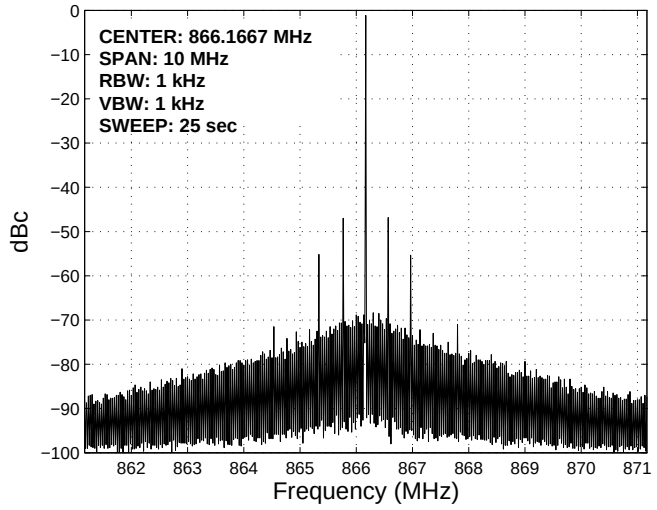


(c)

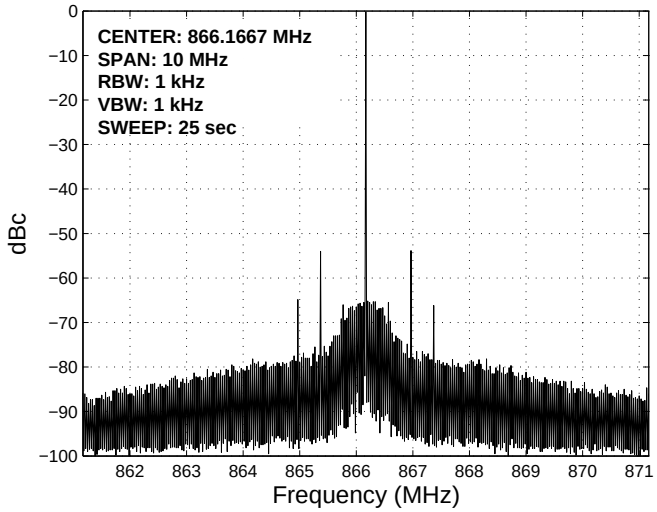
Figure 6.8 Measured spectra of a fractional-*N* synthesiser with 511/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency. (a) No pre-distortion. (b) Pre-distortion on first pair of sideband spurs. (c) Pre-distortion on all of sideband spurs.

The measured spectrum with a fractionality of 511/1024 is shown in Figure 6.8(a). The spectra are measured and recorded by a spectrum analyser HP 8560E. The fractional-*N* intermodulation effect [98-100, 103] and FPGA noise cause rather higher spur levels than predicted, with a pair of high spurs of −28 dBc. Figure 6.8(b) and (c) shows the measured synthesiser output spectra, with 511/1024 fractionality, but now with pre-distortion noise shaping added onto a constant DC input. Figure 6.8(b) presents the spectrum when an appropriate pre-distortion signal at 205 kHz offset frequency is applied. The dominant pair of spurs is reduced from −28 dBc in the uncompensated case shown in Figure 6.8(a) to −65 dBc. Figure 6.8(c) shows the measured spectrum when a series of eight pre-distortion components are introduced corresponding to all the fractional spurs. By comparison with the uncompensated case, it is clear that several pairs of high level close-in spurious components are suppressed by a substantial amount by this technique.

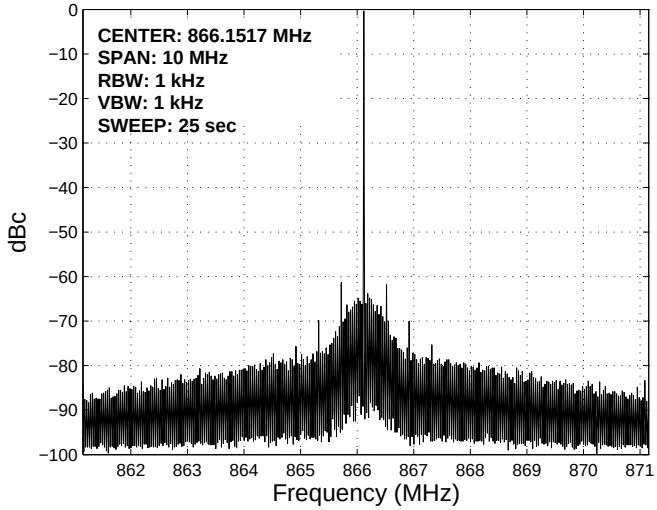
This exercise has been repeated with a variety of pre-distortion waveforms and fractionalities. Figures 6.9 show the results for a synthesiser output frequency of 866.1475 MHz, corresponding to 255/1024 fractionality. In the absence of pre-distortion the measured result shows a number of sideband pairs with high levels, the first three having amplitudes of −46 dBc, −55 dBc, and −66 dBc, spaced by 410 kHz. However, with a 410 kHz pre-distortion component the measured spectrum (Figure 6.9(b)) shows −66 dBc amplitude at 410 kHz offset. Figure 6.9(c) shows the spectrum when three discrete pre-distortion components are applied, with the corresponding experimentally-measured values of −62 dBc, −70 dBc, and −76 dBc, again showing significant suppression and, importantly, no noticeable increase in the phase noise floor – which is an important advantage in comparison with many dithering techniques.



(a)

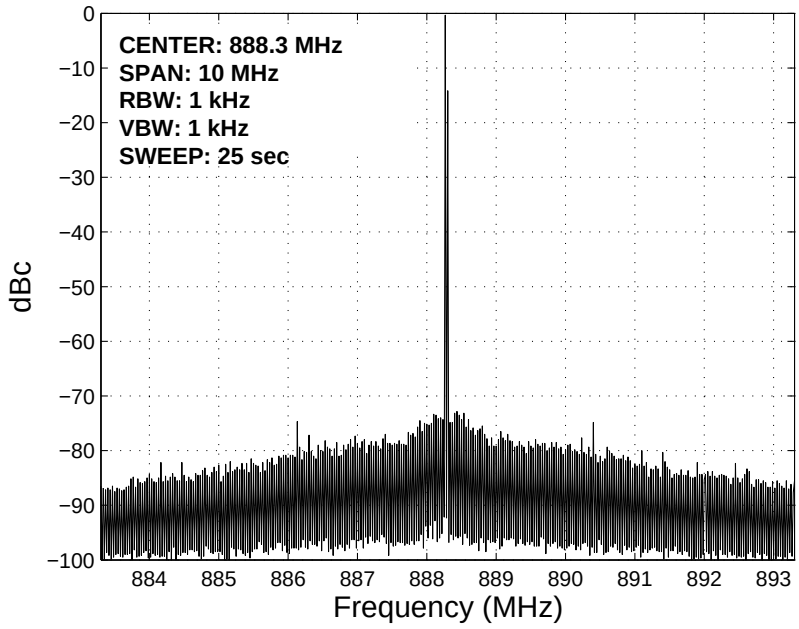


(b)

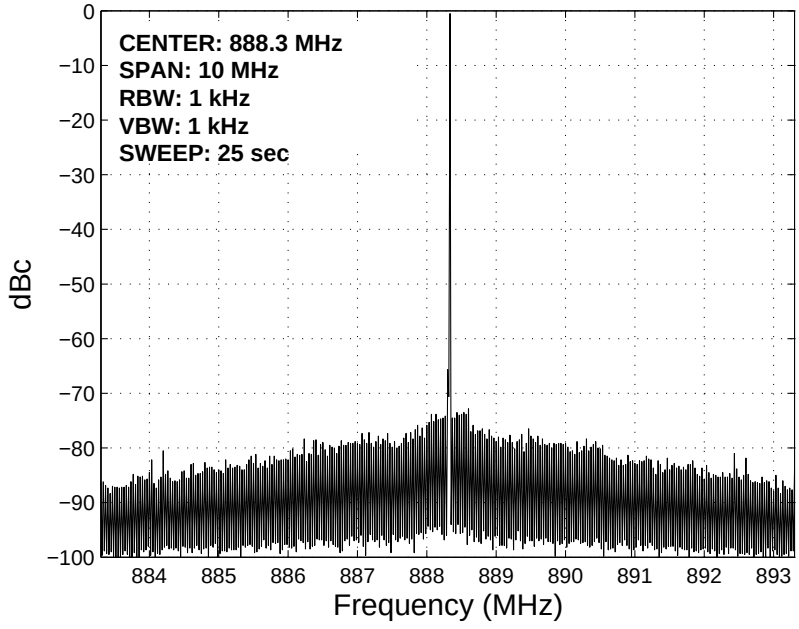


(c)

Figure 6.9 Measured spectra of a fractional-*N* synthesiser with 255/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency. (a) No pre-distortion. (b) Pre-distortion on first pair of sideband spurs. (c) Pre-distortion on all of sideband spurs.



(a)



(b)

Figure 6.10 Measured spectra of a fractional-*N* synthesiser with 471/1024 fractionality, 105 MHz reference frequency and 250 kHz loop natural frequency. (a) No pre-distortion signal. (b) Pre-distortion on sideband spurs.

The measured results have already shown that the proposed pre-distortion technique has ability to suppress high amplitude spurs caused by inadequate randomisation of Σ-Δ modulators and intermodulation effect. However, the majority of channels do not present such high spurious components. To demonstrate the pre-distortion effect on

small amplitude spurs, Figure 6.10 presents measured spectra with a random fractionality of 0.46. The double line of the carriers are caused by display resolution of the spectrum analyser, but not because of carrier instability. Figure 6.10(a) shows that two pairs of low spurs present on the spectrum: −78 dBc at 1.9 MHz offset and −74 dBc at 2.1 MHz offset respectively. Figure 6.10(b) shows the spectrum when two discrete pre-distortion components are applied, with the corresponding experimentally-measured values of −79 dBc, −78 dBc. It is worth noting that there are two pairs of new spurs produced at twice the frequency offset, with amplitude of lower than −80 dBc. This phenomenon is caused by the same mechanism of quantisation noise leakage and Σ-Δ sequence truncation.

These results provide convincing evidence that the proposed technique introduced here – pre-distortion Σ-Δ noise shaping – is a valid solution to control fractional spurs in fractional-*N* synthesisers. This new approach is suitable for various designs with a simple single-bit quantizer and should be applicable to multi-bit modulator architectures. The digital block can be implemented by an FPGA according to different requirements, providing flexible performance in low noise synthesisers.

6.5 Summary

A new and original technique for suppressing fractional spurs in fractional-*N* frequency synthesisers has been presented, which is capable of alleviating the impact of close-in spurious components. The proposed technique utilises a series of low level sinusoidal signal components that are added to the input (normally DC) of a single-bit Σ-Δ modulator to generate a modified bitstream designed to cancel individual discrete spurs. The frequencies of these components are chosen to match the dominant fractional spurs and the amplitudes and phases optimised in order to suppress these components.

The modelled results demonstrate that single-bit quantizers are inclined to produce significant discrete spurious components. Analysis is presented to predict the benefits of applying appropriate pre-distortion components; this is subsequently validated against experimental results obtained from a synthesiser measurement arrangement in which a series of up to eight pre-distortion signal components are applied to the

modulator to cancel the principal fractional spurs. The measured results have shown a spectacular reduction in the discrete close-in fractional spurs, of up to 37 dB, with no enhancement of the phase noise floor.

The experimental results were achieved using a stored-sequence fractional-*N* synthesiser architecture, based on an FPGA implementation in which the cancelling components can be easily incorporated in the modulator architecture. This is, perhaps, the preferred practical method of implementing this technique, but is an entirely reasonable approach to use for demanding synthesiser applications, such as for mobile base stations. Using the proposed technique, fractional spurs arising from the modulator and any other circuit artifacts (such as intermodulation and cross-coupling effects) can be suppressed in an efficient and controlled manner, with no phase noise floor penalty, thus allowing the use of simpler single-loop synthesiser architectures in applications that would otherwise have required multi-loop solutions.

Chapter 7

Conclusions and Further Work

7.1 Conclusions

A fractional-*N* frequency synthesiser designing procedure has been described which is able to simultaneously achieve direct modulation at high data rates and excellent noise performance. This synthesiser is based on a traditional PLL indirect frequency synthesis architecture, with a high speed Σ-Δ modulator implemented by an FPGA, incorporation with an external frequency divider, a PFD, a VCO and a loop filter. In comparison to other fractional-*N* synthesiser designs based on a conventional low speed CMOS digital control component, this design has advantages of wider bandwidth, faster switching between frequencies, higher over-sampling rate, lower phase noise and lower spur levels.

As a very important part of fractional synthesisers, various kinds of Σ-Δ modulator are discussed, including most third order architectures. Higher order Σ-Δ modulators are widely used in A/D converters, but are difficult to use in synthesisers due to practical design considerations regarding cascaded delays and stability margin. To satisfy the stringent requirements of short settling time and low phase noise in GSM base stations, the synthesiser bandwidth is set to 250 kHz, which is impossible to implement in a conventional synthesiser due to the high close-in phase noise floor. To achieve good noise performance with a robust and simple design, a stored-sequence method is utilised to replace the conventional pipelined Σ-Δ modulator. Stored-sequence noise shaping is an attractive technique which offers a number of advantages in the implementation of low cost, high performance wireless communication systems. By the use of optimised Σ-Δ noise shaping sequences, a synthesiser can be constructed achieving an extremely high reference frequency which has inherent advantages in low noise, highly agile loop performance.

In addition to the Σ-Δ modulator, it has been shown that the frequency divider in the synthesiser can be also implemented by the same FPGA component. A new technique, memory-controlled frequency division, is proposed to generate a wider range of modulus values which can be continuously adjusted at high frequencies. A new programmable memory controlled frequency divider has been designed and implemented which is suitable for GSM systems. An extension of the technique has been shown that is capable of operation over a wide range of integer or fractional division ratios. The approach is particularly suited to FPGA or PLD implementation in which the entire synthesiser operation, including the divider and stored-sequence Σ-Δ modulator, can be achieved in one block. Furthermore the outputs of the fractional frequency divider are utilised as the compensating signals for fractional-*N* synthesis.

The techniques presented here can achieve high stability, low noise results. The simulated and measured results show that it is feasible to design a high performance fractional-*N* synthesiser based on a combination of a fast stored-sequence noise shaping and a programmable memory controlled divider. The noise shaping is efficiently implemented by using a ROM to store the individually optimised digital sequences covering full channels of GSM or DCS systems.

To provide proof of concept of these methods, a 900 MHz fractional-*N* synthesiser was built in two modules: an FPGA evaluation board as a platform for Σ-Δ noise shaping; a printed circuit board integrating discrete components of the synthesiser. The reference frequency of the synthesiser was set to 105 MHz and the natural frequency to 250 kHz. A single-stage third order feedback Σ-Δ modulator is used with the division ratio limited to between 8 and 9. This synthesiser has measured phase noise of −113 dBc/Hz at 10 kHz offset, presenting significant improvement in contrast to conventional fractional-*N* synthesisers in mobile handsets with 13 MHz reference frequency. This new design can be used to replace integer “ping-pong” synthesisers in GSM base stations which consist of two separate integer-*N* synthesisers.

A further contribution of this research is on a new phenomenon in frequency synthesis, first reported in 2003 [99], which is capable of producing a series of close-in spurious components of similar distribution to the well-known fractional spurs usually attributed solely to modulator operation. The mechanism is based on small degrees of cross-coupling and/or intermodulation and subsequent phase detector aliasing of the non-

harmonically related components necessarily present in such synthesisers. Numerical and analytic modelling has been developed to predict the amplitudes and frequencies of the components produced by this process, demonstrating that modest degrees of VCO-to-phase detector cross-coupling can produce substantial effects.

An experiment has been successfully conducted for the first time, attempting to validate the existence of the intermodulation effect and finally cancel the VCO to phase detector cross-coupling responsible for this phenomenon. The intermodulation effect has been convincingly demonstrated by experimental results obtained from a synthesiser measurement arrangement, in which a controlled amplitude of VCO signal is cross-coupled to the phase detector input. The measured results have shown good agreement with predictions. An experimental arrangement based on a phase compensation technique is proposed to remove or reduce coupling and intermodulation-borne spurs. The measured results successfully show that these spurious components may be effectively suppressed, by some 18 dB, with appropriate adjustment of the amplitude and phase of the cancelling path. This new technique is suitable for almost all fractional-*N* synthesisers and may have real value in reducing the level of fractional spurs and thus improving spectral purity.

Although the analogue cancellation of phase compensation technique is a valid solution to suppress intermodulation-borne spurs, it can not address fractional spurs introduced by any other reason, especially for single-bit modulators which are vulnerable to generate a family of discrete components. A new and original technique for suppressing fractional spurs in fractional-*N* frequency synthesisers has been presented, which is capable of suppressing close-in spurious components caused by the modulator and any other circuit artifacts (such as intermodulation and cross-coupling effects). The key innovation is the introduction in the bitstream generation process of carefully-chosen set of components at identical offset frequencies and amplitudes and in anti-phase with the principal fractional spurs. The proposed *pre-distortion technique* utilises a series of low level sinusoidal signal components that are added to the input (normally DC) of a single-bit Σ-Δ modulator to generate a modified bitstream designed to cancel individual discrete spurs. The frequencies of these components are chosen to match the dominant fractional spurs and the amplitudes and phases optimised in order to suppress these components.

Analysis is presented to predict the benefits of applying appropriate pre-distortion components; this is subsequently validated against modelled and experimental results obtained from a synthesiser measurement arrangement in which a series of pre-distortion signal components are applied to the modulator inputs to cancel the principal fractional spurs. The measured results have shown a spectacular reduction in the discrete close-in fractional spurs, of up to 37 dB, with no enhancement of the phase noise floor. This approach can be highly effective in improving spectral purity and reduction of spurious components caused by the Σ-Δ modulator, quantisation noise, intermodulation effects and any other circuit factors. The spur cancellation is achieved in the digital section of the synthesiser without introducing additional circuitry or any phase noise floor penalty. The pre-distortion signals are predicted by a simulation of dedicated Σ-Δ architectures, and then individually optimised noise shaping sequences are generated and stored in a ROM. This new technique allows the use of the same stored-sequence synthesiser architecture, rather than refining the synthesiser architecture or employing additional spur cancellation systems or multi-loop solutions. As an advanced dithering technique, this approach allows Σ-Δ modulators and A/D converters with single-bit quantizers to generate smooth noise shaping, which is a reasonable solution for demanding low noise synthesiser applications.

7.2 Future work

Future use of the synthesiser and noise suppression techniques would seem to be dependent on monolithic implementation which integrates the digital and RF elements. The digital element consists of a flash memory which stores a series of pre-generated noise shaping sequences and clocked out by the output of the frequency divider. A flash memory of at least 24 MBytes is necessary to fully cover 375 channels of DCS-1800 system. To fulfill the low phase noise requirement of cellular base stations, a discrete VCO can be used to achieve low noise performance. A highly integrated and economically viable solution should be easily possible with recent technologies, allowing an ideal frequency synthesis solution with a relatively simple architecture.

The aims of the further work fall into several areas. Firstly, the previous stored-sequence synthesiser work was not able to fully exploit the technique due to technological and component limitations at the time; as a result, the maximum output frequency was limited to 950 MHz and the prescaler division ratio was limited to 8 and 9. A divide-by-2/3 dual-modulus divider is ideal in this arrangement to obtain lowest possible phase noise. In this case, the reference frequency will be set to around 400 MHz for GSM-900 and 700 MHz for DCS-1800 respectively. There is no FPGA component that can meet this stringent requirement currently, but the next generation FPGA components implemented in 45 nm technology will definitely achieve higher processing speed. This requires the design of a very fast phase/frequency detector and suitable data multiplexing and pipelining to load the stored channel sequences into the divider. Circuit development would probably be based on fast FPGAs but with a clear route identified for future integration so that the majority of functions are performed on an ASIC with a minimum of external components. Suitable automated numerical methods would also be required to produce optimised bit sequences. This may initially involve optimisation of Σ-Δ weights for each channel of operation in order to give the best possible performance across the entire operating band, but then move on to explore more generic numerical techniques to realise given noise shaping profiles. This latter approach is more challenging but potentially very rewarding since it aims to achieve more control and better performance than is presently possible with Σ-Δ techniques.

A second area of further work is to explore higher order Σ-Δ modulators which can further push most of the quantisation noise to high frequency offsets and leave lower close-in noise. The third order Σ-Δ modulators used in the design are not sufficient to control out-of-band phase noise. Higher order single-stage architectures with 1-bit quantizers will significantly extend the sequence length though their stability margin is limited to a narrower range. Suitable modelling and mathematical analysis are mandatory to build an ideal topology and to select the coefficients, so that the quantisation noise is better shaped to reduce the phase noise floor of the synthesiser.

The measured results have already demonstrated that the out-of-band noise floor exceeds the GSM specification mask at some frequency offsets. This fact demands a higher order loop filter to attenuate phase noise beyond the cut-off frequency of the

synthesiser, without reducing its initial loop bandwidth. This problem is worthy of further scrutiny, perhaps leading to alternative filter topologies.

The phase noise modelling of chapter 3 highlights that the PFD noise dominates the synthesiser in-band phase noise. This is caused by the PFD waveform jitter, and it is severe at high sampling frequencies. A method of eliminating PFD jitter was not pursued as part of this thesis work, and is a subject of future research. A validated approach is to couple a small of Σ-Δ modulation signal onto the PFD output. The Σ-Δ modulator output is integrated by some defined function, then converted to analogue signal by a D/A convertor. The coupling signal is capable of compensating phase errors generated by the digital device and the PFD, and it can reduce both phase noise floor and spurious component. Furthermore, this phase interpolation technique can work with the stored-sequence approach carrying out in software, so circuit mis-matches which affect the performance of the phase interpolation technique is not an issue. In conjunction with the stored-sequence and pre-distortion techniques described in this thesis, it would be a possible solution to provide lower noise than exist designs.

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Appendix A

RF Board Design

A.1 Overview

A four layer printed circuit board was built as part of the prototype system. The board consists of two signal layers (top layer and bottom layer), one power plane and one ground plane. Most of signals are routed on the top signal layer because the gound plane below it can provide dielectric isolation. The bottom layer is mainly used for power regulation. Every component is powered by a dedicated voltage regulator so that potential cross-coupling effect through power supply can be alleviated. Several of the signals on the board run at frequencies around 1 GHz; their respective board traces are required to have 50 Ohms characteristic impedance. To achieve this impedance, these high frequency signals were routed on top signal layer with 19.2 mil wide traces, and a dielectric thickness of 10 mil was specified between the top signal layer and ground plane. An FR4 glass epoxy laminate ($\varepsilon_r = 4.5 \pm 0.2$) is used as the dielectric between all the board layers. Standard SMA connectors are used for reference frequency source and synthesiser output. An SMB interface is used for frequency divider and FPGA section conection.

A.2 Schematics and Layout

A schematic of RF section of the synthesiser prototype is shown in Figure A.1 and a corresponding part list shown in Table A.1. The RF section requires 3.3 V, 5 V and 6 V power supplies. The power comsumption of the frequency divider (UXM15P) is about 300 mW at an input frequency of 1 GHz. To maximise performance, the frequency divider and voltage regulator are attached to good heatsinks on the PC board. The contact area of the package paddle is maximised and contains an array of vias to aid thermal conduction to both a backside heatsink and an internal copper plane.

Layout of the PC board is shown in Figure A.2. Great care was taken in the layout of several sections of the board, especially the high frequency RF section of the board. The RF section comprises components that are operating at 1 GHz with risetimes on the order of nanoseconds. All traces are kept to the minimum possible length, and sized to have 50 Ohms characteristic impedance where indicated. Also, sharp corners have been avoided. Furthermore, traces are avoided to be routed closely and cause signal coupling.

Grounding is always the most important part in RF board design, improper grounding will introduce unexpected noise although other factors are carefully considered. In regards to the grounding strategy, the top and bottom layers are filled by solid copper around signal traces and they are connected to the ground plane at numerous points using through holes.

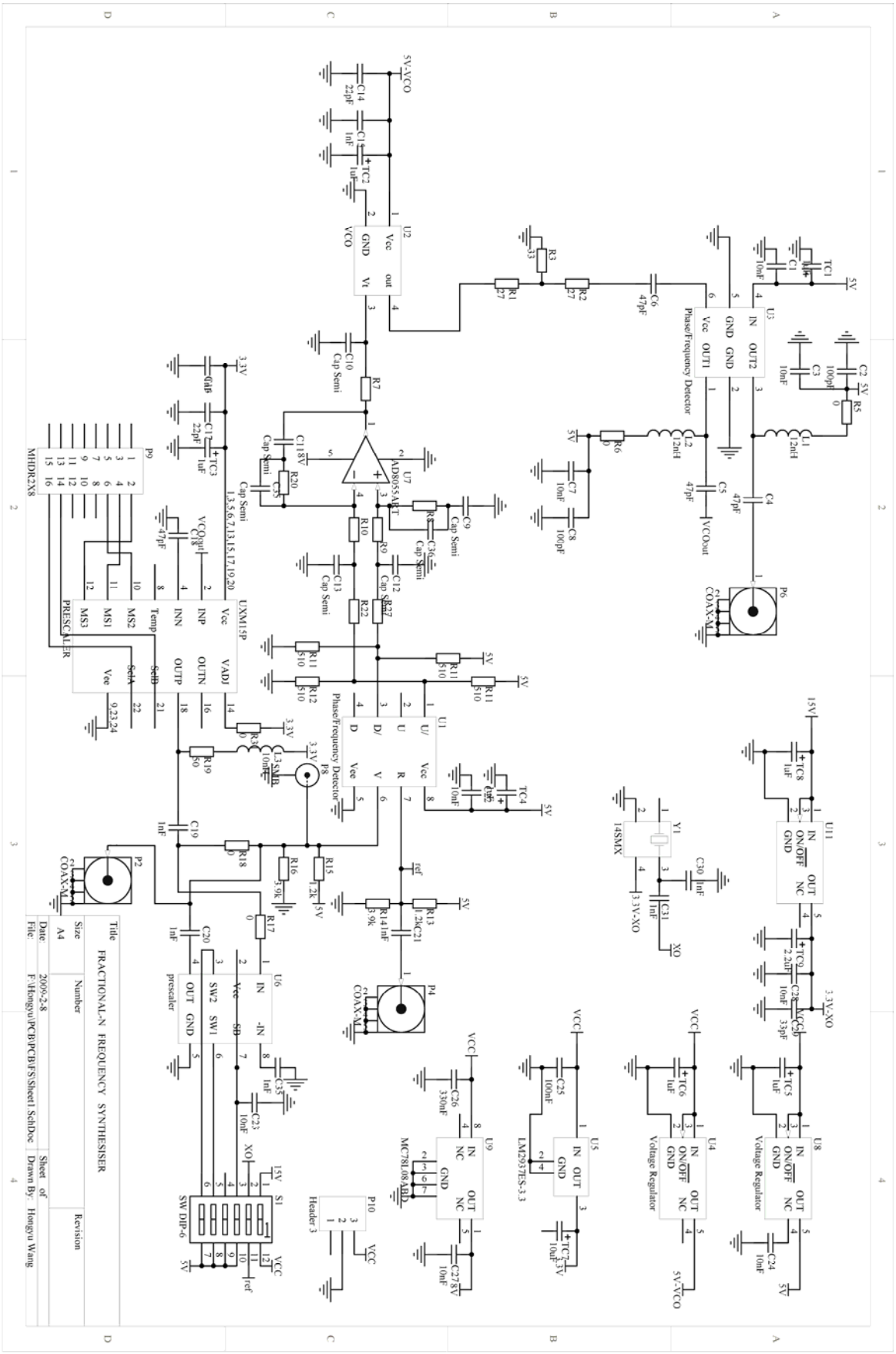
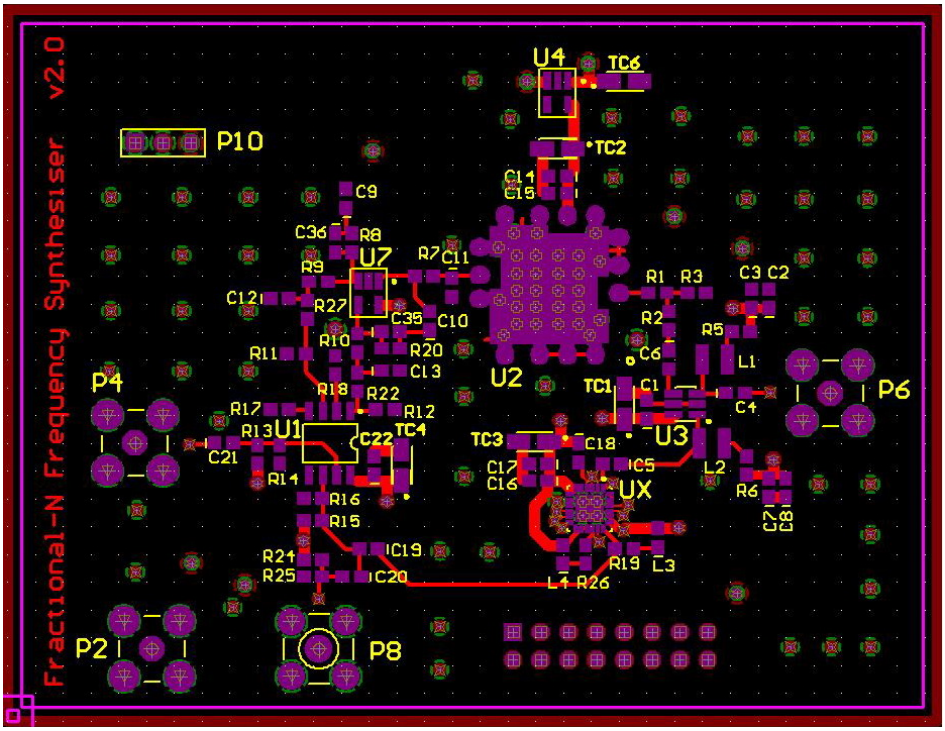


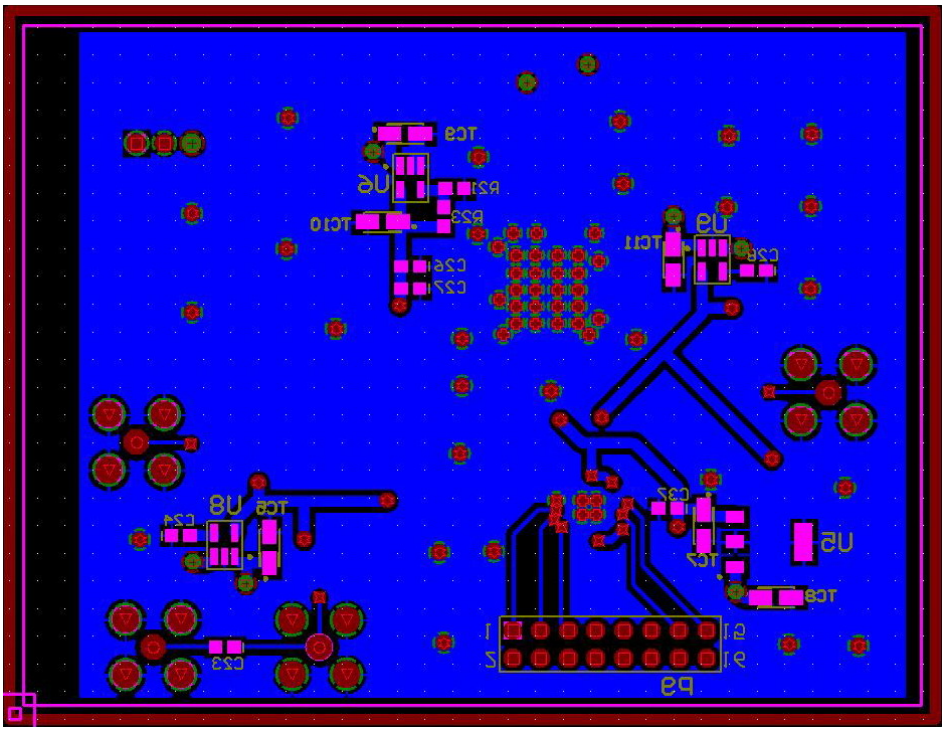
Figure A.1 Schematic of the frational-*N* synthesiser prototype.

Table A.1 Part list of PC board in prototype.

Part Number	Value	Description
C14, C16, C28	22pF	Capacitor 0603
C35, C36	33pF	Capacitor 0603
C4, C5, C6, C18	47pF	Capacitor 0603
C12, C13	68pF	Capacitor 0603
C3, C7, C10, C26, C33, C34, C40	100pF	Capacitor 0603
C15, C17, C19, C21, C23, C29, C31, C32, C37, C39	1nF	Capacitor 0603
C9, C11	2.2nF	Capacitor 0603
C1, C2, C8, C22, C24, C27, C38	10nF	Capacitor 0603
C20, C30		Capacitor 0603
R5, R6, R17,R23, R31	OR	Resistor 0603
R1, R2	27R	Resistor 0603
R3	33R	Resistor 0603
R19, R24	50R	Resistor 0603
R11, R12	510R	Resistor 0603
R7	910R	Resistor 0603
R8. R9. R10, R20, R22, R27	1.1K	Resistor 0603
R13, R15	1.2K	Resistor 0603
R14, R16	3.9K	Resistor 0603
R21	560K	Resistor 0603
R17, R28, R29		Resistor 0603
TC1, TC3-6, TC8, TC12, TC13	1uF	Tantalum Capacitor (Surface Mount)
TC2, TC9, TC10	2.2uF	Tantalum Capacitor (Surface Mount)
TC11	4.7uF	Tantalum Capacitor (Surface Mount)
TC7	10uF	Tantalum Capacitor (Surface Mount)
U1		PHASE/FREQUENCY DETECTOR
U2		VCO (Z-COMM)
U3		VCO BUFFER
U4		50 mA Ultra Low-Dropout Regulator
U5		500 mA Low-Dropout Regulator
U6		PRESCALER
U7		OP-AMP
U8		150 mA Ultra Low-Dropout Regulator
U9		Positive Voltage Regulator
U11		50 mA Ultra Low-Dropout Regulator
UX		PRESCALER
Y1		Surface Mount Quartz Crystal
L3, L4	100nH	Inductor
L1, L2	12nH	Inductor
P2, P4, P6		RF Coaxial PCB Connector, 50 Ohm Impedance
P8		SMB Straight Connector



(a)



(b)

Figure A.2 Layout of the frational-*N* synthesiser prototype. (a) Top layer. (b) Bottom layer.

Appendix B

Matlab Routines

This appendix includes the code of a number of matlab/simulink simulations which are used in all aspects of the design, analysis, noise prediction and optimisation of the novel synthesiser and its noise investigations.

B.1 Sigma-delta PSD Simulation

```
% Simulink of sigma-deltas and Power Spectral Density.

clear
close all

desired_input=471/1024+2^-17+2^-20;
nn=2^18;     % sampling points.
k=984;       % sigma-delta sequence truncation.
m=nn/2+k;    % truncation factor for startup
simpoints=nn+k;
fref=105e6;  % reference frequency.

actual_input=round(desired_input*m)/m;      % nearest available input value

invec=ones(1,nn+k);
invec=invec'.*actual_input;     % vector input to modulator
timevec=(linspace(1,nn+k,nn+k))';     % simulink requires time next.
inmat2(:,1)=timevec;     % fill up the simulink matrix
inmat2(:,2)=invec;

% call simulink model.
sim('third_feedback',simpoints);
Vc(1:nn)=bitstream(1+k:nn+k);  % sigma-delta output sequence.
sum=cumsum(Vc);

%dlmwrite('pm34.coe',Vc,'delimiter','\n','precision','%1d');

figure(1);
stairs(Vc);        % plot time domain modulator output
axis([5001 51100 -1 2]);
grid;
xlabel('Sample point','fontsize',12);
ylabel('Modulator output','fontsize',12);
% title('time domain modulator output','fontsize',14);

% figure(3);
```

```
% stairs(Vc);      % plot time domain modulator output
% axis([131072 131171 -1 2]);
% grid;

DC=mean(Vc);
V=Vc-DC;     % remove DC component

l=length(V);

deltaphi=2*pi*cumsum(V);
meandeltaphi=mean(deltaphi);
deltaphi1=deltaphi-meandeltaphi;
V=2*V.*transpose(hanning(l));

deltaphi1=2*deltaphi1.*transpose(hanning(l));
psd=pwelch(V,l,[],[],fref,'twosided');       %power spectrum density
mag=10*log10(psd);                                %log scale
mag=mag';
mag=mag+10*log10(fref/l);


out_len=length(V);
f=[0:1/out_len:1-1/out_len]; % vector to form the frequency axis

z=exp(j*2*pi.*f);

%y=(z-1)./z;             %first order
%y=((z-1).^3)./(z.^3);         %MASH 1-1-1
%y=((z-1).^4)./(z.^4);         %MASH 1-1-1
y=((z-1).^3)./(z.^3+22*(z.^2)-37*z+15);  %third-order single-stage with
feedback
y=y.^2;
y=y/nn;
y=10*log10(y);

figure(2)

semilogx(f,mag,f,y);
grid on;
xlabel('Normalised frequency, f/fref','fontsize',12)
ylabel('Quantisation noise (dB)','fontsize',12)
axis([0.0001 0.5 -250 0]);
```

B.2 Coupling-induced VCO Discrete Spurs

```
% Computes VCO discrete spurs due to VCO cross-talk onto phase detector input

clear
close all

% define parameters
A=0.01;                          % relative level of cross-talk
N=1024*64;                        % number of samples

%fs=1.8092e9*2;
fs=20e6;

P=90;                            % prescaler lower ratio
fmin=1805e6;                     % lower limit of band
fmax=1880e6;                     % upper limit of band
fref=(fmin+fmax)/(2*P+1)         % fref set so that division ratio = p+0.5 in
midband

fref=20e6                        % enter desired fref here directly, if
required         %%%%%%
fout=1809.2e6                        % desired fout
desiredpq=fout/fref-P;           % desired p/q value
desiredpq=0.46                   % enter desired pq here directly, if required
%%%%%%
actualpq=round(desiredpq*N)/N;  % nearest available p/q value so that p/q*NN
is integer
pq=actualpq;
k=P+actualpq

t(1:N)=1:N;

% calculate deltat using Newton iterative method
for n=1:N
deltat(n)=0;
    for m=1:6;
        resultant=sin(2*pi*deltat(n))+A*sin(2*pi*k*(t(n)+deltat(n)));

resultantdash=2*pi*(cos(2*pi*deltat(n)))+2*pi*k*A*cos(2*pi*k*(t(n)+deltat(n)));
%        resultant=A*sin(2*pi*(1/k)*(t(n)+deltat(n)))+sin(2*pi*deltat(n));
%
resultantdash=2*pi*(1/k)*A*(cos(2*pi*(1/k)*(t(n)+deltat(n))))+2*pi*cos(2*pi*de
ltat(n));
        deltat(n)=deltat(n)-resultant/resultantdash;
    end
end
deltaphi=2*pi*deltat;
deltaphi=(1/k)*deltaphi;

% take FFT and scale by factor of k to allow for loop multiplication of phase
jitter
l=length(deltaphi);
spec=(2/l)*fft(deltaphi);
spec=k*abs(spec);

% -6dB narrow-band PM conversion - giving output spectrum in absence of any
loop filter
spec=spec/2;
spec=20*log10((spec+10e-11));
```

```
% third order loop transfer function
f=[0:1/l:1-1/l];
%f=[0:1/l:1-1/l]*fs;

phi=pi/3;                       % desired phase margin
fn=100e3;                       % desired loop natural frequency
fn=fn/fref;                     % normalise loop natural frequency
fn=fn/fout;
T=tan(phi)+sec(phi);
ff=f/fn;
response=(1+T*T*ff.*ff)./((1-T*ff.*ff).*(1-T*ff.*ff)+(T*ff-ff.*ff.*ff).*(T*ff-
ff.*ff.*ff));
response=response.^0.5;
response=20*log10(response);

% apply third order loop response
spec2=spec+response;

% find maximum spur level and frequency at which it occurs
[r,s]=max(spec);
maxspurdbc = r
atfreqoverfref = s/l

% plot
figure
axes('box', 'on', 'fontsize', 12)
%semilogx(f,spec,f,response)
plot(f,response,f,spec)
%axis([0,0.5*fref,-200,0])
title('spurs due to -20 dB VCO cross-talk to PFD, fout = 1825 MHz , fn = 250
kHz, divide ratio = 8.419', 'fontsize',11)
xlabel('Frequency/fref', 'fontsize',12)
ylabel('Spurious level, dBc', 'fontsize',12)
```

B.3 Synthesiser Phase Noise Simulation

```
% Computes bitstream and resulting spectrum for hopping/burst operation
% (no adjustment to desired pq value)

clear
close all

% define p/q, fref and no. of samples
nn=1024*128
fmin=1805e6;
fmax=1880e6;
fref = (fmin+fmax)/17

%desired fout in MHz

fout=1825e6
desiredpq=fout/fref-8
actualpq=round(desiredpq*nn)/nn         %nearest available p/q value
pq=actualpq;
k=984               % gives meandeltaphi~0
% define prescaler modulation waveform

Vc=zeros(1,nn+k);
b=zeros(1,nn+k);
d=zeros(1,nn+k);
f=zeros(1,nn+k);
x=0;

% third order sigma-delta
aa=8;
bb=16;
for n=2:nn+k;
%   if round(n/4096)-n/4096 == 0
%       Count = n/1024
%   end

    b(n)=b(n-1)+pq-x;
    d(n)=d(n-1)+b(n)-aa*x;
    f(n)=f(n-1)+d(n)-bb*x;
    if f(n) > 0.5
        Vc(n)=1;
        x=1;
    else
        Vc(n)=0;
        x=0;
    end
end

figure(1)

stairs(d);
axis([0 131072 -10 20]);
grid on

fmax=max(d)
fmin=min(d)

Vcy=Vc;

Vcx(1:nn)=Vc(1+k:nn+k);
```

```
Vc=Vcx;

% integrate frequency steps to get phase steps (with zero mean value)
l=length(Vc);
meanVc= mean(Vc)
deltaphi=2*pi*cumsum(Vc-pq);
meandeltaphi=mean(deltaphi);
deltaphi=deltaphi-meandeltaphi;

excess1bits=nn*(meanVc-actualpq)

% take spectrum of phase modulation due to the prescaler modulation waveform
fn=(2/l)*fft(deltaphi);

% -6dB narrow-band PM conversion - giving output spectrum in absence of any
loop filter
fn=fn/2;
mag=10*log10((fn.*conj(fn)+10e-11));

% convert to dBc/Hz by dividing by FFT resolution (fref/l)
mag=mag-10*log10(fref/l);
f=[0:1/l:1-1/l];

% third order loop transfer function
phi=pi/3;
% normalised loop natural frequency
fn=250e3;
fn=fn/fref;
T=tan(phi)+sec(phi);
ff=f/fn;
response=(1+T*T*ff.*ff)./((1-T*ff.*ff).*(1-T*ff.*ff)+(T*ff-ff.*ff.*ff).*(T*ff-
ff.*ff.*ff));
response=response.^0.5;
response=20*log10(response);

% apply third order loop response
mag2=mag+response;

[s,t]=max(mag2);

dB=10*log10(fref/l);
maxspurdbc = s + dB
atfreq = t*fref/nn

figure(2)
axes('box', 'on', 'fontsize', 12)
%semilogx(f,mag, f, response, f, mag2)
semilogx(f,mag2)

% DCS mask
xmask=[1e5/fref 2e5/fref 2e5/fref 2.5e5/fref 2.5e5/fref 4e5/fref 4e5/fref
6e5/fref 6e5/fref 12e5/fref 12e5/fref 18e5/fref 18e5/fref 6e6/fref 6e6/fref
0.5];
ymask=[-44 -44 -75 -75 -78 -78 -105 -105 -115 -115 -118 -118 -125 -125 -130 -
130];
yymask=[0.5-dB 0.5-dB -30-dB -30-dB -33-dB -33-dB -60-dB -60-dB -70-dB -70-dB
-73-dB -73-dB -75-dB -75-dB -80-dB -80-dB];
line(xmask, ymask, 'color', 'r')
line(xmask, yymask, 'color', 'r')
axis([0.001,0.5,-150,-30])
title('3rd order sigma-delta, pq=0.673, natural frequency fn = 250 kHz, A=8, B
= 16', 'fontsize',12)
xlabel('Frequency/fref', 'fontsize',12)
ylabel('Phase noise dBc/Hz', 'fontsize',12)
grid on
```

B.4 Closed Loop Response

```
% Third order type 2 loop filter closed and open loop complex phase response

clear
close all

f=linspace(1000,1000e5,100000);% frequency range
omega=2*pi.*f;     % natural frequency range
sigma=zeros(1,length(f));
s=sigma+j.*omega;
f_nat=250e3;
omega_nat=f_nat*2*pi; % loop natural frequency
w=omega_nat;

% loop phase margin in radians
phi=pi*60/180;
phi2=pi*45/180;
phi3=pi*30/180;

% ECL phase detector levels
Vo_h=4;
Vo_l=3.2;
swing=(Vo_h-Vo_l);

% phase detector gain volts per radian
Kp=swing/(2*pi);

% VCO gain in Radians/volt.
Kv=29e6*2*pi;

% loop divider
N=73.5;

% loop filter time constants
T1=(Kp*Kv/(N*(omega_nat)^2))*(tan(phi)+sec(phi));
T2=1/(omega_nat * (tan(phi)+sec(phi)) );
T3=(tan(phi)+sec(phi))/omega_nat;

% calculate loop filter gain and phase
G=(1./(s.*T1)).*(1+s.*T3).*(1./(1+s.*T2));
f_path=(G./s).*(Kp*Kv);
loop_gain=(G./s).*(Kp*Kv/N);
phase_resp= (f_path)./(1+loop_gain);

T12=(Kp*Kv/(N*(omega_nat)^2))*(tan(phi2)+sec(phi2));
T22=1/(omega_nat * (tan(phi2)+sec(phi2)) );
T32=(tan(phi2)+sec(phi2))/omega_nat;

% calculate loop filter gain and phase
G2=(1./(s.*T12)).*(1+s.*T32).*(1./(1+s.*T22));
f_path2=(G2./s).*(Kp*Kv);
loop_gain2=(G2./s).*(Kp*Kv/N);
phase_resp2= (f_path2)./(1+loop_gain2);

T13=(Kp*Kv/(N*(omega_nat)^2))*(tan(phi3)+sec(phi3));
T23=1/(omega_nat * (tan(phi3)+sec(phi3)) );
T33=(tan(phi3)+sec(phi3))/omega_nat;

% calculate loop filter gain and phase
G3=(1./(s.*T13)).*(1+s.*T33).*(1./(1+s.*T23));
```

```
f_path3=(G3./s).*(Kp*Kv);
loop_gain3=(G3./s).*(Kp*Kv/N);
phase_resp3= (f_path3)./(1+loop_gain3);

%semilogx(f,20*log10(abs(phase_resp)),f,20*log10(abs(phase_resp2)),f,20*log10(
abs(phase_resp3)));
grid
% hold
semilogx(f,angle(phase_resp)*180/pi,f,angle(phase_resp2)*180/pi,f,angle(phase_
resp3)*180/pi);
% title('Closed Loop Complex Phase Response');
xlabel('Frequency /Hz');
ylabel('Amplitude /dB, Phase /degrees');

figure(2)
semilogx(f,20*log10(abs(loop_gain)));
grid
hold
semilogx(f,angle(loop_gain)*180/pi);

title('Open Loop Complex Phase Response');
xlabel('Frequency /Hz');
ylabel('Amplitude /dB, Phase /degrees');

figure(3)
theta=angle(loop_gain);
rho=abs(loop_gain);
polar(theta(100:10000),rho(100:10000));
title('Nyquist Plot of Open Loop Complex Phase Response')
R2C1 = 2 * tan(phi)/omega_nat; % T3 (ns)
R1C1 = Kp * Kv / N / omega_nat^2 * (tan(phi) + 1/cos(phi)); % T1 (ns)
R2C2 = 1/(omega_nat *(tan(phi) +1/cos(phi))); % T2 (ns)
R2 = 1e3; % resistor in the op amps feedback path
C1 = R2C1 / R2; % capacitor in feedback path in series with R2 and C2
R1 = R1C1 / C1; % resistor at the op amp input.
C2 = R2C2 / R2; % capacitor in parallel with R2
disp('');
disp(['C1 = ' num2str(C1*1e12) 'pF']);
disp(['R1 =' num2str(R1) ' ohms']);
disp(['C2 = ' num2str(C2*1e12) 'pF']);
disp(['R2 = ' num2str(R2) ' ohms']);

s=[0.1*w 10*w 0.01*w];
fm=(s.^3+w*(tan(phi)+sec(phi))*s.^2)/(s.^3+w*(tan(phi)+sec(phi))*s.^2+w.^2*(ta
n(phi)+sec(phi)*s+w.^3));

figure(4)
semilogx(s/w,fm);
grid

title('Frequency Modulation');
xlabel('Frequency /Natural Frequency');
ylabel('Response /dB');
```

B.5 Step Response of PLLs*

```
%*This Program is written by Farhat Masood, College of Electrical and
Mechanical Engineering, NUST.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%The phase locked loop(PLL),adjusts the phase of a local oscillator
%w.r.t the incoming modulated signal.In this way,the phase of the
%incoming signal is locked and the signal is demodulated.This scheme
%is used in PM and FM as well.
%We will implement it by using a closed loop system.Control systems
%techniques are applied here.
%************************************************************


%STEP RESPONSE OF THE FIRST ORDER CLOSED LOOP TRANSMITTANCE OF PLL
%H(S) = 1;
%SYSTEM TYPE NUMBER = 1;
%THETAo/THETAi (output phase/input phase)


close all
kv = 1;
kd = 1;
dt = 0.01
t = 0:dt:2
u = ones(1,length(t))
g11 = [tf([2*pi*kv*kd],[1 2*pi*kv*kd])]  %its the transfer function given in
the handout
[y11 t] = lsim(g11,u,t)
figure
plot(t,y11)
xlabel('TIME IN SECONDS')
ylabel('AMPLITUDE')
title('STEP RESPONSE OF 1st ORDER CLOSED LOOP TRANSMITTANCE')
%************************************************************


%STEP RESPONSE OF THE FIRST ORDER CLOSED LOOP ERROR TRANSMITTANCE OF PLL
%ALL THE OTHER FACTORS H(S) etc ARE SAME HERE
%THETAe/THETAi (same interp. as above)

g12 = [tf([1 0],[1 2*pi*kv*kd])]   %error transmittance given in the handout
[y12 t] = lsim(g12,u,t)
figure
plot(t,y12)
xlabel('TIME IN SECONDS')
ylabel('AMPLITUDE')
title('STEP RESPONSE OF 1st ORDER CLOSED LOOP ERROR TRANSMITTANCE')
%************************************************************

%STEP RESPONSE OF THE FIRST ORDER CLOSED LOOP TRANSMITTANCE OF PLL
%BETWEEN VCO AND INPUT SIGNAL PHASE
%H(S) = 1;
%SYSTEM TYPE NUMBER = 1;
%V2/THETAi
Kd =1;
g13 = [tf([Kd 0],[1 2*pi*kv*kd])]   %vco voltage and input signal
transmittance
[y13 t] = lsim(g13,u,t)
figure
```

```
plot(t,y13)
xlabel('TIME IN SECONDS')
ylabel('AMPLITUDE')
title('STEP RESPONSE OF 1st ORDER CLOSED LOOP TRANSMITTANCE B/W VCO AND INPUT
PHASE')
%*********************************************************************

%STEP RESPONSE OF THE SECOND ORDER CLOSED LOOP TRANSMITTANCE OF PLL
%SYSTEM TYPE NUMBER = 2;
%THETAo/THETAi

a = 3.15
zeta = sqrt((pi*kv*kd)/(2*a))
omegan = sqrt(2*pi*kv*kd*a)
g21 = [tf([2*zeta*omegan omegan^2],[1 2*zeta*omegan omegan^2])]
[y21 t] = lsim(g21,u,t)
figure
plot(t,y21)
xlabel('TIME IN SECONDS')
ylabel('AMPLITUDE')
title('STEP RESPONSE OF SECOND ORDER CLOSED LOOP TRANSMITTANCE OF PLL')
%*********************************************************************

%STEP RESPONSE OF THE SECOND ORDER CLOSED LOOP ERROR TRANSMITTANCE OF PLL
%SYSTEM TYPE NUMBER = 2;
%THETAe/THETAi

g22 = [tf([1 0 0],[1 2*zeta*omegan omegan^2])]
[y22 t] = lsim(g22,u,t)
figure
plot(t,y22)
xlabel('TIME IN SECONDS')
ylabel('AMPLITUDE')
title('STEP RESPONSE OF SECOND ORDER CLOSED LOOP ERROR TRANSMITTANCE OF PLL')
%*********************************************************************

%STEP RESPONSE OF THE SECOND ORDER CLOSED LOOP TRANSMITTANCE OF PLL
%BETWEEN VCO AND INPUT SIGNAL PHASE
%SYSTEM TYPE NUMBER = 2;
%V2/THETAi

g23 = [tf([kd kd*a 0],[1 2*pi*kv*kd 2*pi*kv*kd*a])]
[y23 t] = lsim(g23,u,t)
figure
plot(t,y23)
xlabel('TIME IN SECONDS')
ylabel('AMPLITUDE')
title('STEP RESPONSE OF SECOND ORDER CLOSED LOOP TRANSMITTANCE B/W VCO AND
INPUT PHASE')
%*********************************************************************
```