Polymer Multimode Waveguide Optical and Electronic PCB Manufacturing

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ABSTRACT

The paper describes the research in the £1.3 million I*e*MRC Integrated Optical and Electronic Interconnect PCB Manufacturing (OPCB) Flagship Project in which 8 companies and 3 universities carry out collaborative research and which was formed and is technically led by the author. The consortium's research is aimed at investigating a range of fabrication techniques, some established and some novel, for fabricating polymer multimode waveguides from several polymers, some formulations of which are being developed within the project. The challenge is to develop low cost waveguide manufacturing techniques compatible with commercial PCB manufacturing and to reduce their alignment cost. The project aims to take the first steps in making this hybrid optical waveguide and electrical copper track printed circuit board disruptive technology widely available by establishing and incorporating waveguide design rules into commercial PCB layout software and transferring the technology for fabricating such boards to a commercial PCB manufacturer. To focus the research the project is designing an optical waveguide backplane to tight realistic constraints, using commercial layout software with the new optical design rules, for a demonstrator into which 4 daughter cards are plugged, each carrying an aggregate of 80 Gb/s data so that each waveguide carries 10 Gb/s.

Keywords: Polymer Waveguide, Design Rules, Fabrication, Modeling, Multimode, Switch Fabric Demonstrator, crossings, 90° bends, straight tapers, bent tapers, photolithography, laser ablation, laser direct write, ink jet printing

1. INTRODUCTION AND MOTIVATION

Leading computer companies such as Hewlett Packard are investigating optical interconnections for use on silicon chip integrated circuits. Ray Beausoleil [1] in his plenary paper clearly outlines the motivation: As transistors and logic gates have become smaller, more have been packed onto integrated circuits. John E. Cunningham of Sun Microsystems [7] suggested that according to Moore's law, a doubling of the number of transistors on a chip was expected every 18 months and that actually this has occurred every 2 years. A doubling of performance has been achieved every two years until recently, mainly by increases in clock speed [3]; however, clock speed is no longer increasing at the same rate [1]. Various benchmarking programs have been run and these have shown a linear dependence of performance on clock speed [1]. However, there is currently about a 0.1 GHz increase in clock speed every 18 months. The maximum distance a clock pulse travels on a chip in one clock cycle is the clock radius. The clock radius is now much less than the size of a chip. Therefore, the chips have been divided into 1, 4, 6, 8 and soon 16 processor cores within each of which the clock can travel in one cycle. All Intel products have been multi-core since late 2006 [3]. However, the chip begins to run out of real estate [7] for 8 cores are at the 2 cm reticule limit. Even as early as 2007 Intel demonstrated 80 core chip operating at 60 W at 1 Teraflop as a supercomputer in a desktop, however, this was not product, due to impractical trade-offs made in the design, but it demonstrated what was possible [3]. The ITRS roadmap expects that by 2017 there will be 256 cores on a chip. This may result in an increase in performance but only for highly parallel problems. The multiple cores must be highly interconnected with high bandwidths of multiple Gb/s to cache memory on-die [3] and vertical stacking is being investigated. Terabytes of data must be moved around on the die but this is thought not to be a problem [3]. The problem lies in the multiple off-die connectors via PCIe and Ethernet, for example [3], which interconnect the chips to one another and to hard disk storage. The number of electrical pins from a low cost organic package is 1000 and may be expected to increase to 3000. However, this is accompanied by an increase in insertion force and lack of planarity and further increases will not be fruitful [3]. The signals have to go from the silicon chip through multiple layers in the socket, through the backplane and back up again in the next chip. To achieve this, there has been an

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increase in the number of layers of copper tracks with large vias and amplifiers powering each interconnection. It can be done but it costs power for the 200 million devices being sold each year [3]. FR4 PCB material is limited to about 10-14 Gb/s for realistic costs. Minimum features on chip are shrinking from 45 nm to 22 nm and this is associated with an increase in Jitter on the silicon. At the moment, the increases in jitter are being absorbed by the timing margin but it is creating issues in high volume production. It may be better to get increases in speed by optimizing the software, adding more cache memory stages and putting memory on the CPU. For example, Multi-threading makes better use of the core [7]. Therefore, the highest data rates of 400 Gb/s could be to local 128 MByte cache memory, 40 Gb/s to a second level of 1 Gbyte cache memory further away and as low as 300 Mb/s to a third level of very large memories much further away. Every 4 years the PC architecture changes [3] and it is a large market of $7.5 billion.

For connections of less than 1 mm, copper tracks may serve well but for distances over 1 mm it is more efficient to use CMOS compatible optical interconnects. In 1997 David Miller [2] discussed the scaling laws for copper interconnects and showed that the bandwidth is fixed unless more copper tracks are made, making the interconnect density an important consideration. The power consumed is given by the product of the capacitance, the voltage squared and the clock frequency [3]. This implies that it is better to have many small cores rather than one large core [3]. Over-clocking the core gives better performance but at an increased power penalty cost while under-clocking gives worse performance but saves power. Expenditure of power is a strong driver [3]. One third of the computer power is expended in spreading the clock around. Optical interconnects have a wide bandwidth which is not as dependent on length of interconnect as for copper tracks and more than one signal can be multiplexed onto one line, for example, by DWDM. Jerry Bautista of Intel [3] expects that the highest bandwidths of 100 Gb/s will be needed between a CPU array and DIMMS bulk memory, that bandwidths of 10 Gb/s are needed between the multiple cores and Hard Disk Storage and that lower bandwidths of 1 Gb/s are needed between boxes, shelves or rack units. It it the connections on the backplane between multiple cores and hard disk memory at 10 Gb/s that we concentrate on in this paper and in the OPCB project together with the Hard Disk rack unit supplier, Xyratex Technology. Jerry Bautista of Intel [3] noted that the IBM Roadrunner became more reliable once optical input and output had been implemented. It was expected two years ago that optical interconnects would be in use by 2010 so we only have one year to meet that target. However, meeting a low cost target is more important than meeting a Telcordia specification on environmental and aging tests [3].

Printed Circuit Boards have served well as a means to connect current integrated circuits to one another and to other electronic components by means of copper tracks. So we may consider whether optical interconnects can be formed on such boards to form interconnections rather as copper track do today. However, these new types of printed circuit board cannot just have optical interconnections as power must also be routed to chips and only copper tracks can carry this. So a new type of hybrid printed circuit board having both optical and electrical connections must be designed and new ways to manufacture such a board must be developed. In order for the optical interconnections to supplant the copper tracks, the manufacturing techniques for this Optical Printed Circuit Board (OPCB) need to be readily adapted for mass, low cost production. Jeffrey A. Kash of IBM Thomas J Watson Research Center and Jerry Bautista of Intel [3] expects that ultimately a cost of 1$/Gb/s needs to be achieved [4]. In addition, the optical interconnections must be arranged, particularly at connectors, to provide denser and higher aggregate bandwidth [5]. The optical power budget should ideally be about 8 dB as that is what is in the specification for 10 Gb/s Ethernet in order for it to be compatible. Therefore, the optical interconnections were chosen to be polymer waveguides as these have low loss at the low cost VCSEL wavelength of 850 nm and can readily be fabricated at low cost in mass production and several different fabrications techniques exist. Phillippe M. Fauchet of University of Rochester [6] has carried out computer modeling to calculate latency delay, bandwidth density, power × delay product and jitter. These suggest that DWDM is required if optical interconnects are to achieve the high density and aggregate data rates in a small volume to compete with copper tracks. John E. Cunningham of Sun Microsystems also adds to these cooling and complexity [7] and points out that optical jitter can arise from coherent noise from optical multiple reflections between facets and quotes the figure of merit Power/(Payload length)/(Delivery time) of picoJoule per useful bit. In this paper, we begin by examining mainly experimentally a single layer of waveguides at one wavelength, as the design is scalable to multiple layers and wavelengths later.

2. THE I*E*MRC OPCB PROJECT

Our vision is that a complete route to market needs to be developed to allow current PCB designers to design the new OPCBs without the need for much extra training and that PCB manufacturers will also be able to fabricate the new type of OPCBs without the need for major costly changes to their existing production lines. This is an ambitious goal and cannot be achieved in a single small project as it represents the full introduction of a new disruptive technology to the whole electronics industry. However, in one project we can hope to make some progress towards this goal and to identify the challenges that need to be tackled. In order to do that the author brought together several companies as representatives of typical industries along this chain to market and a number of university experts having specialist technical knowledge.

As our end user companies who demand that such a technology be developed we chose Xyratex Technology who assembles and delivers high quality Terabyte storage systems, BAE Systems who develop avionic systems for aircraft such as the Eurofighter Typhoon and Renishaw who develop and sell optical sensors. The software developed and sold by Cadence is in widespread use for laying out printed circuit board copper connections on multiple layers with through hole vias, including the checking of the layout against design rules and autorouting which automatically lays out printed circuit boards to meet the design rules. Our aim is to develop optical design rules and to incorporate them into the Cadence suite of programs so that optical waveguide interconnections can also be laid out in a similar manner and autorouted so PCB designers will not need much additional training. Stevenage Circuits is an established PCB manufacturer and is able to comment on the feasibility of incorporating different fabrication procedures into their production line facility. Two polymer manufacturers provide their latest photosensitive polymer formulations. Exxelis provides the Truemode® acrylate/methacrylate formulation and Dow Corning their Polysiloxane formulation polymers. High quality standard optical measurements and the development of new measurement techniques are provided by the National Physical Laboratory (NPL). These companies are complemented by three different university departments, the Department of Electronic and Electrical Engineering, University College London (UCL), Heriot Watt University, and Loughborough University. The research of the universities is detailed later in this paper.

The partners made a successful bid for matched funding from the Innovative Electronics Manufacturing Research Center (IeMRC) and the project was led by David Milward as Project Manager and the author as Lead Technical Manager. The project began with the aim of comparing several fabrication techniques for waveguides and was extended to include two different polymer formulations during the project. The research performed is multidisciplinary including the development of new chemical polymer formulations, the adaptation of layout software to include design rules, the development of existing fabrication techniques and the investigation of a completely new one, the development of novel mathematical techniques for waveguide modeling, the optimization of optical measurement techniques and development of a new one, the design of new demonstrator system backplanes. In this paper we give an overview of just some of the research performed by the researchers listed in the Acknowledgements section.

3. PHOTOLITHOGRAPHIC FABRICATION OF WAVEGUIDES

The companies Exxelis and Dow Corning fabricated a number of polymer waveguide structures such as bends, crossings, tapers, bent tapers by photolithography. In this process a generally 6 inch FR4 wafer is used as the substrate and a lower cladding is spun on to a thickness of about 50 µms. This also serves to planarize the often rippled surface of the FR4 due to the weave of the glass fibers inside it. After several stages of curing thermally and by UV illumination a second layer of core polymer having a slightly higher refractive index, is spun on. An electron beam or photomask pattern designed by UCL was used to expose the core. In the case of the Truemode® polymer, the mask must be held a short 100 µm distance above the wet polymer to avoid it coming into contact and a nitrogen blanket purge is used to remove oxygen from the polymer surface during the exposure. After removal of the unexposed polymer during a development step the core is fully cured. Finally, an upper cladding layer is spun over all of the waveguides to a depth of about 50 µms above the top of the waveguides which is then UV and thermally cured. The result is a number of square or rectangular cross section core waveguides buried within a surrounding cladding.

4. DIRECT LASER WRITE FABRICATION OF WAVEGUIDES

The lower cladding is deposited as for photolithographic waveguides or is spread over a larger area by pulling a doctor knife blade parallel to the substrate across the surface of the polymer and is then UV and thermally cured. The Truemode® core is then spread to a uniform depth and the substrate immersed in oil to exclude oxygen. Then the substrate is mounted in an oil bath to exclude oxygen on an XY motorized translation stage. A Helium-Cadmium 325 nm wavelength laser is used to illuminate a 50 or 60 µm square aperture, which is then in turn imaged onto the surface of the core polymer. The XY stage is moved under the laser to "draw" waveguide patterns. The UV laser cures the polymer as it moves. The use of the aperture reduces the effect of the Gaussian intensity profile of the laser beam if the beam is expanded to illuminate the aperture. If the aperture is not exactly focused onto the polymer surface Fresnel diffraction fringes can occur which give rippled along the length of the waveguide. When a waveguide bend is drawn, the sidewalls can slope, as the square aperture does not turn around the curve. The direct write technique does not require a mask to be fabricated first. The writing beams can be angled to that they meet the polymer at 45° which gives a 45° sloping waveguide facet surface which can be metallised with silver, for example, and used during operation with infra-red lasers to deflect normally incident beams into the waveguides. However, the writing speed needs to be sufficiently slow, 75 µm/s at 100 µW power, to enable the polymer to cure.

In this project, Heriot Watt University carried out and further developed both the fabrication technique and the polymer formulation itself. Techniques were developed to focus accurately the aperture on the surface to avoid diffraction fringes. The square pinhole was replaced by a circular one, which better waveguide sidewalls around bends. A new custom polymer formulation was developed to give good waveguide cross sections but at substantially faster writing speeds of about 50 mm/s at increased optical UV writing powers of 8 mW. In addition, the effect of writing over the same waveguide, 1, 2, and 4 times were investigated. Larger 600 mm by 300 mm travel motorized translation stages now allow larger optical OPCBs to be manufactured.

5. LASER ABLATION FABRICATION OF WAVEGUIDES

In the fabrication process of laser ablation, a laser is used to remove core and cladding polymer material on either side of a region, which forms the waveguide. The laser ablation process is the opposite of the laser direct write process as the ablation laser has to write outside the waveguide region. It could be used to remove all of the material between the waveguides but this is time consuming so it suffices simply to cut grooves through the core and often through some or all of the lower cladding as well, on each side of the position of the waveguide to break the lateral continuity of the core polymer.

Firstly, an FR4 substrate is prepared by spin coating two polymer layers, one of lower cladding polymer and one of core polymer, each cured by UV and several baking steps in turn. This is carried out at Loughborough University and at Dow Corning. The prepared substrate is then ready for laser ablation. There are two techniques which may be used: Thermal ablation, for example, using a 10 W maximum power, carbon dioxide, CO_2 gas, 10.6 µm wavelength, infra-red laser, which makes use of the full laser thermal power, and the second photo-chemical technique which uses either a Nd:YAG UV Laser or Excimer UV laser at low power levels. In the latter case, the photon energy is chosen to break bonds, with which it resonates, in the polymer. All three techniques are being investigated in this project using lasers at Loughborough University and a Nd:YAG in Stevenage Circuits Ltd PCB Manufacturer which they usually use to drill vias and holes in conventional PCB boards. The ablated holes and grooves are wider at the entry point of the laser and taper down in width. Finally, the upper cladding is deposited which fills the grooves caused by the ablation process and which buries the waveguide cores to a depth of about 50 µm and this is finally cured by UV and thermal baking steps.

After CO_2 thermal ablation the cross section of the groove formed had a wide curved approximately parabolic form with shallowly sloping walls. The intense heat at the center of the CO_2 laser beam caused severe damage to the polymer leaving a random honeycomb structure but it had the advantage of cutting through the polymer quickly. The Nd:YAG 355 nm wavelength, UV pulsed laser with 60 ns pulse duration cut narrow grooves on either side of the waveguide by

photochemical ablation and a waveguide of slightly trapezoidal cross section with sloping side walls was formed of size 71 µm x 79 µm. The Excimer UV laser was used to from a wide groove removing some of the core polymer material between the waveguides and not just a groove on each side. Two straight ridge waveguides with sloping walls of 70 µm width were formed having a center-to-center spacing of 330 µm but remaining coupled by some remaining core material between them.

To our knowledge, this is the first demonstration of the formation of polymer waveguides, by laser ablation, using a Nd:YAG laser at a commercial PCB manufacturer, without making major modifications to it, so that it could continue to be used on their conventional PCB manufacturing production line and represents a step forward in transferring the waveguide fabrication technology to commercial PCB manufacturers. Loughborough University plan to continue to investigate the laser ablation of flat 45° mirrors in-plane and curved mirrors.

6. INK JET PRINTING FABRICATION OF WAVEGUIDES

The PCB manufacturing industry is moving more towards the use of ink jet printing of features on the PCB. For example, a catalyst can be printed and then electroless plated to form copper track. Ink jet printing only deposits material where it is needed whereas the conventional process puts it down everywhere and then removes most of it, which is wasteful and costly. There have also been great advances in developing low cost, high precision, very large area ink jet printing machines for the printing and graphic arts industries. These considerations convinced the author that it may be a good time to revisit this technology for the printing of polymer cladding and waveguides. 100 µm wide waveguides and splitters have previously been fabricated [8], to our knowledge, using thermosetting polymer. The loss recorded at that time was rather high which may have been due to both the cross sectional shape and the choice of an optically lossy polymer. Therefore, in this project Loughborough University investigated whether new low loss UV curable polymers such as Truemode® acrylate/methacrylate formulation and Dow Corning Polysiloxane could be ink jet printed using the most recent ink jet printing heads from Xaar. These latest print heads save on use of polymer, as they only require pico-litre droplets only where they are needed.

One of the key issues to solve was that of making the polymer sufficiently low viscosity to allow it to be successfully jetted without blocking the ink jet head. At the same time if the polymer had too low a viscosity it would spread to a thin layer on the substrate. A number of methods to tackle this were investigated the first being the use of several solvents, to thin down the original polymer formulations. However, after jetting a droplet onto the substrate surface the solvent evaporated unevenly leaving a ridge of polymer material around the edge of the dried droplet with only a thin layer in the middle. It was found that cooling the substrate slowed down solvent evaporation and fix or pin the edge of the droplet so that it did not spread. The frequency of droplet emission and speed of droplet emission were also investigated. After the droplet had been deposited it was cured by UV exposure at varying times after emission from the ink jet head.

The droplet shape after deposition is determined by surface tension between it and the substrate and by its viscosity. The surface tension can be controlled by coating the substrate surface in hydrophilic or hydrophobic monolayers. Hydrophilic layers cause the droplets to spread which is good in that they join together to form a long stripe but bad because they spread sideways and give a very think structure. Hydrophobic layers cause a deposited stripe of polymer to become unstable and to draw itself back up into a row of individual discrete droplets. By controlling all of these variables, first a waveguide with an undulating sidewall and then a perfect waveguide were formed.

The next problem to tackle is the waveguide cross section, which is flat on the bottom but approximately circular above and at the sides giving a width of 80 µm a thickness of about 10 µm. Although there are several parameters, which can be varied, a balance needs to be attained also to control the wettability, line stability and adhesion. John Chappell [9] of Loughborough University was awarded a prize for his paper at ESTC, Greenwich, UK in 2008 for this thorough scientific investigation.

7. WAVEGUIDE COMPONENTS, MEASUREMENTS AND MODELLING

A number of waveguide component structures have and are being investigated in this project including, arrays of straight waveguides of various widths and spacings, waveguides crossing at a range of angles, 90° bends with a range of widths and radii of curvature 5.5 mm < R < 35 mm, ΔR = 1 mm, straight tapers with various taper input width to output width ratios, bent tapers which are a new element consisting of both a bend and a taper combined [10], spirals and other designs. The tapers are interesting elements as we have shown for the first time that the input light source can be misaligned laterally and that the taper still allows a reasonable coupling efficiency. This reduces the need for highly precise alignment in the connector so reducing its cost. However, UCL found that as the input facet of the taper is widened compared to the output of the taper, the loss of the taper increases. So there is a loss penalty for this improvement in input lateral coupling misalignment tolerance. Long adiabatic tapers gave the lowest loss. UCL found that in practical systems where one connector is placed very close to another the input waveguide has to bend almost immediately to avoid the next adjacent connector there is no room for a long low loss taper. So UCL introduced the new element which is a combination of a taper and a bend and proved that it combines the benefits of both [10].

The waveguide elements are modeled using ray tracing and beam propagation method, BPM. BPM is only designed for wave propagation, which deviates by small angles from the original direction of propagation so it would not normally be suitable for modeling 90° bends. However, we split the 90° bends into segments in which the waveguide only turns through small angles. Then each segment can be analyzed and the output field captured and transferred to the next section and run again. Finally, all of the segments can be joined together to give the result for a full 90° bend. Modeling offers additional advantages that the beam power can be monitored at many cross sections along the bend and so the loss can be separated into its contributions from transition or mode mismatch loss from a straight to a bend, radiation loss around the bend, propagation loss along a waveguide and input and output coupling loss [11].

The wide range of waveguide components are fabricated using a variety of fabrication techniques in two polymers, namely Truemode® acrylate/methacrylate formulation and Dow Corning's polysiloxane, on FR4 substrates. The individual waveguide components are diced and milled into convenient shapes and sizes for measurement. Dicing using a rotating saw blade leaves a slightly rough waveguide facet, which was measured by UCL using an atomic force microscope to have an RMS surface roughness of 26 nm to 192 nm. Subsequent polishing can be carried out but this adds an additional time consuming processing step which would raise the cost of the optical interconnect.

After fabrication the waveguide components are characterized optically to measure loss, crosstalk, and physically to measure misalignment tolerance, sidewall roughness and the system measurements of bit error rate and eye diagram. The results obtained from optical measurements are strongly dependent on the manner in which they are measured. In this paper the results were obtained by coupling an 850 nm 0 dBm VCSEL into a 50/125 µm step index multimode fiber. The fiber is wound around a drum former to mix the modes and it was checked that the output from the fiber fully filled its numerical aperture. The fiber output is butt coupled via index matching fluid to the waveguide entrance facet. The index matching fluid tends to suppress the scattering from the diced entrance face facet. At the waveguide output facet a pinhole is attached again with the same index matching fluid and beyond that an integrating sphere photodetector placed to measure the received power. This approximates the use of photodetector of aperture similar to that of the pinhole, 70 µm. The pinhole is also chosen to exclude much of the light traveling through the cladding.

8. WAVEGUIDE LAYOUT DESIGN RULES

When light is coupled into one waveguide in an array the light is scattered at the sidewall, which we measured for the first time to have an RMS roughness of 9 nm to 74 nm. Although this is a nano-roughness it still scatters the light out of

the waveguide into the cladding leading to propagation loss. If it scatters the light out it will also scatter the light into an adjacent waveguide by the same means causing cross talk. UCL measured the crosstalk for the first time [12] and found how far the adjacent waveguide should be to reduce crosstalk to a certain level so giving design rule. The sidewall roughness also couples the modes within the waveguide and UCL derived a new theory to model this [13].

The optimum width and thickness of a waveguide depends on the illumination source and the photodetector area. In our case, we chose a VCSEL with a 7 μm circular aperture and a photodiode with the largest aperture we could find 70 microns both operating at 10 Gb/s. The large photodetector aperture allows the waveguide to have a larger misalignment tolerance and the small VCSEL aperture compared to waveguide allows the VCSEL to have a larger misalignment tolerance. For our choice of source and detector we found the waveguide size with lowest loss and lowest crosstalk was 70 μm ×70 μm.

The first bit error rate measurements taken as a function of misalignment of a straight waveguide and for 90° waveguide bends from the source were taken at 2.5 Gb/s and showed the best bit error rate when exactly aligned with similar misalignment results for both straight and bent waveguides [14].

The input optical source and the output photodetector were each separately moved in XYZ directions to show how much misalignment could be tolerated. Misalignment away from contact with the waveguide facet did not cause serious loss of coupling until moved some distance from the facet. However, the misalignment along two axes normal to the propagation gave a more sensitive increase in loss and contour maps were plotted in X and Y.

The waveguide crossings showed that loss in passing through a crossing increased as the angle between the waveguides decreased. By choosing a minimum loss that can be tolerated a range of crossing angles permissible, more than 20º, can be established and entered as design rule into the Cadence Layout software.

For waveguide bends the smaller radius bends had higher combined bend loss whereas larger radius bends had more propagation loss. So there was found to be an optimum radius of about 15.3 mm for a waveguide width of 75 μm and this could again be entered as a design rule into the Cadence layout software.

9. SYSTEM DEMONSTRATOR WITH OPTICAL WAVEGUIDE BACKPLANE

A system demonstrator is being designed by Xyratex as part of their internal Candeo project and in a collaborative approach this IeMRC OPCB project was used to design the layout of the waveguides on the optical backplane. The daughter boards in the demonstrator are designed to take 4 input channels at 10 Gb/s each through 4 XFP ports and to pass them through an 8 × 8 multiway switch to the active connector which contains 4 VCSEL lasers preceded by their drive circuits. The connector also contains 4 photodiodes and receiver circuits which feed back signals via the 8 × 8 switch to the 4 10 Gb/s XFP ports. An FPGA on each daughter board is used to control the XFPs, the 8 × 8 switches, the laser drivers and photodiode receivers in the active connector. A graphical user interface has already been written for easy control of the FPGA. Each connector will carry an aggregate data rate of 80 Gb/s with 40 Gb/s in each direction. Each daughter board also carries an aggregate input and output data rate of 80 Gb/s.

This demonstrator was designed to meet the realistic needs of the end user. Therefore, it was specified that the waveguides could not enter certain parts of the PCB and should mainly lie within a limited area. In addition, all of the input and output waveguides must originate and terminate at the same side of a milled hole in the board which made way for a one sided connector. The connector had first been designed in an earlier project sponsored by EPSRC between

Xyratex Technology and UCL and is being commercialized in the Candeo project. The connector uses a low cost yet high precision alignment technique developed by UCL [12]. It was specified that the daughter cards must be capable of being interchanged without rotating them between insertions into the backplane. In addition, the spacing of the daughter cards was set to be rather close. Each connector site had to be connected to and from all of the other sites to allow total interconnectivity and 4 daughter cards were to be interconnected.

These tight constraints allowed a realistic test of the Cadence layout software together with the waveguide design rules established during this project. The waveguides had to bend almost immediately after their entrance facet to avoid the next connector and to meet the optimum bend radius requirement. We chose not to use tapers as our new alignment technique gave such high precision at low cost to make this unnecessary. Crossing waveguides allowed increased design flexibility and the angles were chosen to as large as possible from the design rules. To avoid crosstalk adjacent waveguides were designed to carry data in opposite directions. A new element was introduced for the first time, namely a straight waveguide crossing a bent waveguide. For all optical interconnections a power budget must be carried out for each point-to-point link. The laser had an output power of –2 dBm and the receiver sensitivity required an input power of –12 dBm for error free propagation at 10 Gb/s. If we allow a 2 dB power safety margin this gives a power budget of 8 dB similar to that required by the Ethernet standard specification. The bends had a higher loss than the crossings so it was best to reduce the number of bends however, a certain number had to be retained in order to meet the end user requirements.

The Cadence layout software output a suitable datafile for fabrication. The waveguides were made at IBM Zurich using their laser direct write process. The backplane has been mounted in the demonstrator unit and 4 daughter cards plugged in using the new connectors. Red lasers have been aligned to the waveguides and they can be seen traveling around the waveguides in the pattern designed as required. The waveguides are currently being measured to assess their loss and bit error rate and we hope to be able to report results soon. In the meantime, the datafile was supplied to Stevenage circuits who fabricated a dummy board proving that the design and data file is compatible with their commercial fabrication processes.

10. CONCLUSIONS

In this paper, the author outlines the collaboration of 8 companies and 3 universities in the IeMRC OPCB project. The various strands of research are described ranging from several fabrication techniques, new polymer formulations, novel ink jet fabrication developments, novel mathematical modeling techniques and finally a realistic full system demonstrator where progress is almost complete. The project has 7 more months to run before completion. In addition to the papers already cited, the partners, in this and in earlier projects, have fully disseminated the research as it was being performed via further published papers, conference talks, book chapters, visits to companies, universities, and to schools [15-31].

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