Computers Working at the Speed of Light

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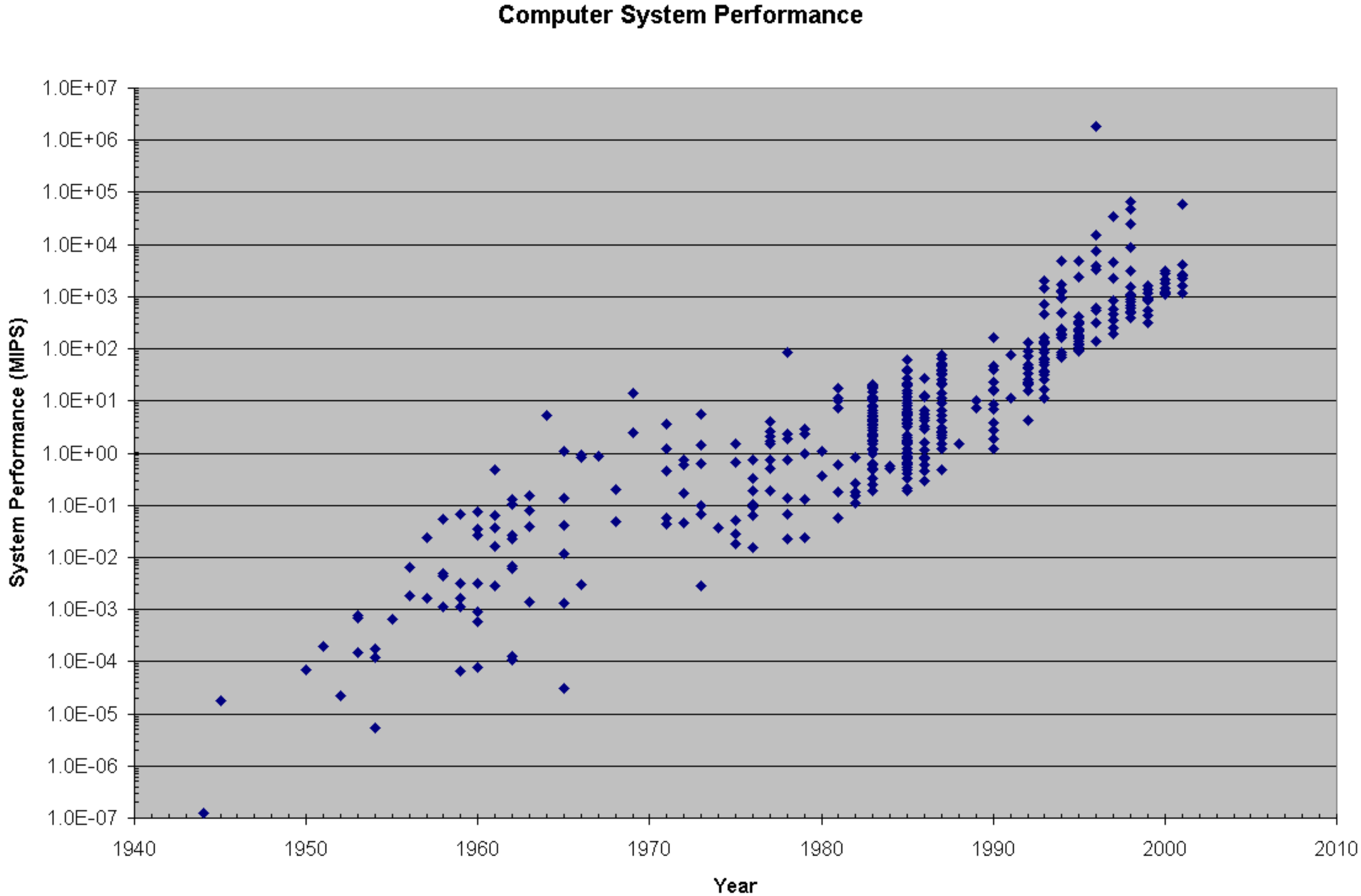
Moore's Law

- Gordon Moore was a co-founder of Intel.
- In 1965 he said that the number of transistors in an integrated circuit will increase exponentially, almost doubling every two years in an article in Electronics, Volume 38, Number 8, April 19, 1965
- Moore's law has been obeyed since the invention of the integrated circuit in 1958 to now
- The smaller the transistor the faster the switching speed can be giving faster computers.

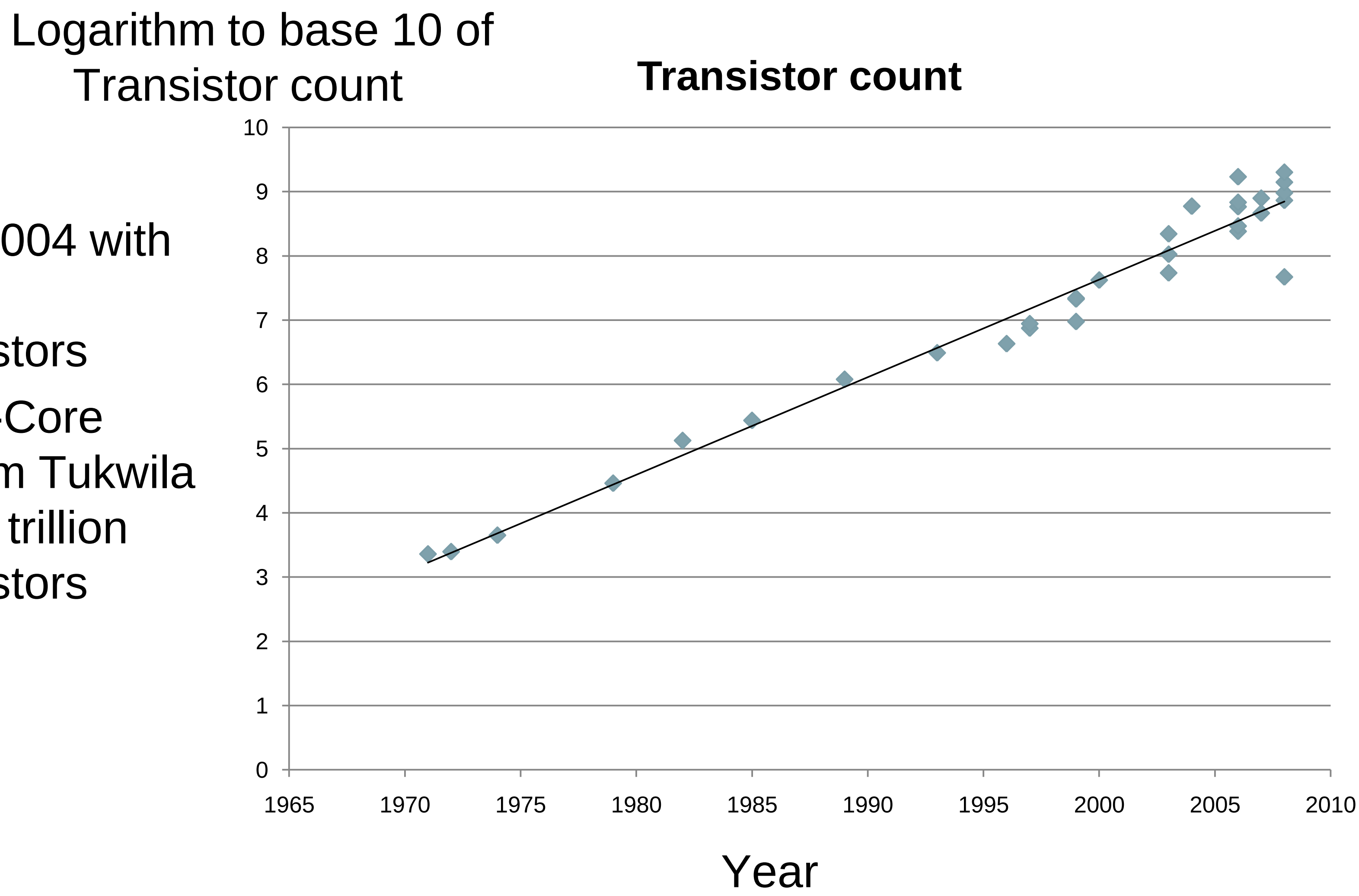
Computer CPU Performance Trend



Thanks to John McCallum http://www.jcmit.com/cpu-perf-chart.htm

Computer Processor Transistor Count Trend

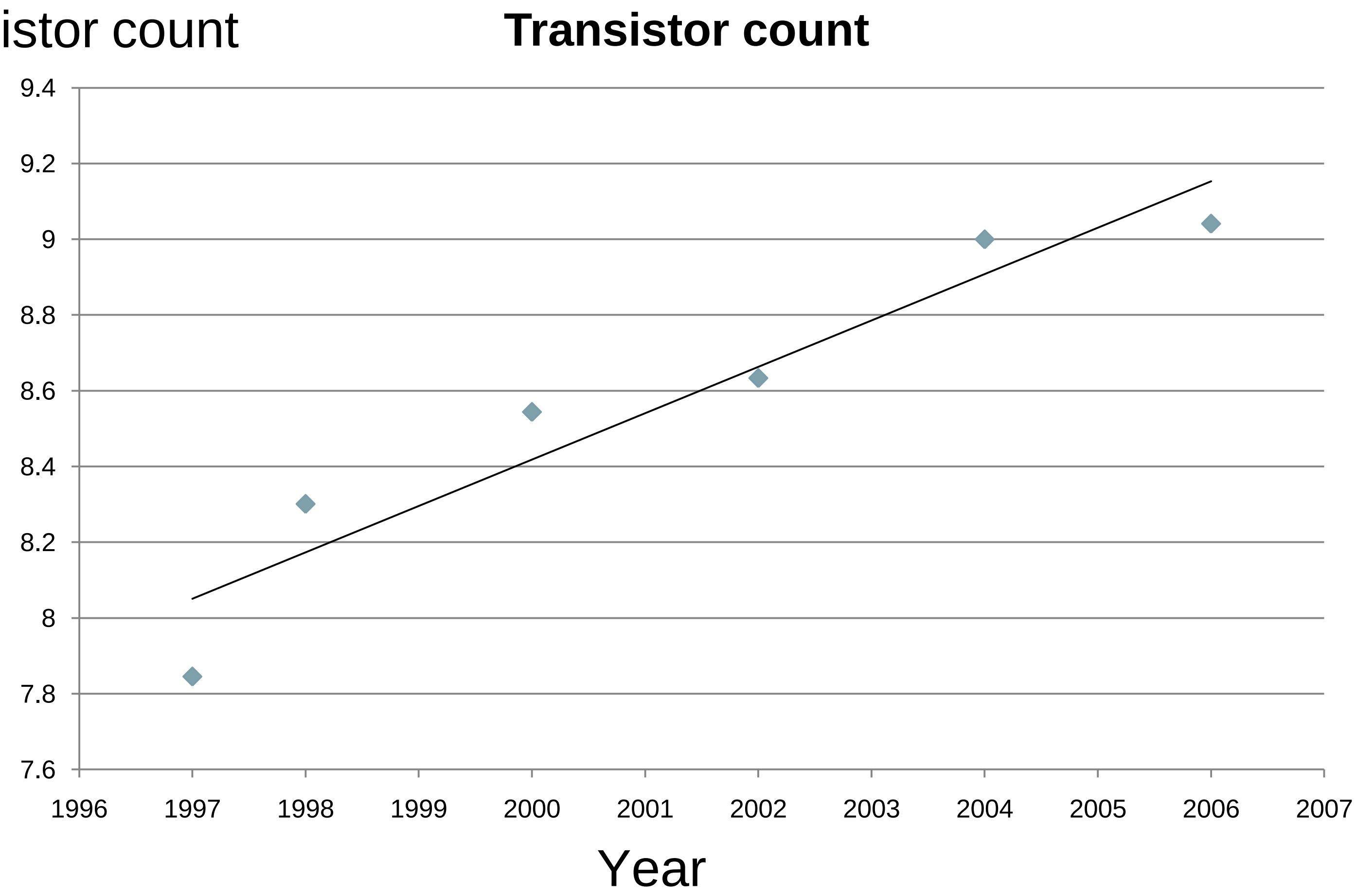
- Intel 4004 with 2300 transistors
- Quad-Core Itanium Tukwila with 2 trillion transistors



Field Programmable Gate Arrays, FPGA Transistor count for Xilinx Series

Logarithm to base 10 of Transistor count

- Virtex with 70 million transistors
- Virtex E
- Virtex II
- Virtex II Pro
- Virtex 4
- Virtex 5 with 1.1 trillion transistors



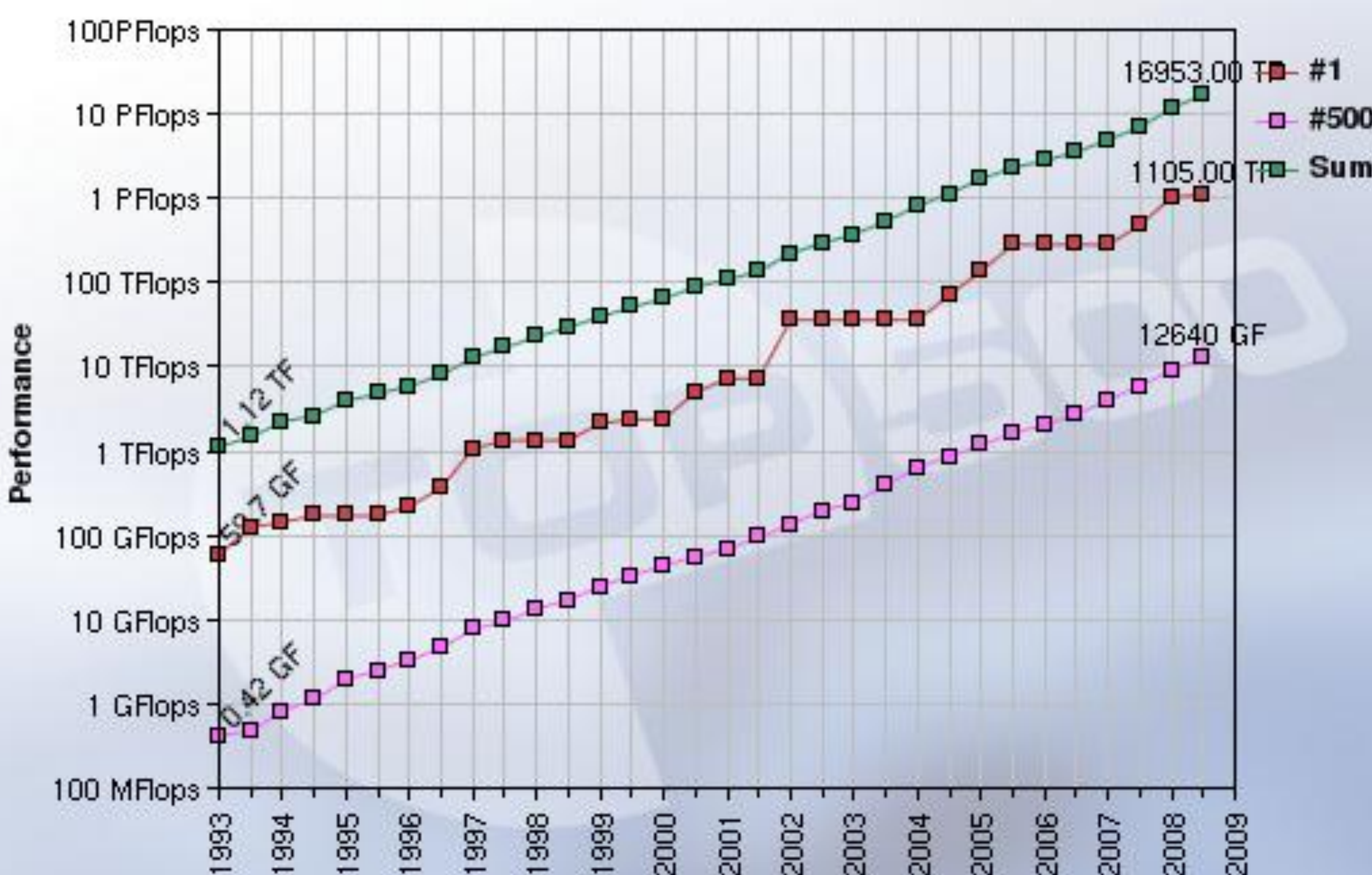
IBM's Blue Gene/L: world's fastest supercomputer in 2005

- The 65,536-processor machine can sustain 280.6 trillion calculations per second, called 280.6 teraflops

IBM's Blue Gene/L supercomputer simulated half a mouse brain 2007

- University of Nevada with IBM Almaden Research Lab, ran a "cortical simulator that was as big and as complex as half of a mouse's brain on the BlueGene L,"
- It had 8,000 neurons and 6,3000 synapses
- It ran for 10 seconds at a speed "ten times slower than real-time"

Performance Development



14/11/2008 http://www.top500.org/

Top 10 Fastest Computers in December 2008

1	Roadrunner - BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz , Voltaire Infiniband
2	Jaguar - Cray XT5 QC 2.3 GHz
3	Pleiades - SGI Altix ICE 8200EX, Xeon QC 3.0/2.8 GHz
4	BlueGene/L - eServer Blue Gene Solution
5	Blue Gene/P Solution
6	Ranger - SunBlade x6420, Opteron QC 2.3 GHz, Infiniband
7	Franklin - Cray XT4 QuadCore 2.3 GHz
8	Jaguar - Cray XT4 QuadCore 2.1 GHz
9	Red Storm - Sandia/ Cray Red Storm, XT3/4, 2.4/2.2 GHz dual/quad core
10	Dawning 5000A - Dawning 5000A, QC Opteron 1.9 GHz, Infiniband, Windows HPC 2008

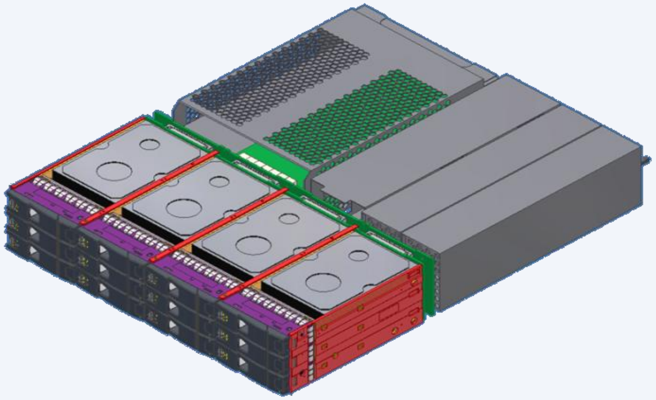
IBM Roadrunner Supercomputer at Los Alamos National Laboratory in June 2008 is worlds fastest

- 1.105 petaflop/s
- Second fastest is the Cray XT5 supercomputer at Oak Ridge National Laboratory called Jaguar.
- The system, is the second to break the petaflop/s barrier
- One petaflop/s represents one quadrillion floating point operations per second.

Data storage systems increasing in complexity, density and speed

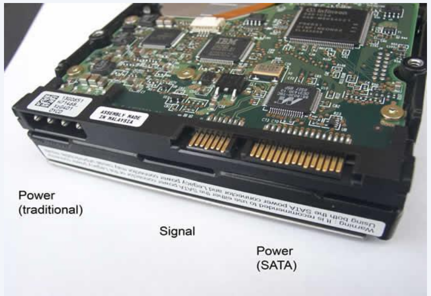
Storage demand increasing

- Manage more storage
- Increased complexity



Data rates increasing

- Data access speeds:
- *3 Gb/s SAS → 6 Gb/s SAS*
- *10 Gb/s Gigabit Ethernet*
- *12 Gb/s SAS*

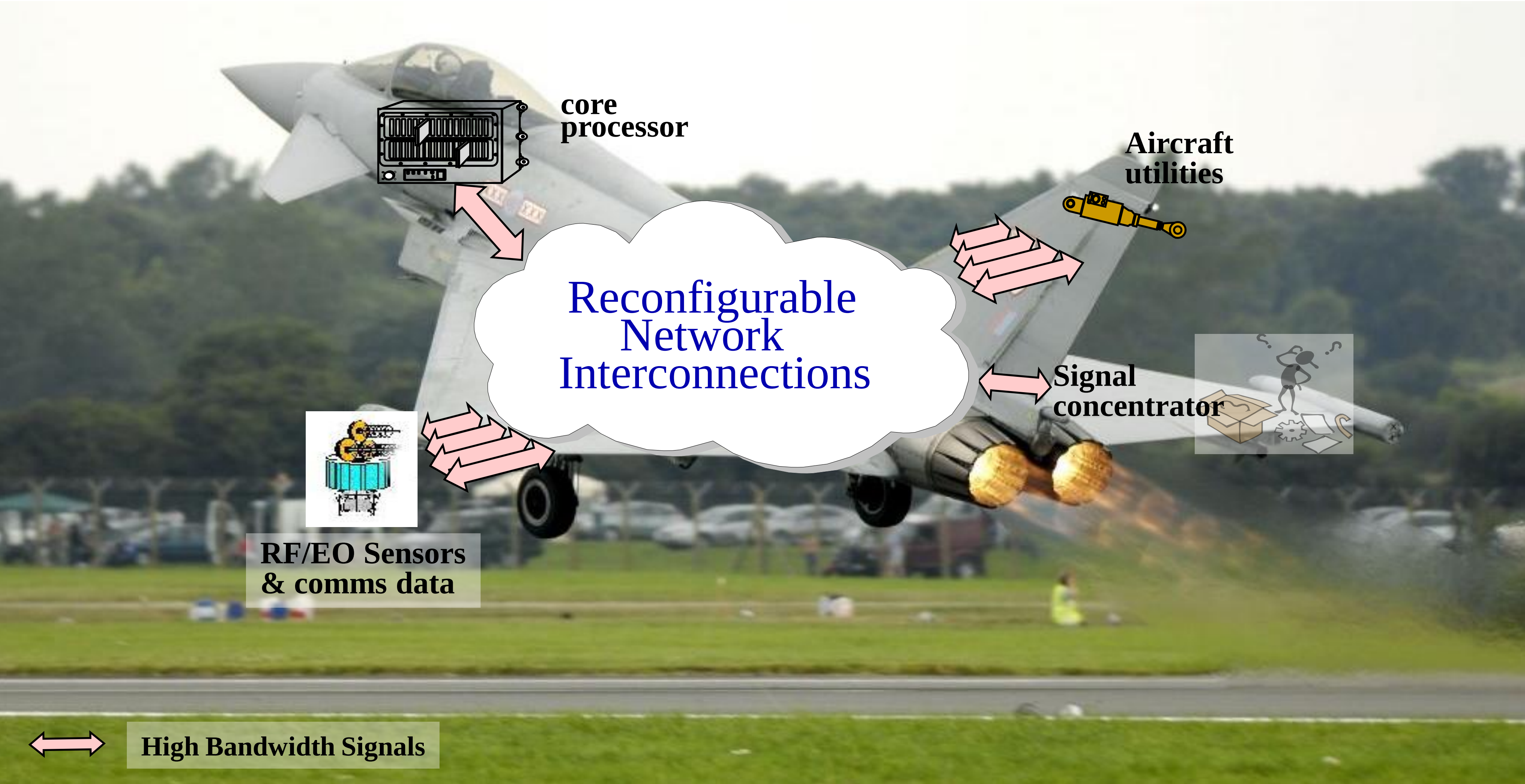


Disk sizes decreasing

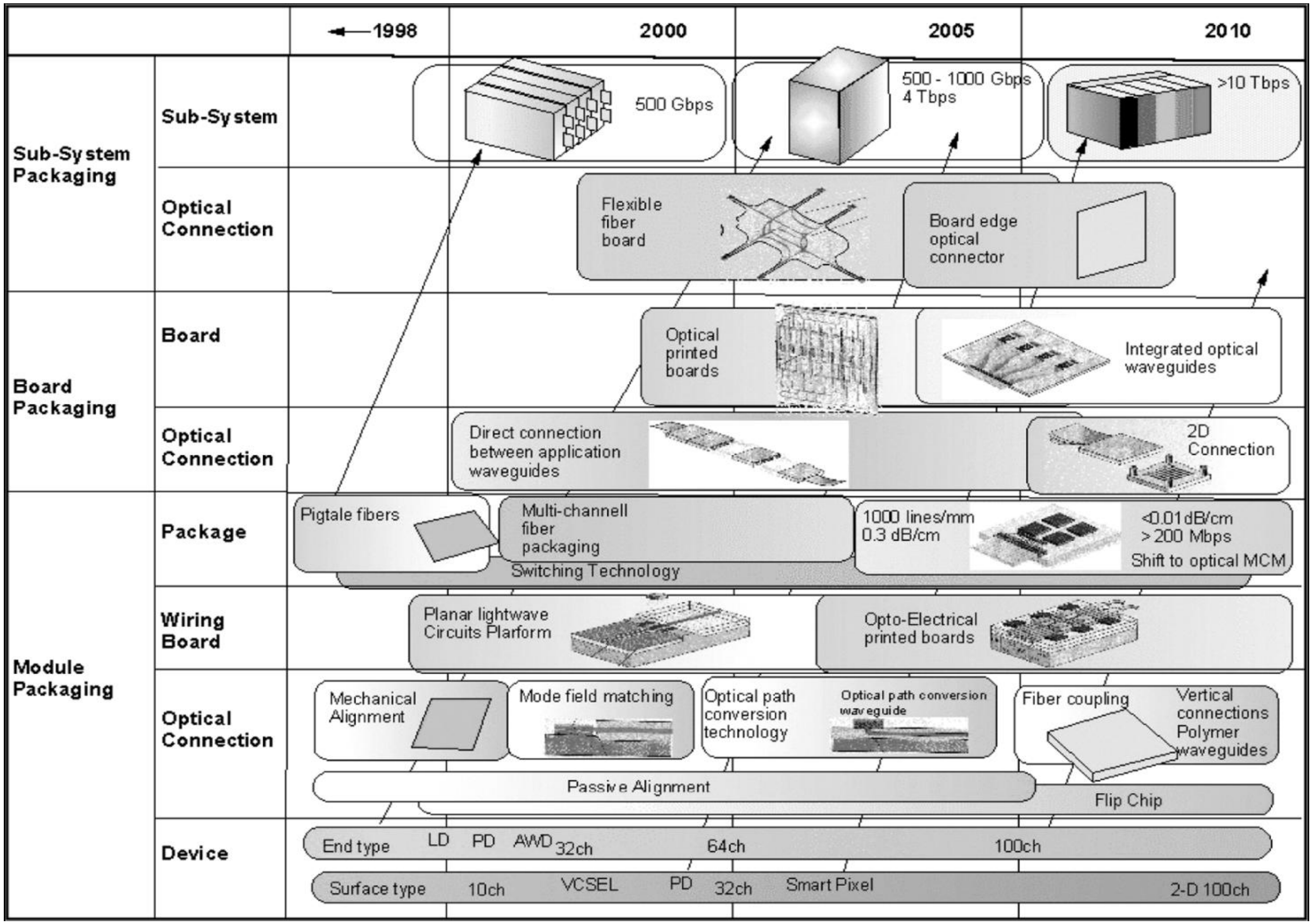
- 3.5” → 2.5” → 1.8” → 1”
- Increased system density

On-board Platform Applications

On-board Platform Applications

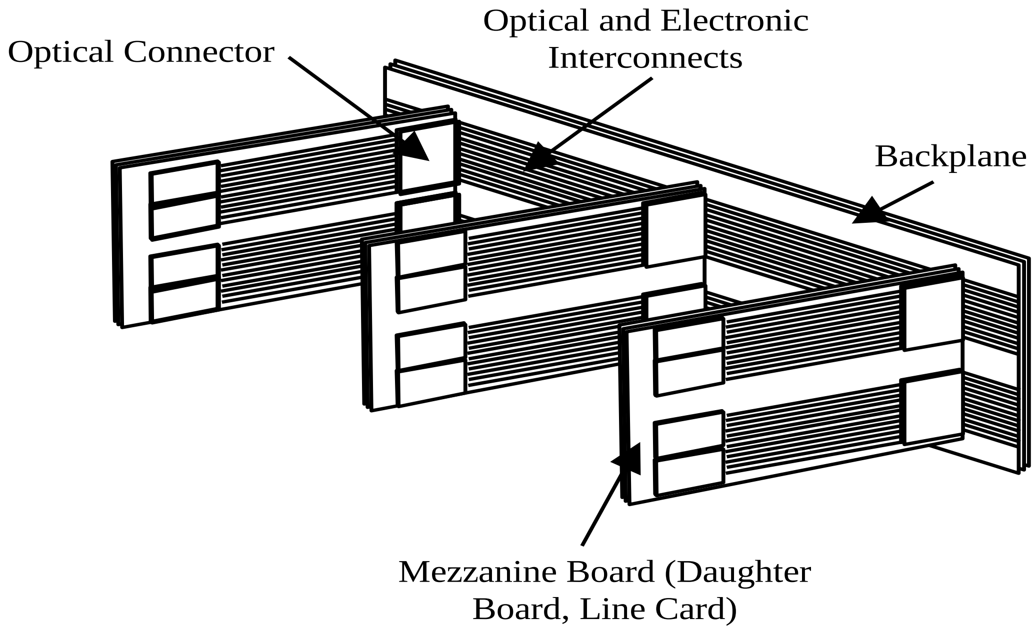


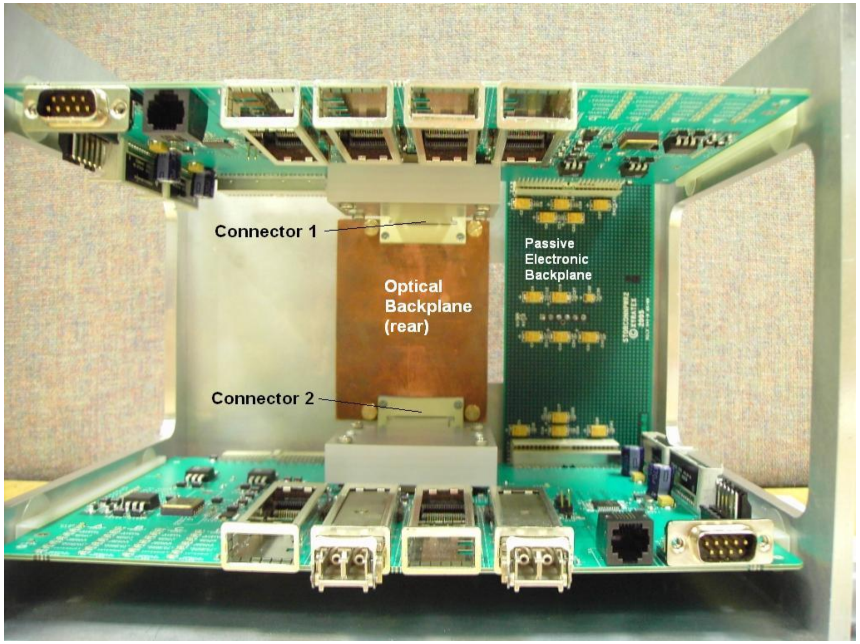
JIEP Optical Packaging Roadmap 2002



Happy T. Holden
The developing technologies of integrated optical waveguides in printed circuits
Circuit World
29/4 [2003] 42–50

Backplane Motherboards



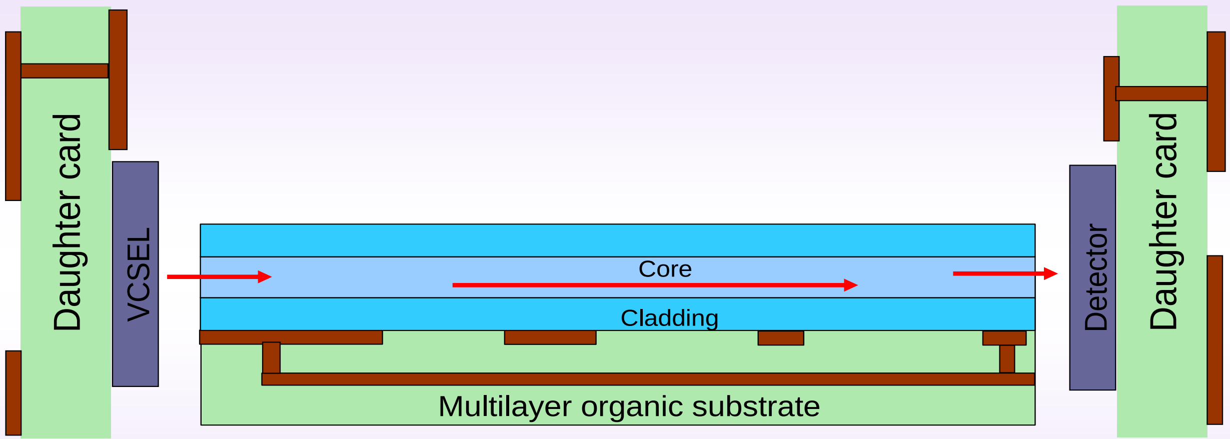


Copper Tracks versus Optical Waveguides for High Bit Rate Interconnects

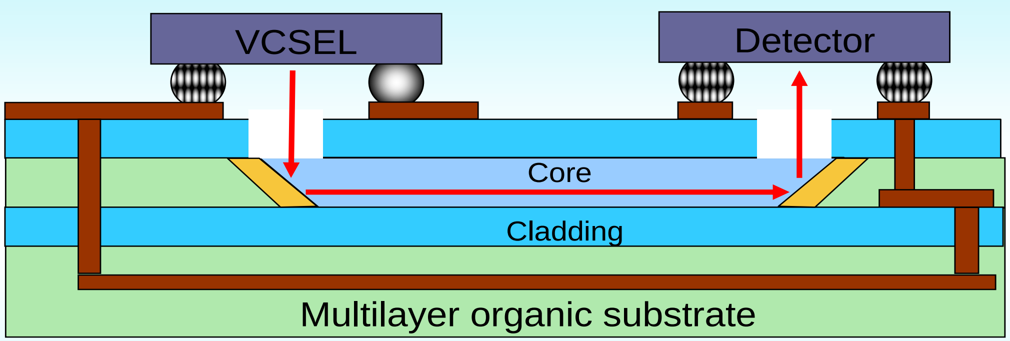
- Copper Track
  - EMI Crosstalk
  - Loss
  - Impedance control to minimize back reflections, additional equalisation, costly board material

- Optical Waveguides
  - Low loss
  - Low cost
  - Low power consumption
  - Low crosstalk
  - Low clock skew
  - WDM gives higher aggregate bit rate
  - Cannot transmit electrical power

Integration of Optics and Electronics

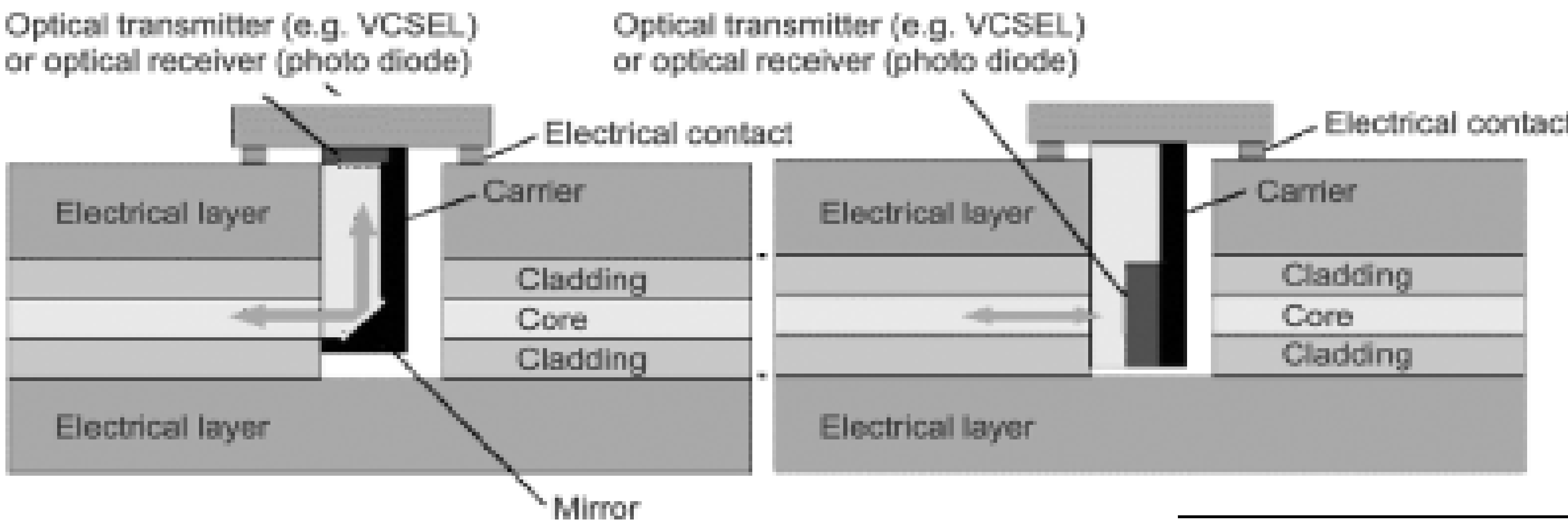


- Backplanes
  - Butt connection of "plug-in" daughter cards
  - In-plane interconnection
- Focus of OPCB project



- Out-of-plane connection
  - 45 mirrors
  - Chip to chip connection possible

Optical Connectors (Griese, 2002)



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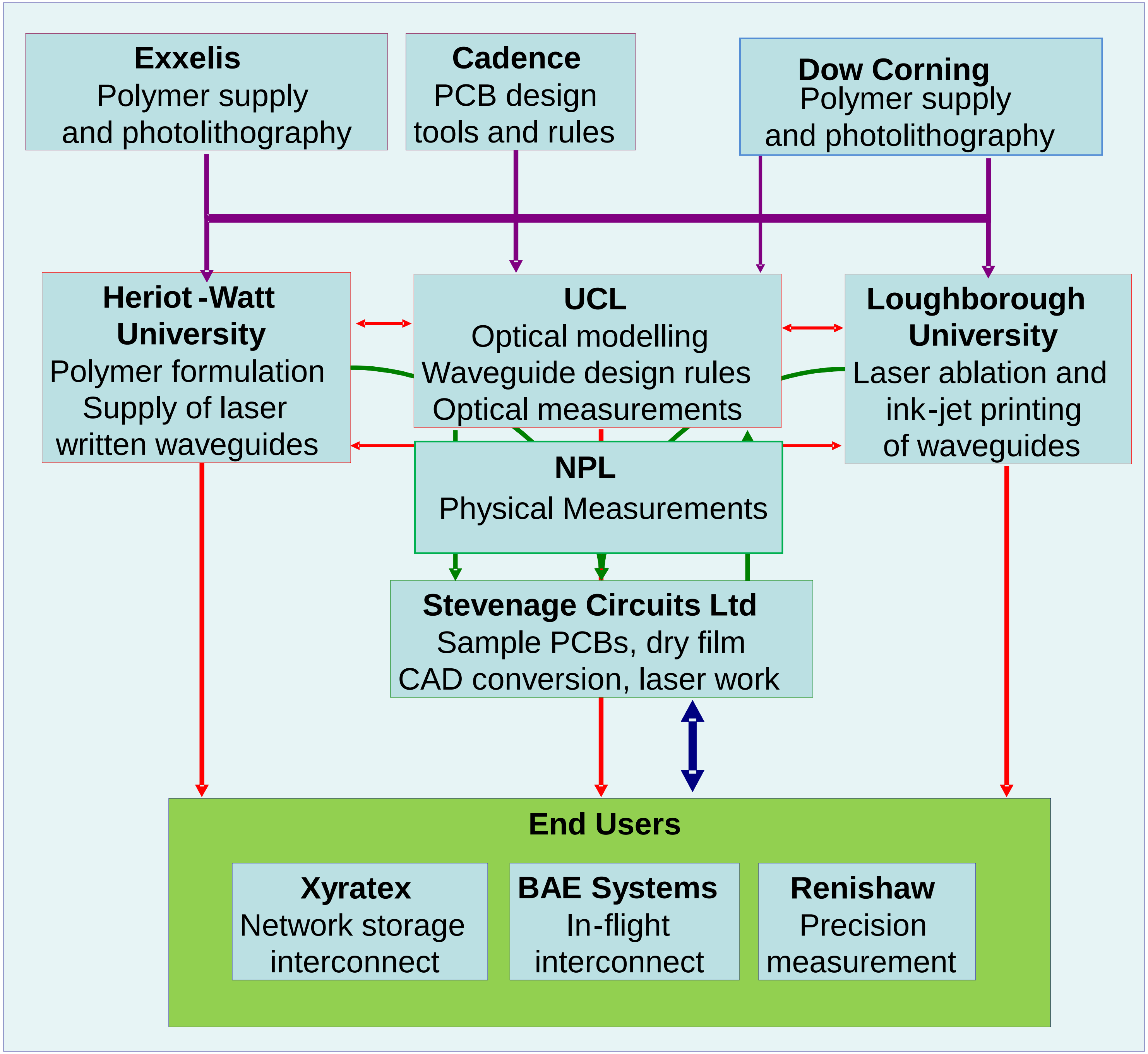
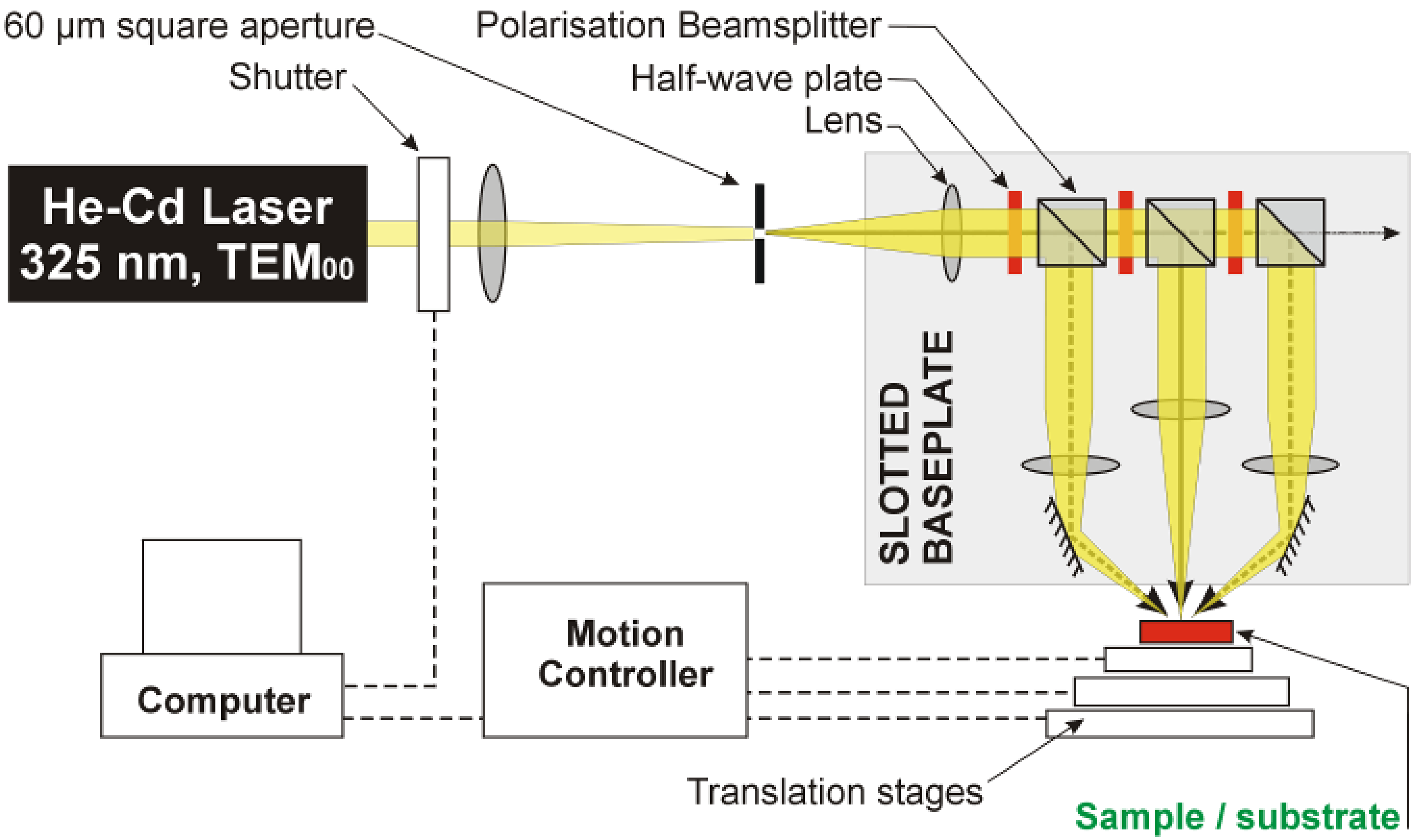
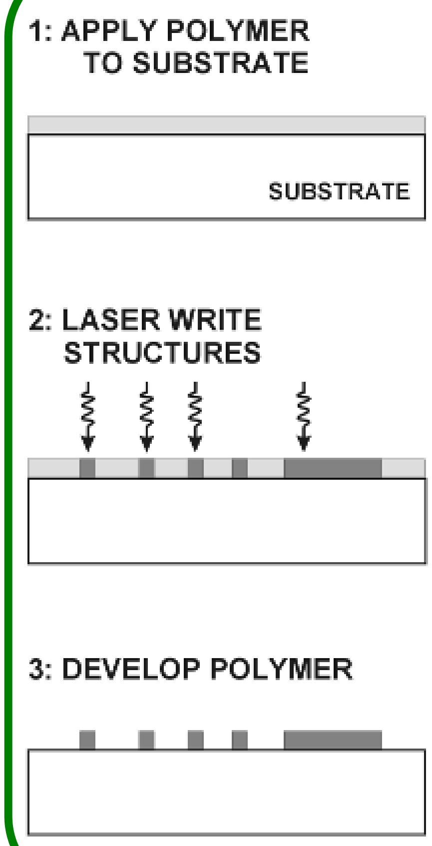
The Integrated Optical and Electronic Interconnect PCB Manufacturing (OPCB) project

- Hybrid Optical and Electronic PCB Manufacturing Techniques
- 8 Industrial and 3 University Partners led by industry end user
- Multimode waveguides at 10 Gb/s on a 19 inch PCB
- Project funded by UK Engineering and Physical Sciences Research Council (EPSRC) via the Innovative Electronics Manufacturing Research Centre (IeMRC) as a Flagship Project
- 2 years into the 3 year, £1.3 million project


Exxelis
Polymer supply
and photolithography
Cadence
PCB design
tools and rules
Dow Corning
Polymer supply
and photolithography
Heriot -Watt
University
Polymer formulation
Supply of laser
written waveguides
UCL
Optical modelling
Waveguide design rules
Optical measurements
Loughborough
University
Laser ablation and
ink-jet printing
of waveguides
NPL
Physical Measurements
Stevenage Circuits Ltd
Sample PCBs, dry film
CAD conversion, laser work
End Users
Xyratex
Network storage
interconnect
BAE Systems
In-flight
interconnect
Renishaw
Precision
measurement

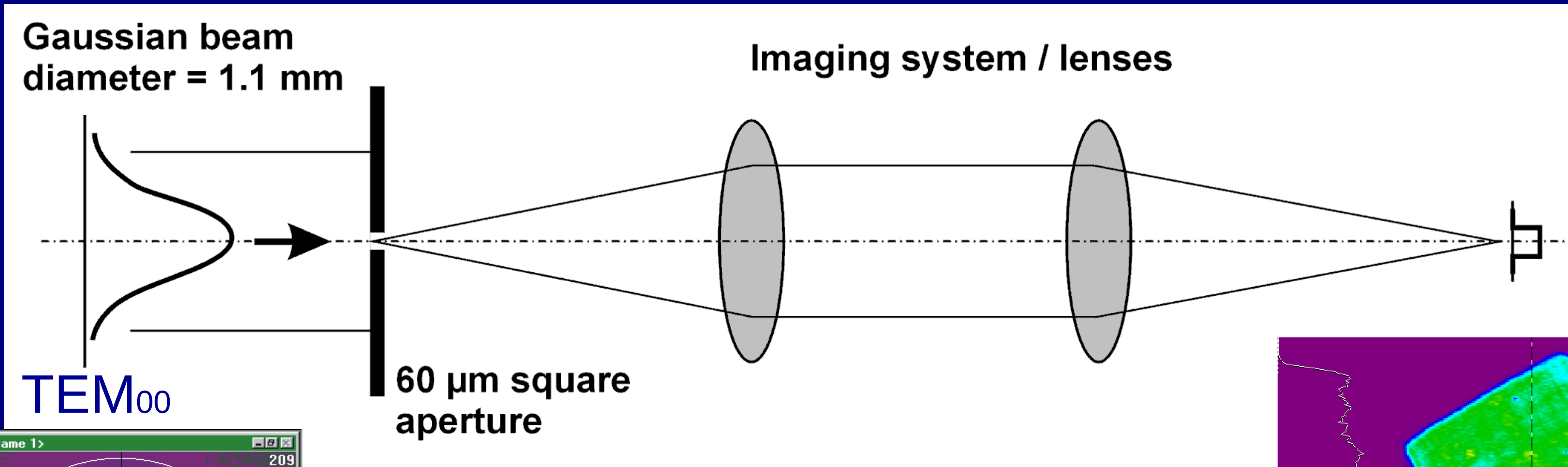
Direct Laser-writing Setup: Schematic

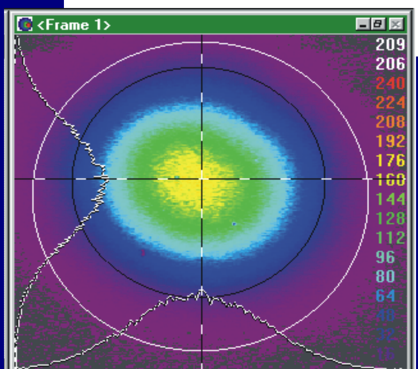


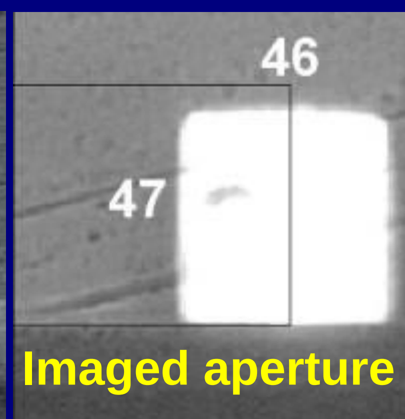


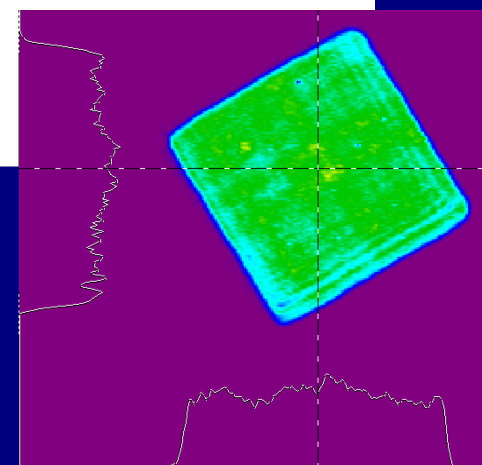
- **Slotted baseplate** mounted vertically over translation, rotation & vertical stages; components held in place with magnets
- By using two opposing 45º beams we minimise the amount of substrate rotation needed

Writing sharply defined features
– flat-top, rectangular laser spot







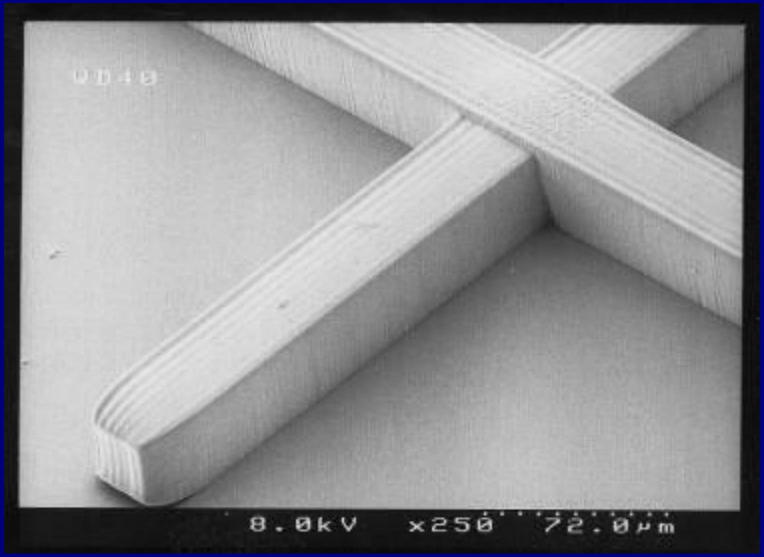


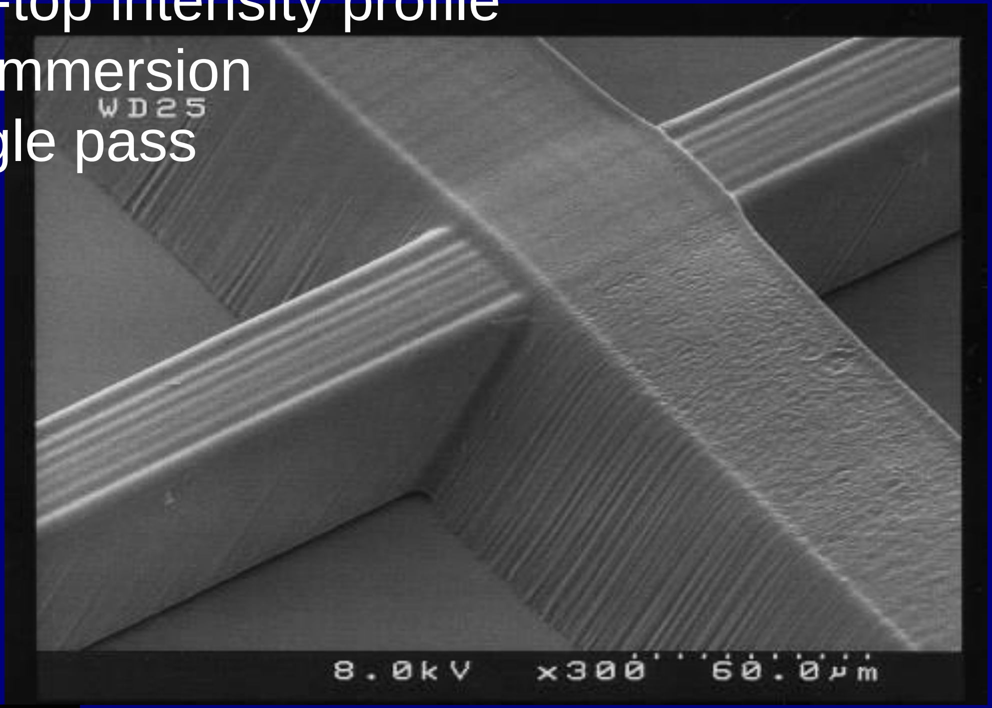
Images of the resulting waveguide core cross-sections

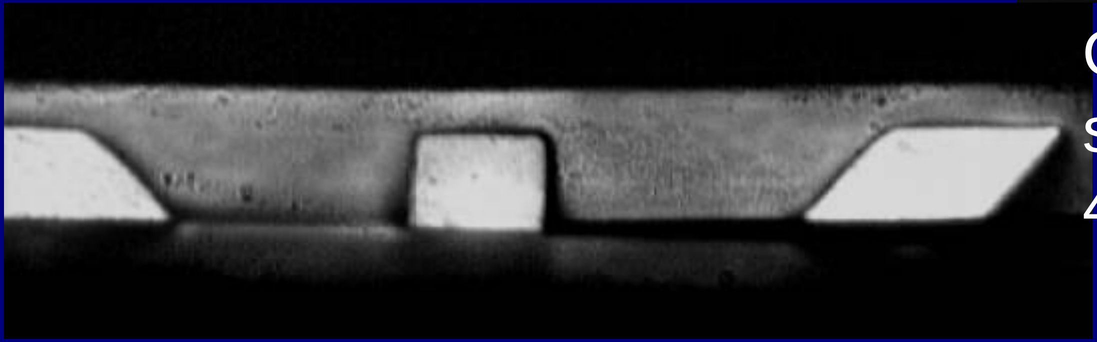
Laser written polymer structures

SEM images of polymer structures written using imaged 50 µm square aperture (chrome on glass)

- Writing speed: ~75 µm / s
- Optical power: ~100 µW
- Flat-top intensity profile
- Oil immersion
- Single pass





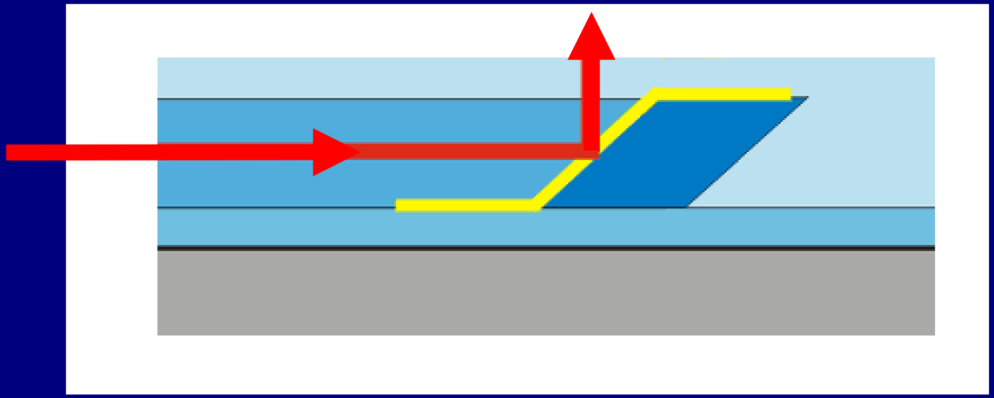


Optical microscope image showing end on view of the 45º surfaces

Waveguide terminated with 45-deg mirror

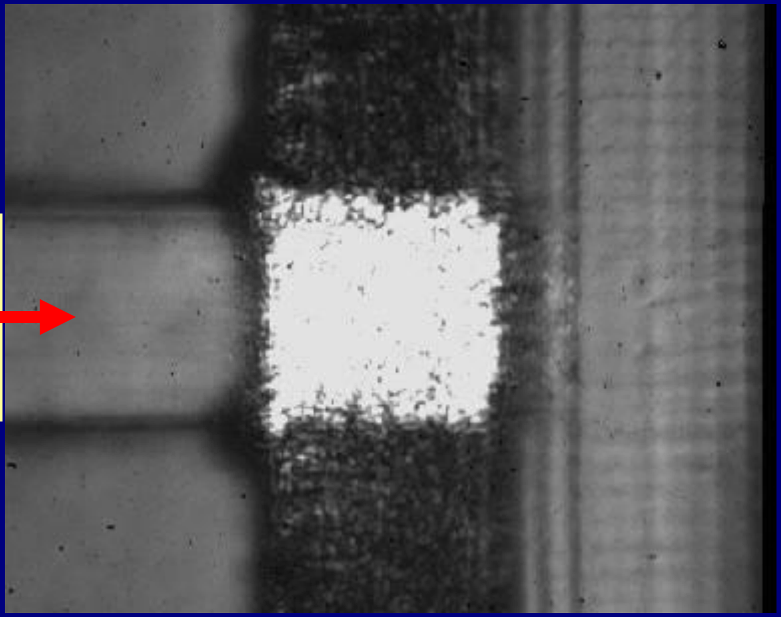
Out-of-plane coupling,

using 45-deg mirror (silver)



Microscope image looking
down on mirror
coupling light towards camera

OPTICAL INPUT



Current Results

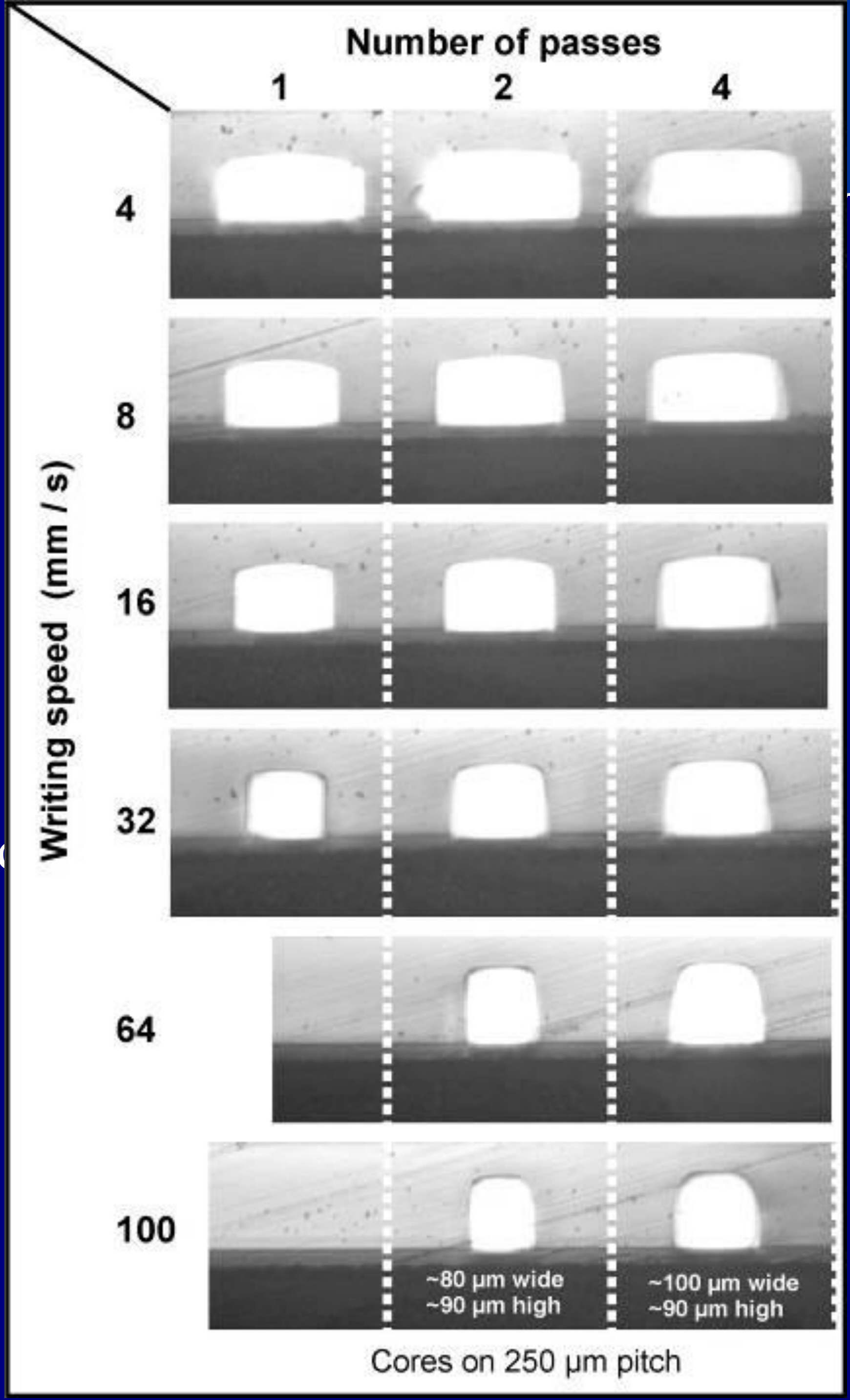
Laser-writing Parameters:

- Intensity profile: Gaussian
- Optical power: ~8 mW
- Cores written in oil

Polymer:

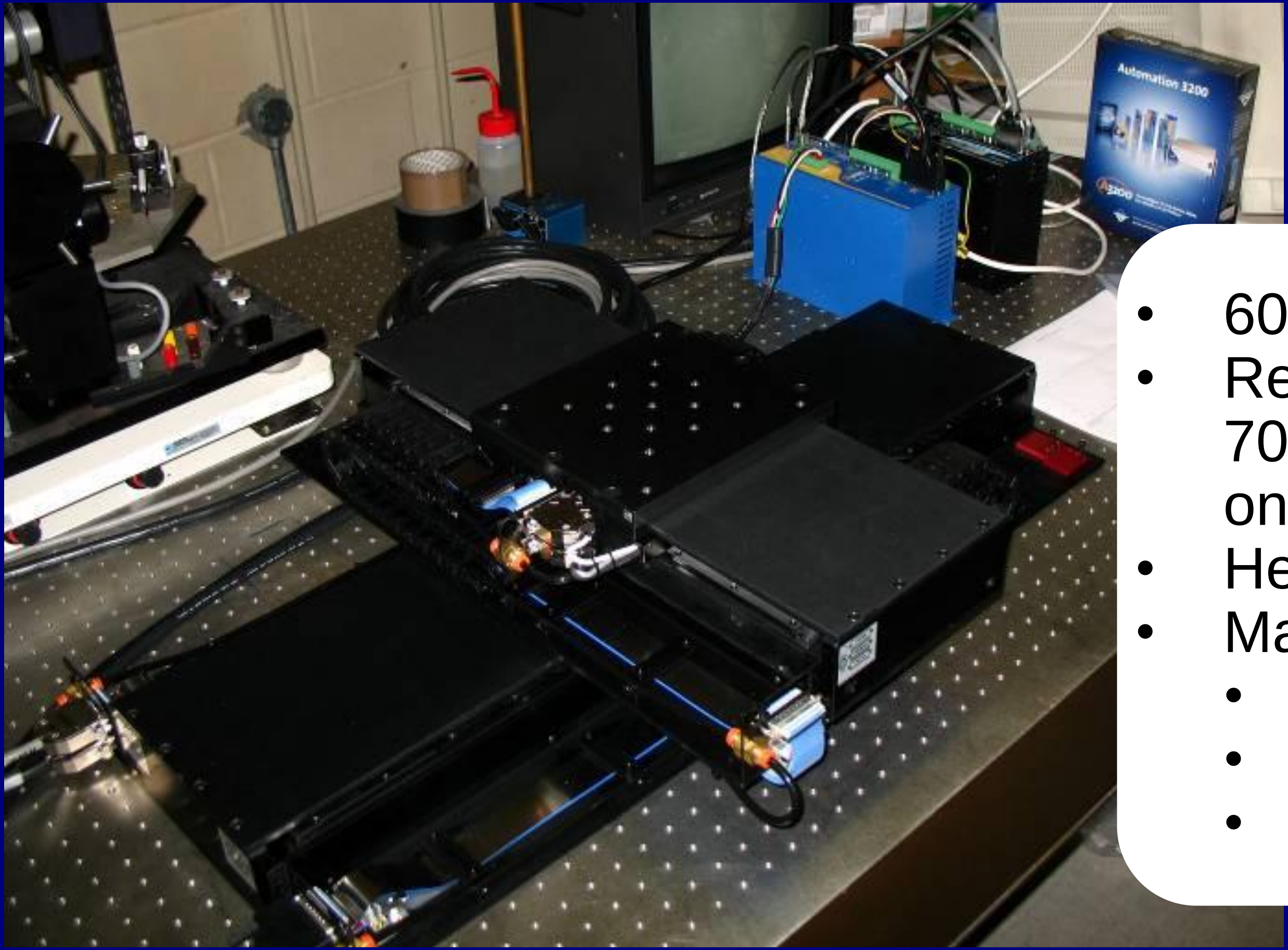
- Custom multifunctional acrylate photo-polymer
- Fastest "effective" writing spee
  to date: 50 mm/s

(Substrate: FR4 with polymer undercladding)



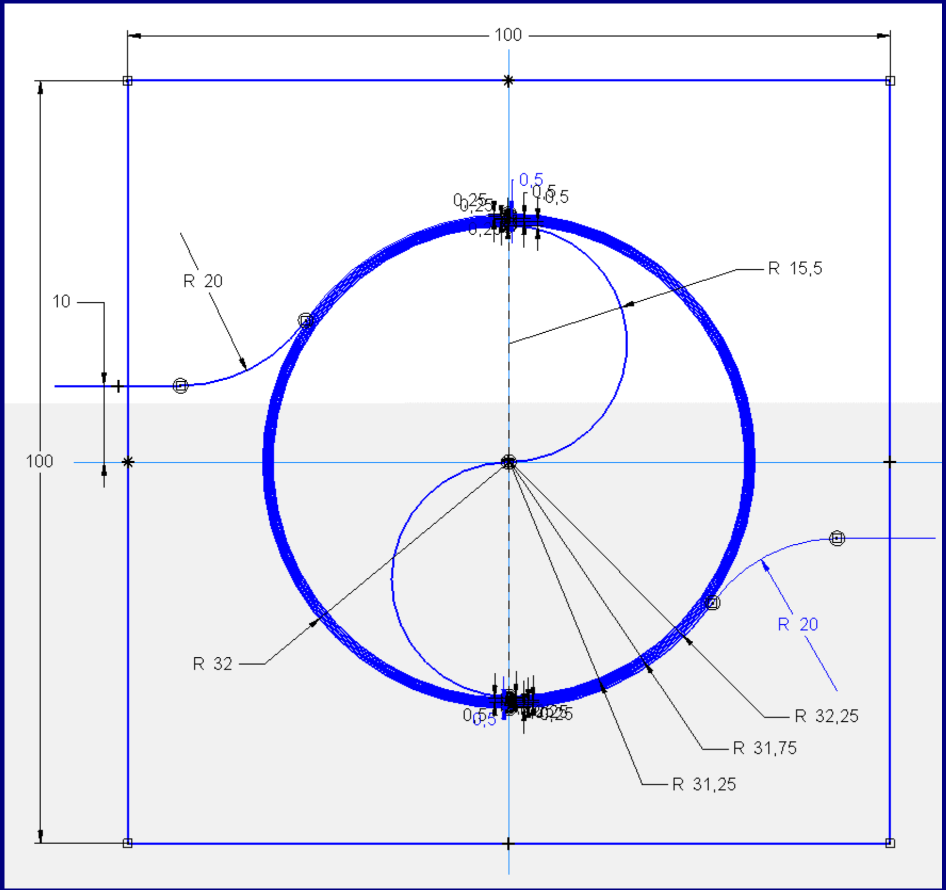
Large Board Processing: Writing

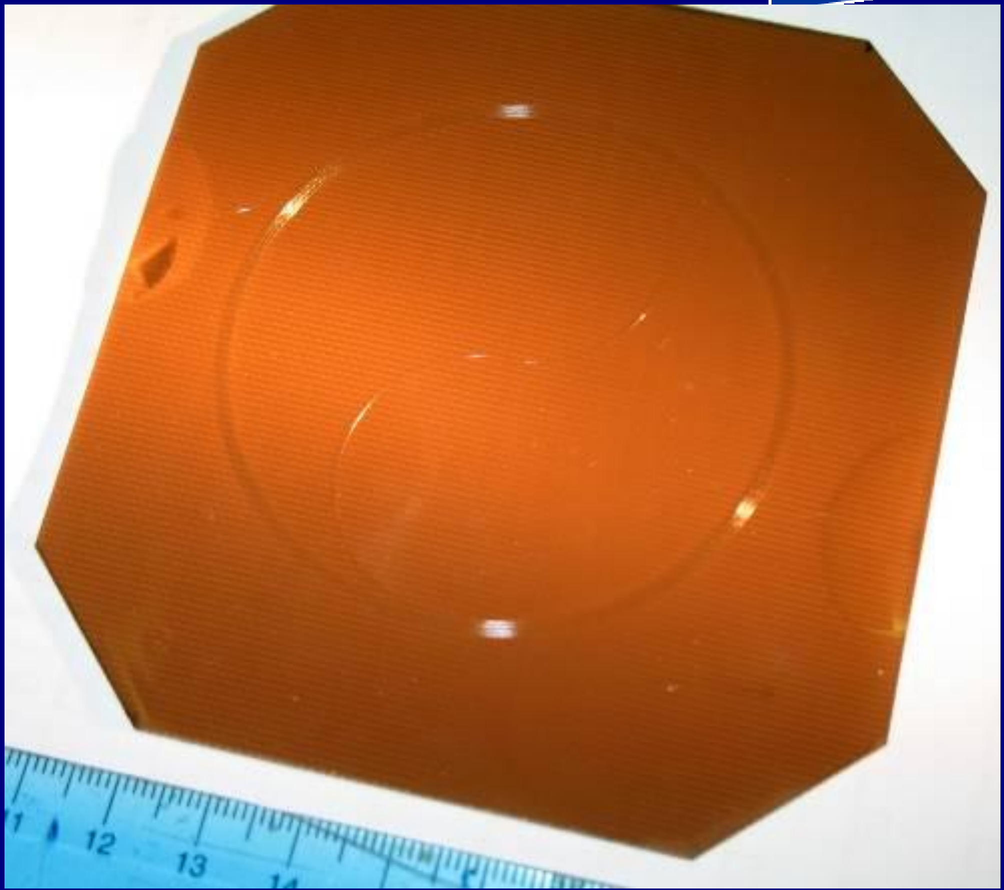
- Stationary “writing head” with board moved using Aerotech sub-µm precision stages
- Waveguide trajectories produced using CAD program



- 600 x 300 mm travel
- Requires a minimum of 700 x 1000 mm space on optical bench
- Height: ~250 mm
- Mass:
  - 300 mm: 21 kg
  - 600 mm: 33 kg
  - Vacuum tabletop

Large Board Processing: Writing

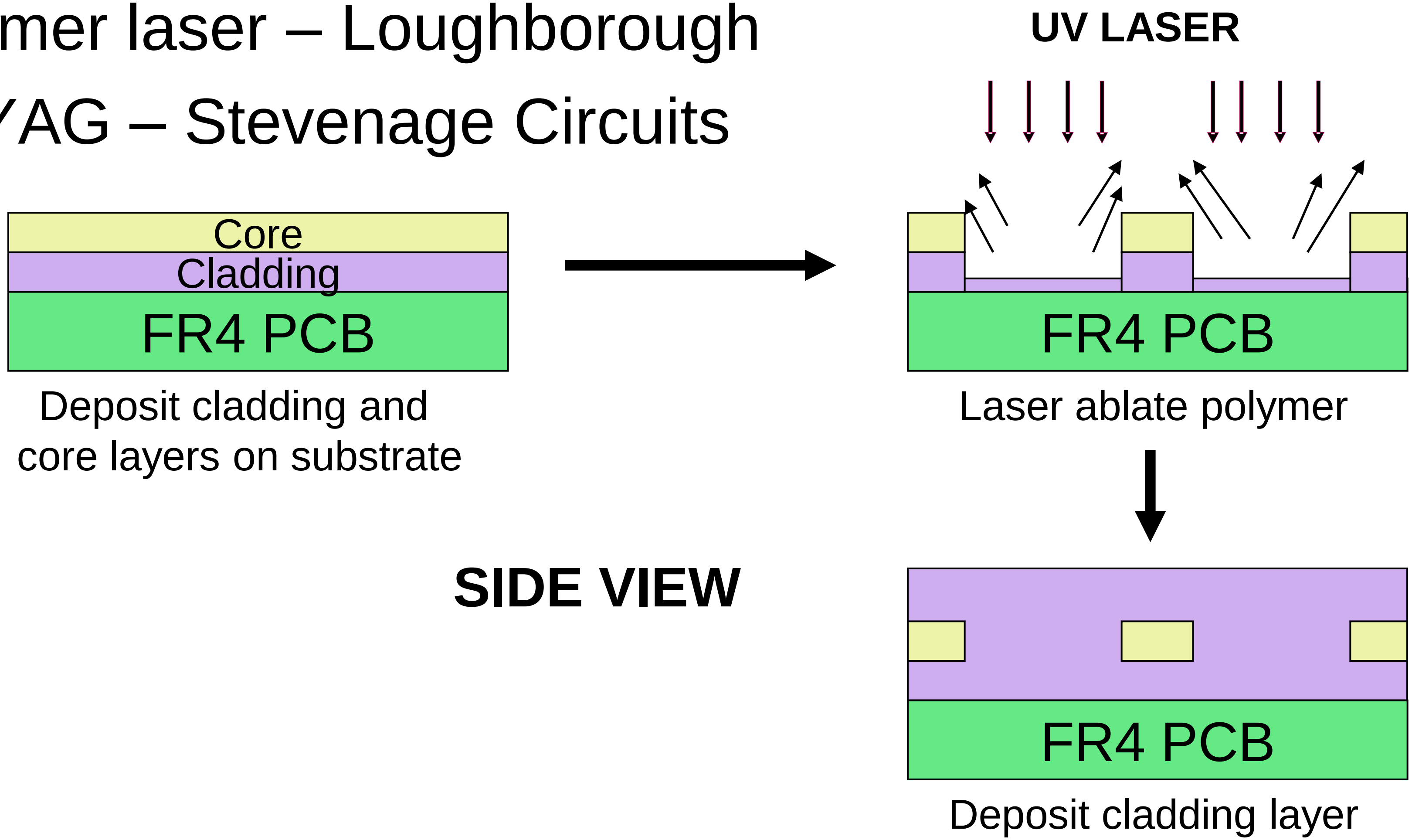




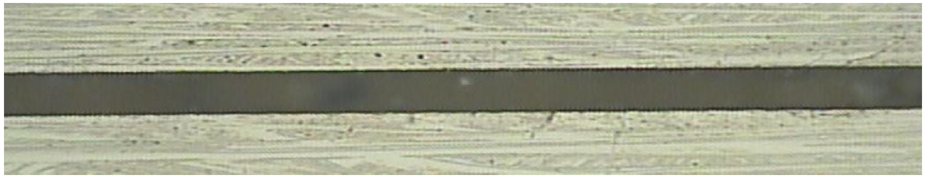
The spiral was fabricated using a Gaussian intensity profile at a writing speed of 2.5 mm/s on a 10 x 10 cm lower clad FR4 substrate. Total length of spiral waveguide is **~1.4 m**. The spiral was upper cladded at both ends for cutting.

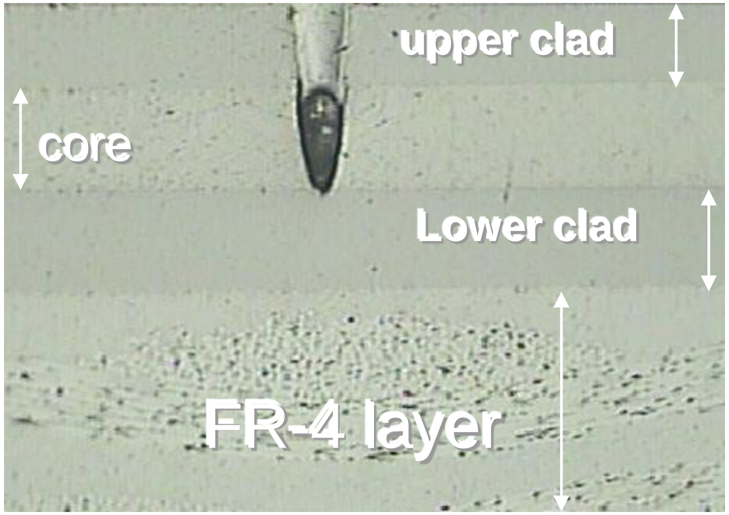
Laser Ablation for Waveguide Fabrication

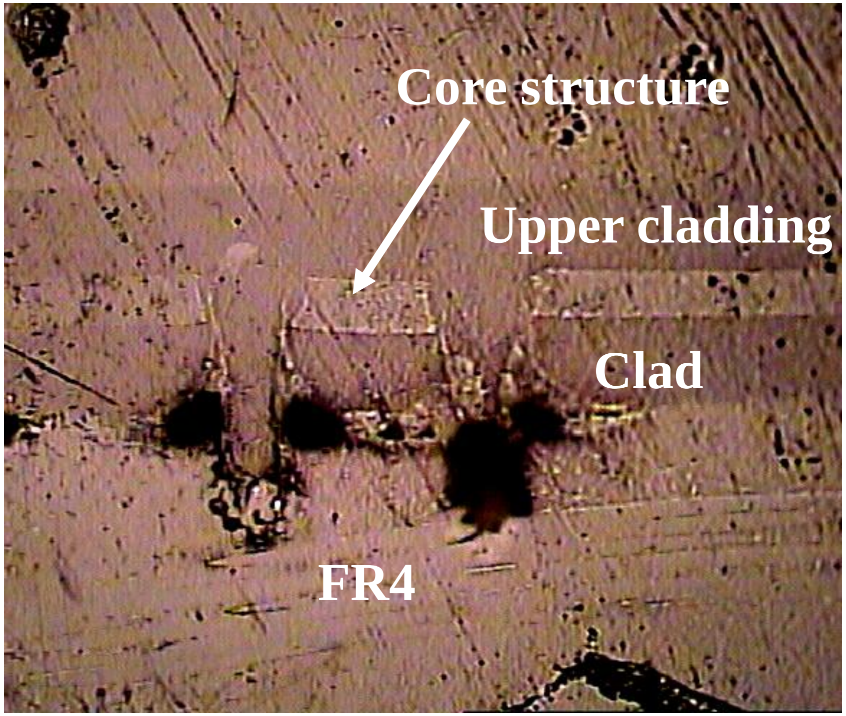
- Ablation to leave waveguides
- Excimer laser – Loughborough
- Nd:YAG – Stevenage Circuits



Nd:YAG Ablation

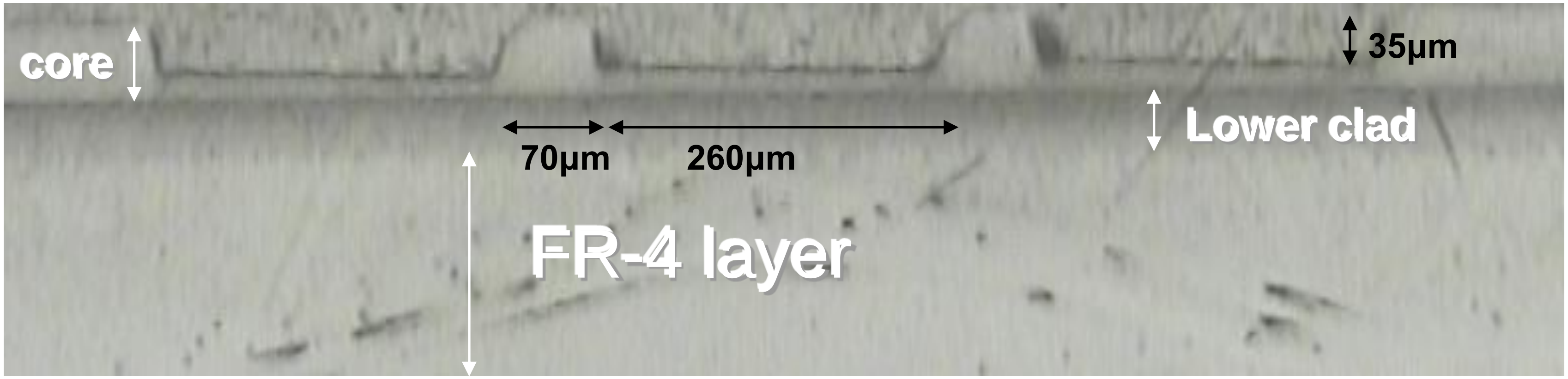




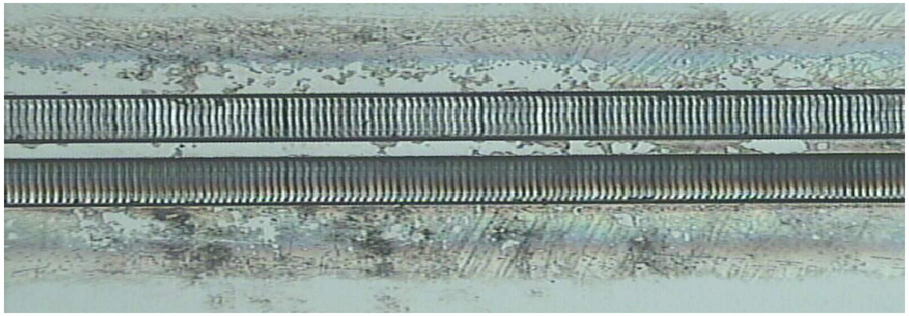


- Nd:YAG laser based at Stevenage Circuits
- Grooves machined in optical polymer and ablation depth characterised for machining parameters
- Initial waveguide structures prepared

Excimer Laser Ablation



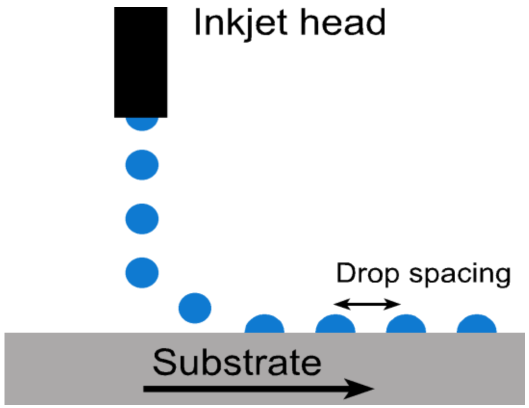
Cross-section



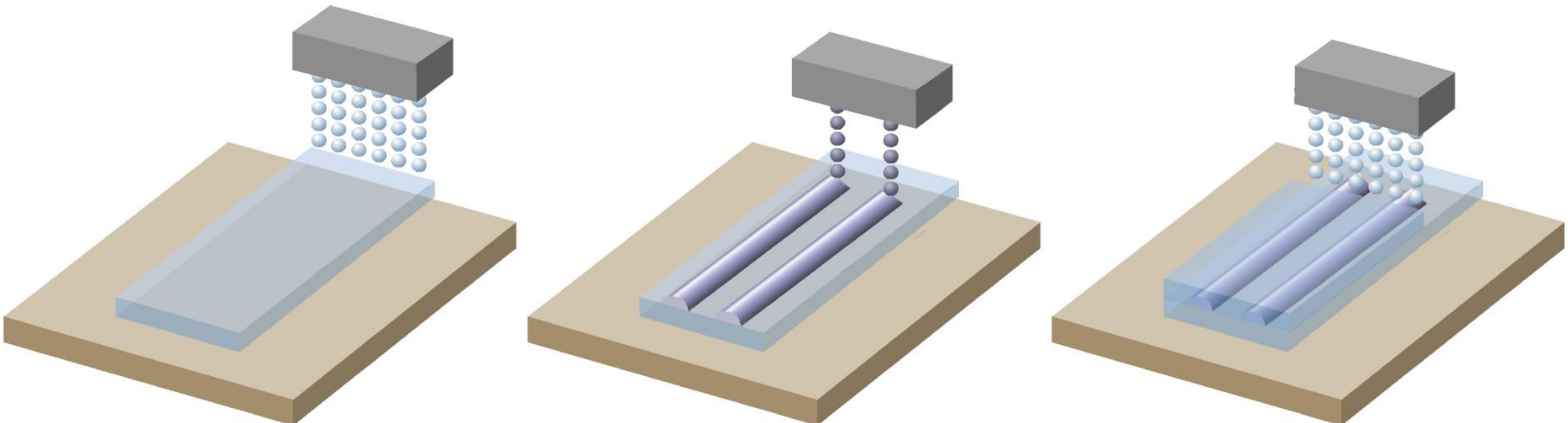
Plan View

- Straight structures machined in polymer
- Future work to investigate preparation of curved mirrors for out of plane interconnection

Inkjetting as a Route to Waveguide Deposition



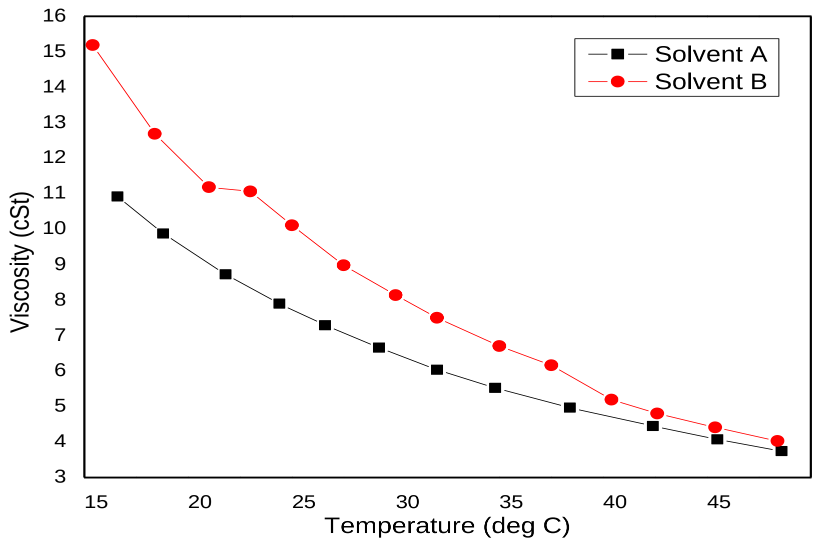
- Print polymer then UV cure
- Advantages:
  - controlled, selective deposition of core and clad
  - less wastage: picolitre volumes
  - large area printing
  - low cost

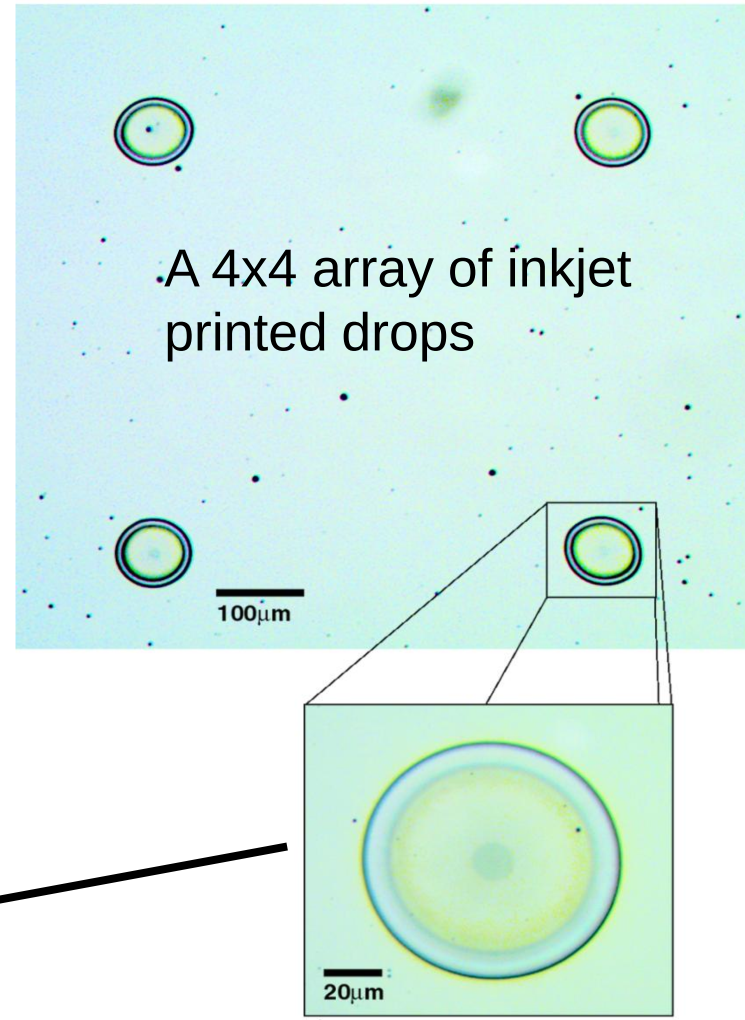


Deposit Lower Cladding | **Deposit Core** | **Deposit Upper Cladding**

Challenges of Inkjet Deposition

- Viscosity tailored to inkjet head via addition of solvent
- “Coffee stain” effects

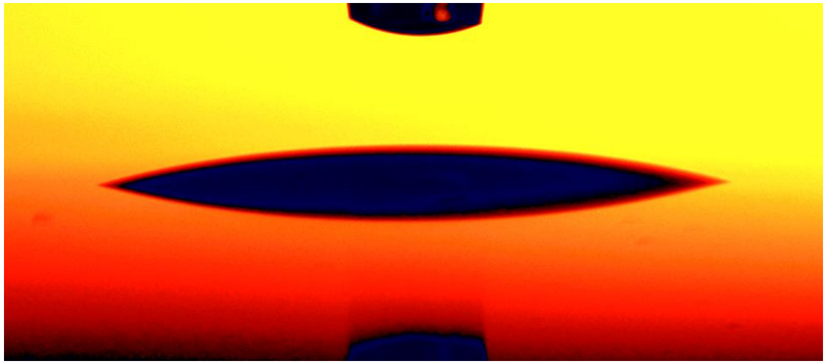


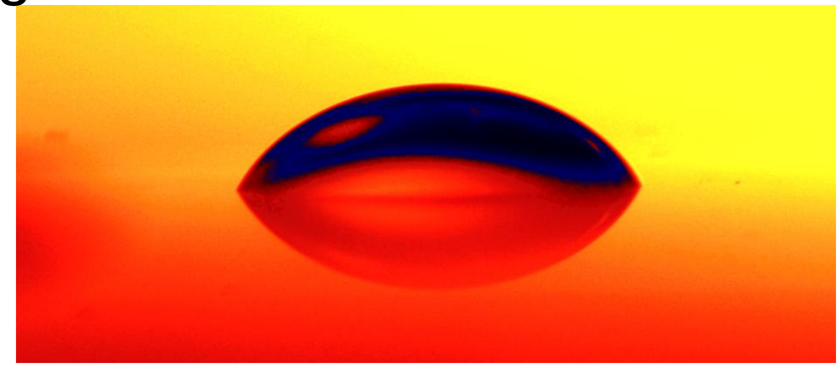


Cross-section of dried droplet
“coffee-stain” effect

Changing Surface Wettability

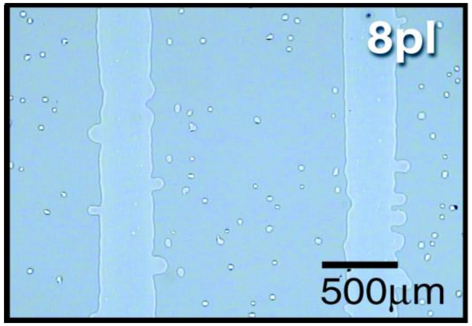
Contact Angles

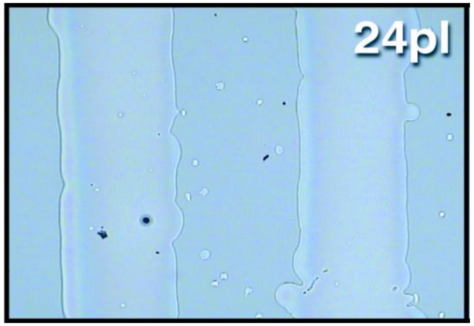


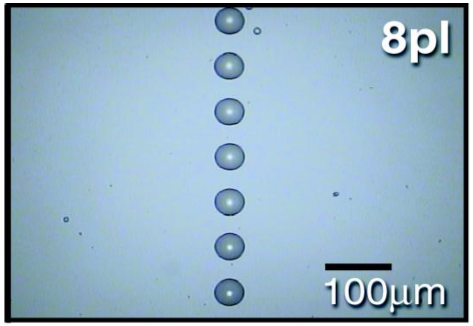


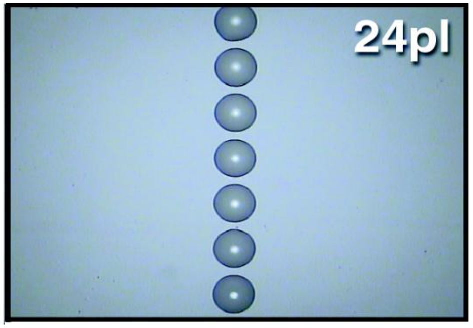
Core material on cladding

Core material on modified glass surface (hydrophobic)







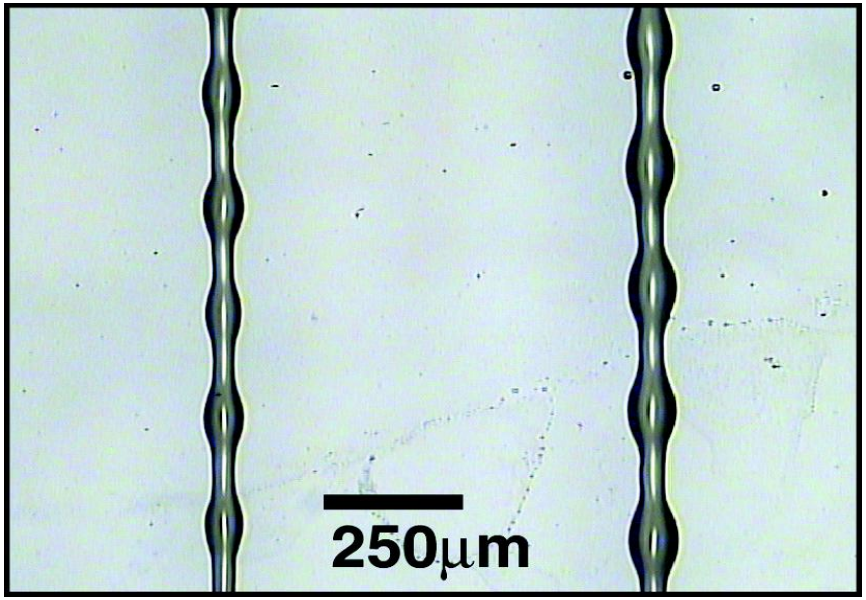


Large wetting - broad inkjetted lines

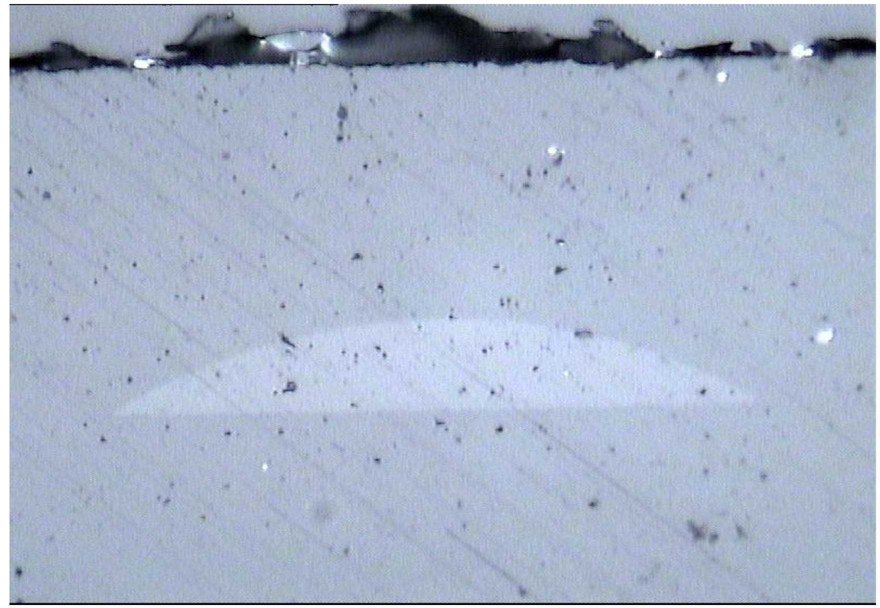
Reduced wetting – discrete droplets

Identical inkjetting conditions - spreading inhibited on modified surface

Towards Stable Structures



Stable line structures with periodic features

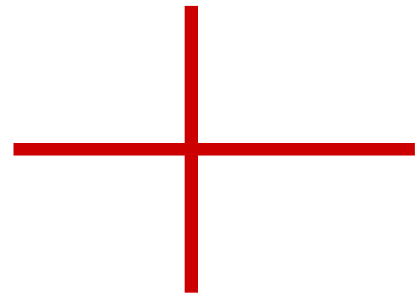


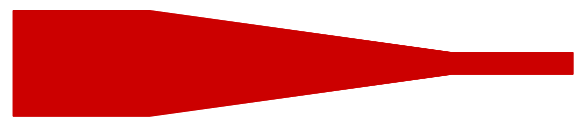
Cross section of inkjetted core material surrounded by cladding (width 80 microns)

A balance between wettability, line stability and adhesion

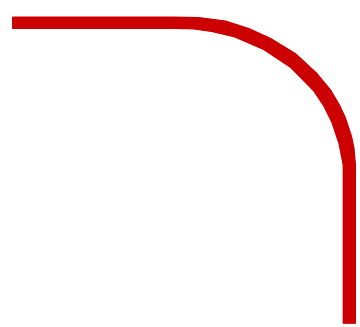
Waveguide components and measurements

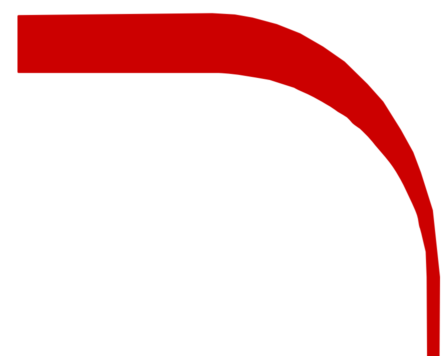
- Straight waveguides 480 mm x 70 µm x 70 µm
- Bends with a range of radii
- Crossings
- Spiral waveguides
- Tapered waveguides
- Bent tapered waveguides



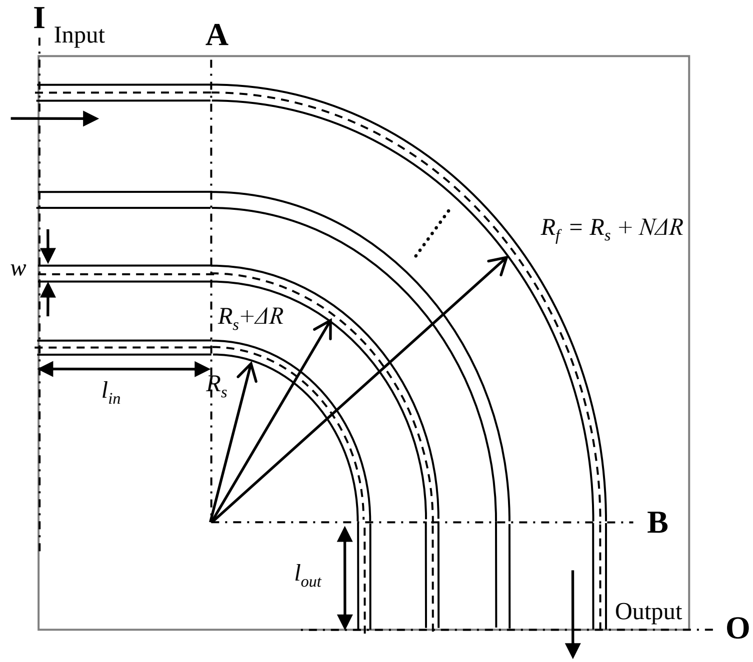


- Loss
- Crosstalk
- Misalignment tolerance
- Surface Roughness
- Bit Error Rate, Eye Diagram

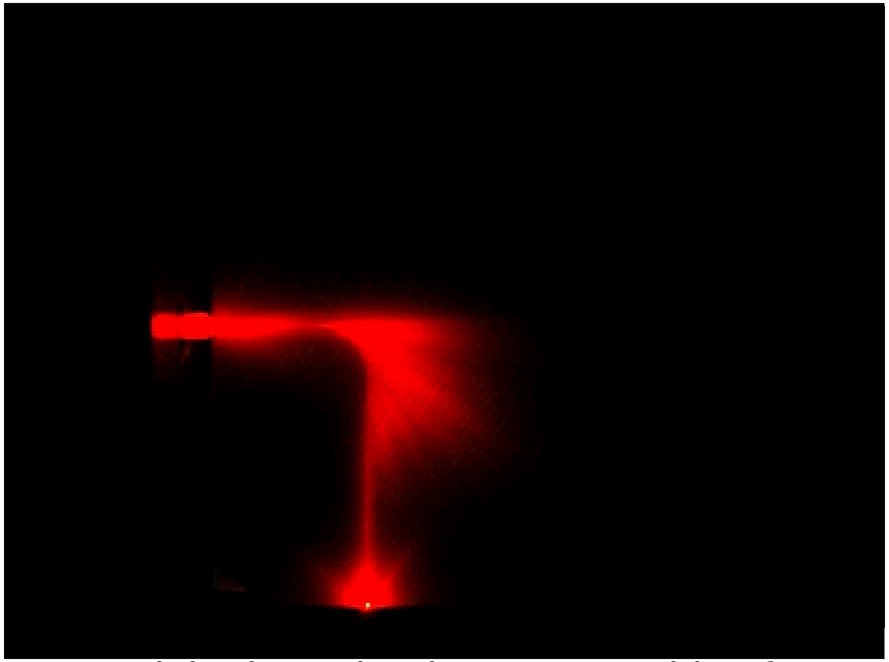




Optical Power Loss in 90 Waveguide Bends



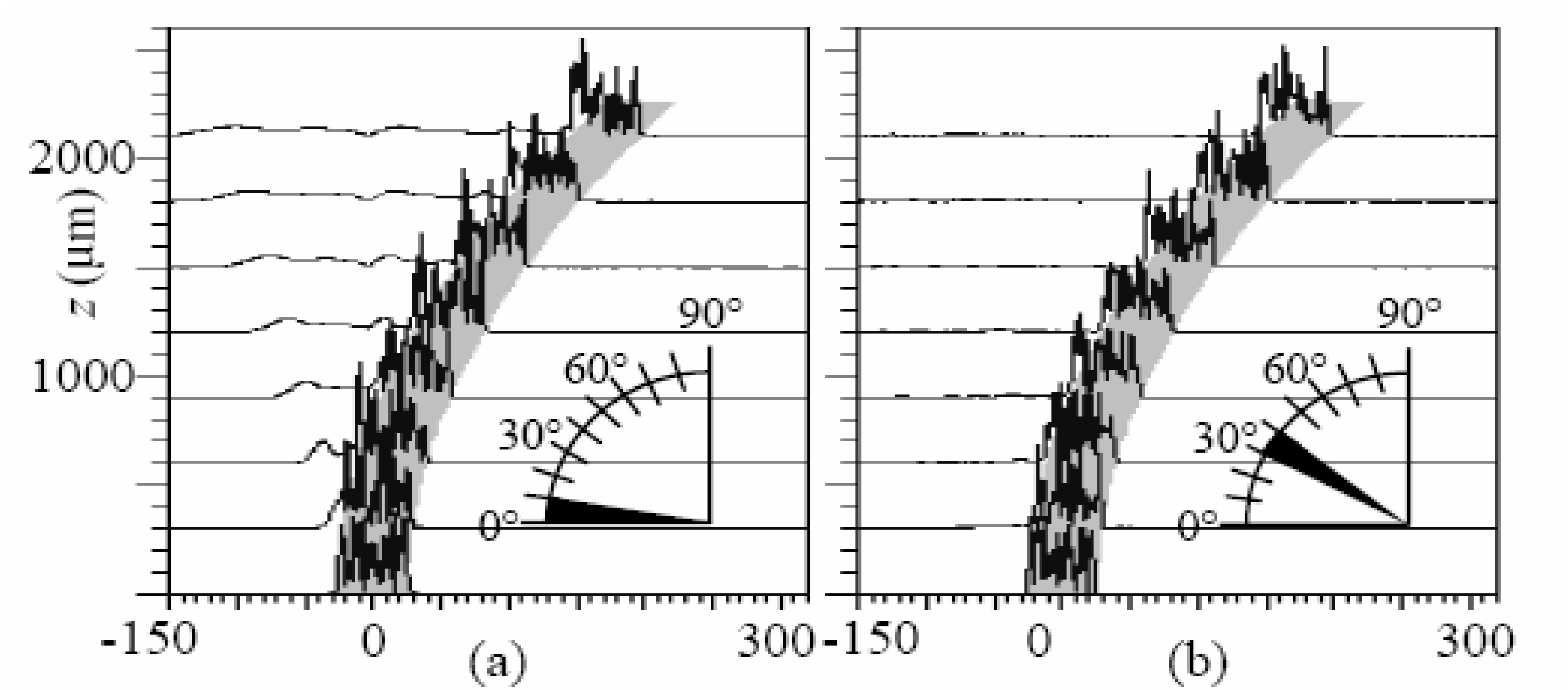
Schematic diagram of one set of curved waveguides.



Light through a bent waveguide of *R* = 5.5 mm – 34.5 mm

- Radius *R*, varied between 5.5 mm < *R* < 35 mm, *ΔR* = 1 mm
- Light lost due to scattering, transition loss, bend loss, reflection and back-scattering
- Illuminated by a MM fiber with a red-laser.

BPM, beam propagation method modeling of optical field in bend segments

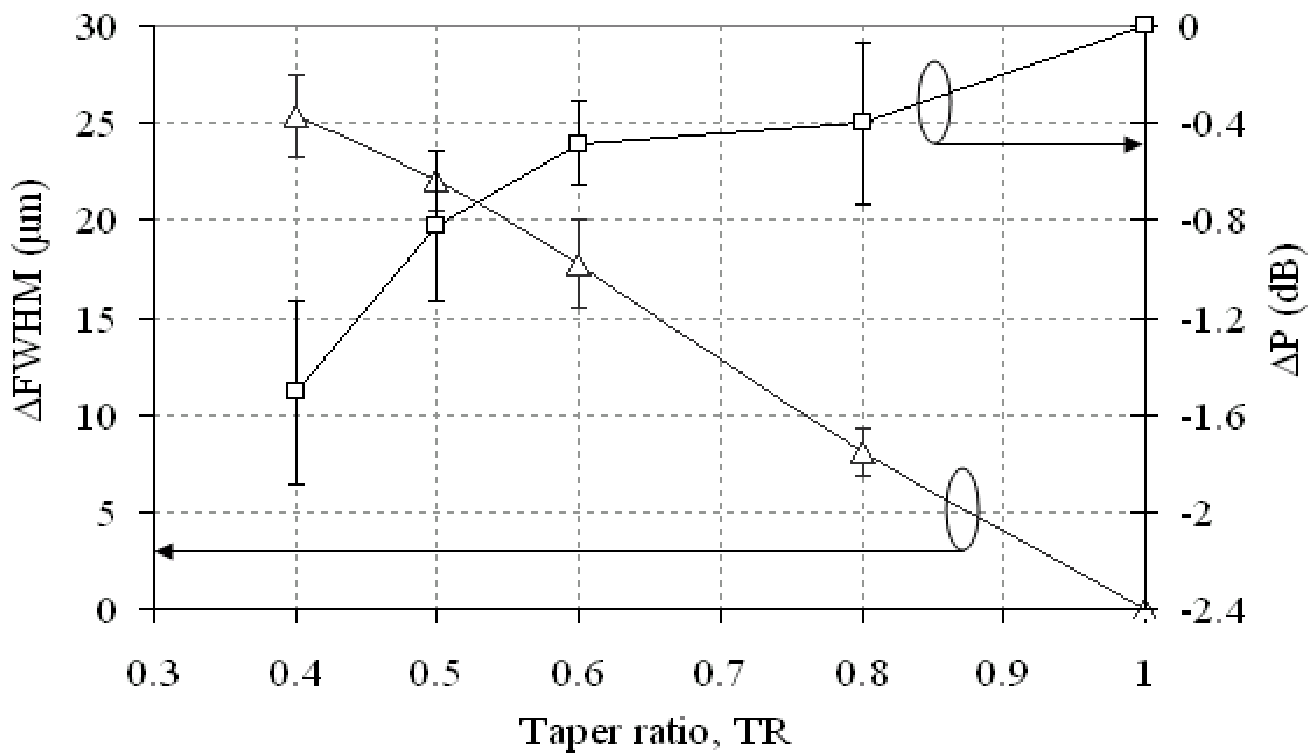


w = 50 μm, R = 13 mm

(left picture) in the first segment (first 10°).

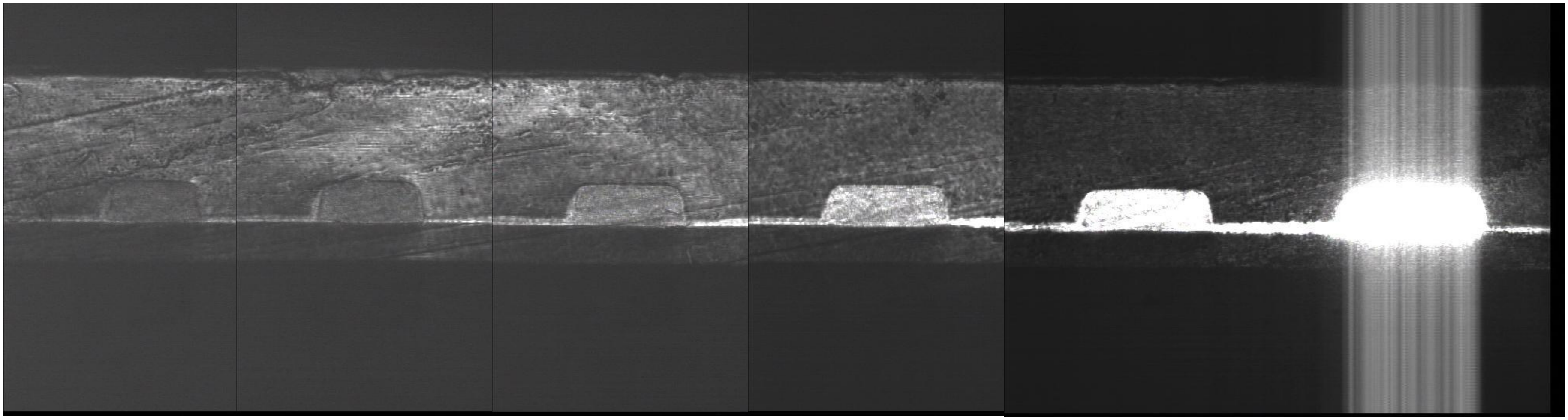
(right picture) in the 30° to 40° degree segment.

Differences in misalignment tolerance and loss as a function of taper ratio



- Graph plots the differences between a tapered bend and a bend
- There is a trade off between insertion loss and misalignment tolerance

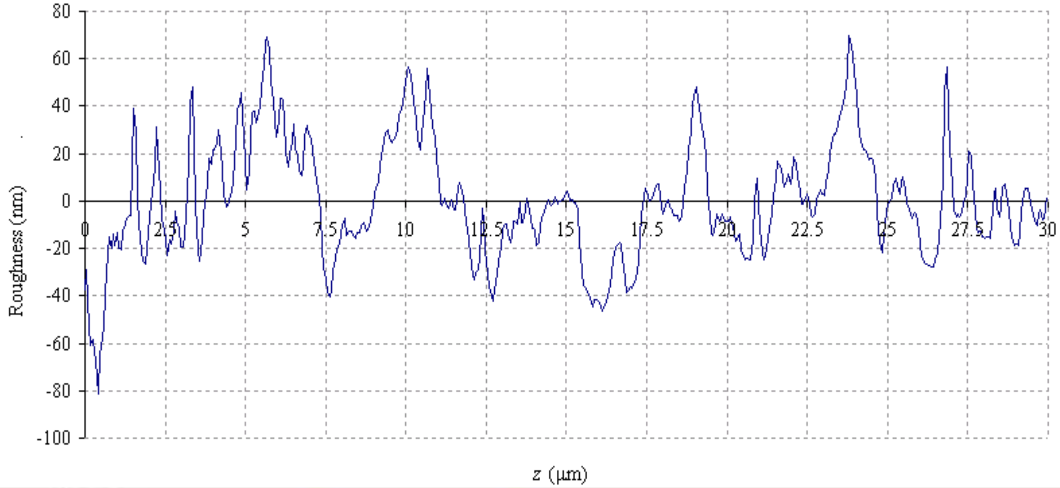
Crosstalk in Chirped Width Waveguide Array



100 µm 110 µm 120 µm 130 µm 140 µm 150 µm

- Light launched from VCSEL imaged via a GRIN lens into 50 µm x 150 µm waveguide
- Photolithographically fabricated chirped with waveguide array
- Photomosaic with increased camera gain towards left

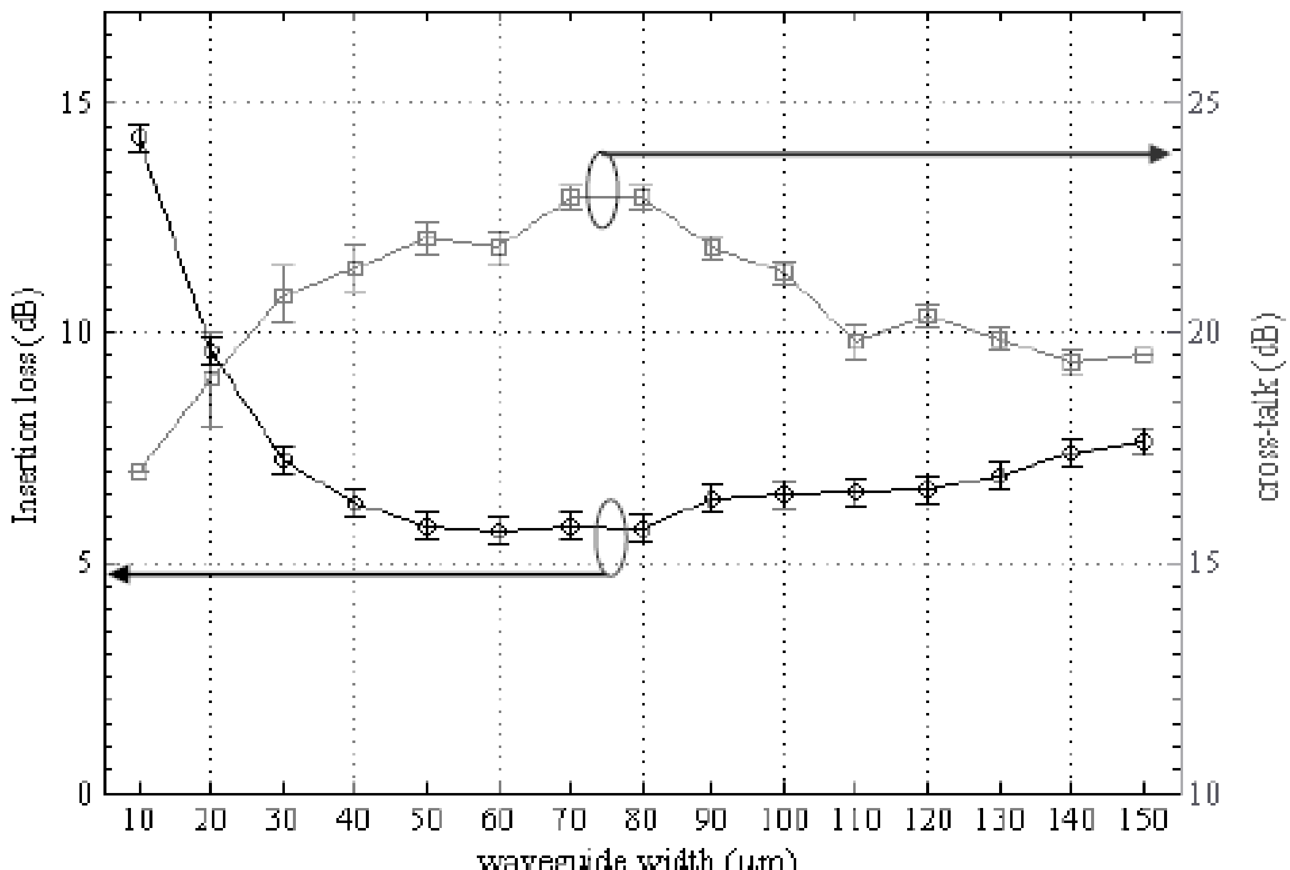
Surface roughness



- RMS side wall roughness: 9 nm to 74 nm

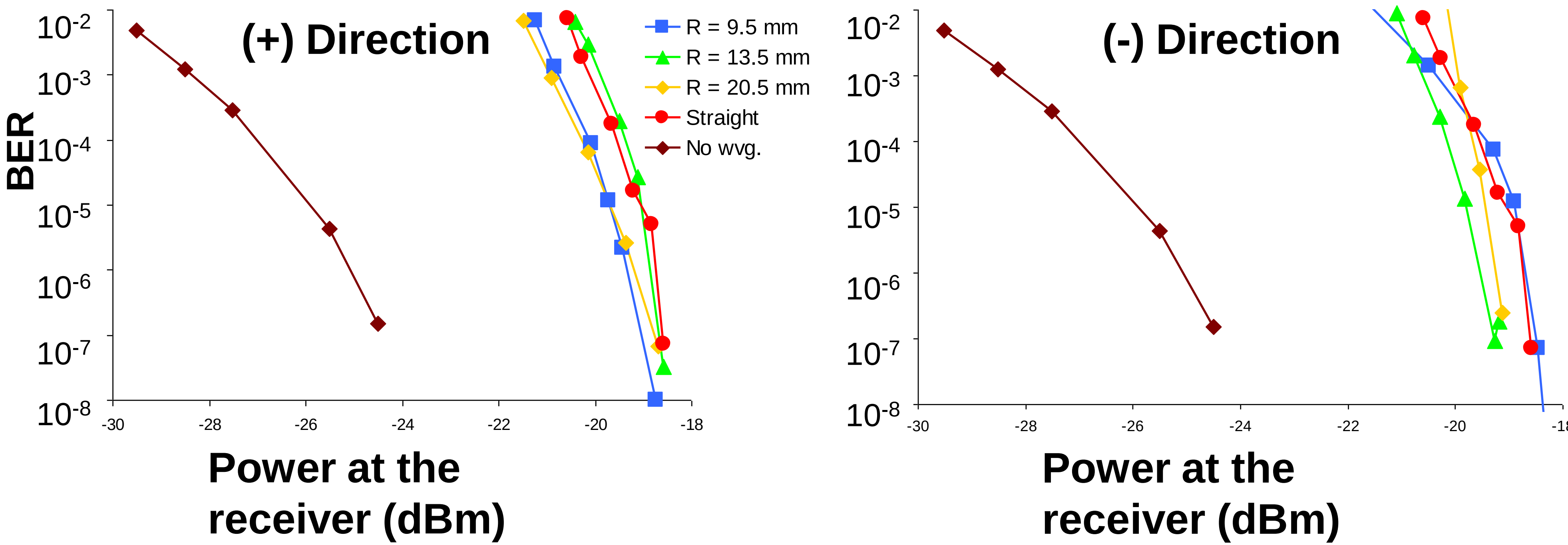
- RMS polished end surface roughness: 26 nm to 192 nm.

Design rules for waveguide width depending on insertion loss and cross-talk

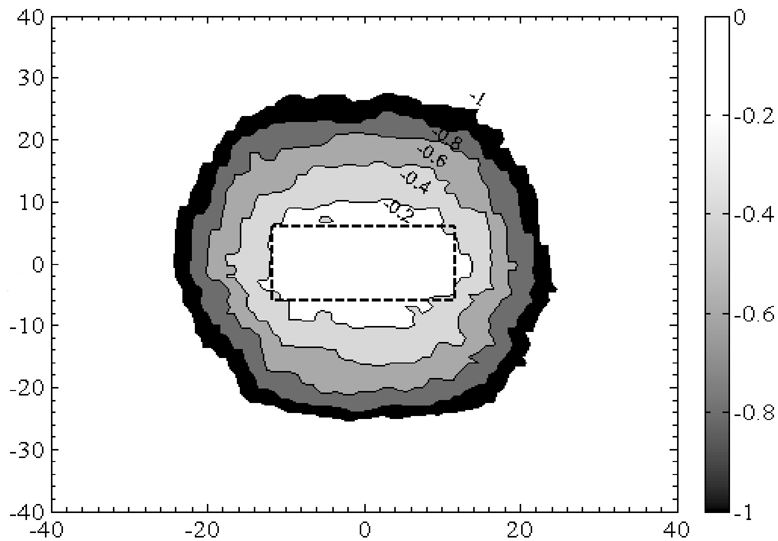


6~7dB for a 70 μm width waveguide

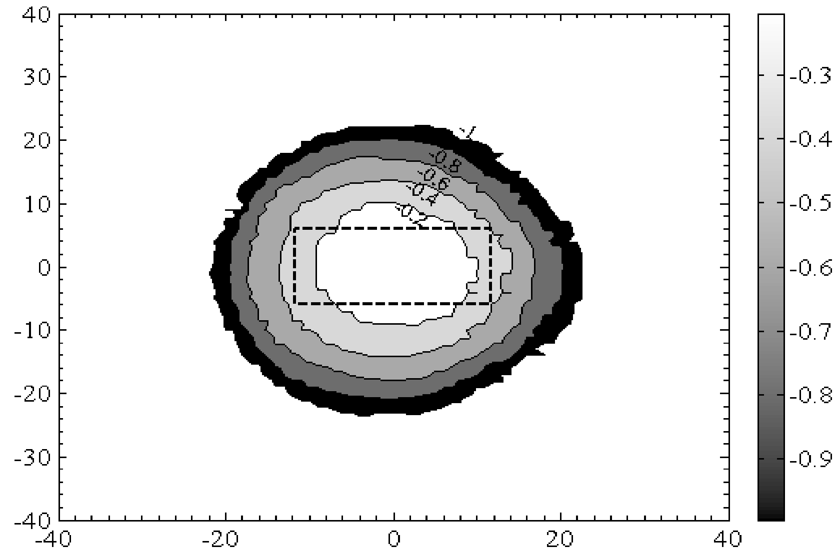
Bit error rate for laterally misaligned 1550 nm 2.5 Gb/s DFB laser



Contour map of VCSEL and PD misalignment



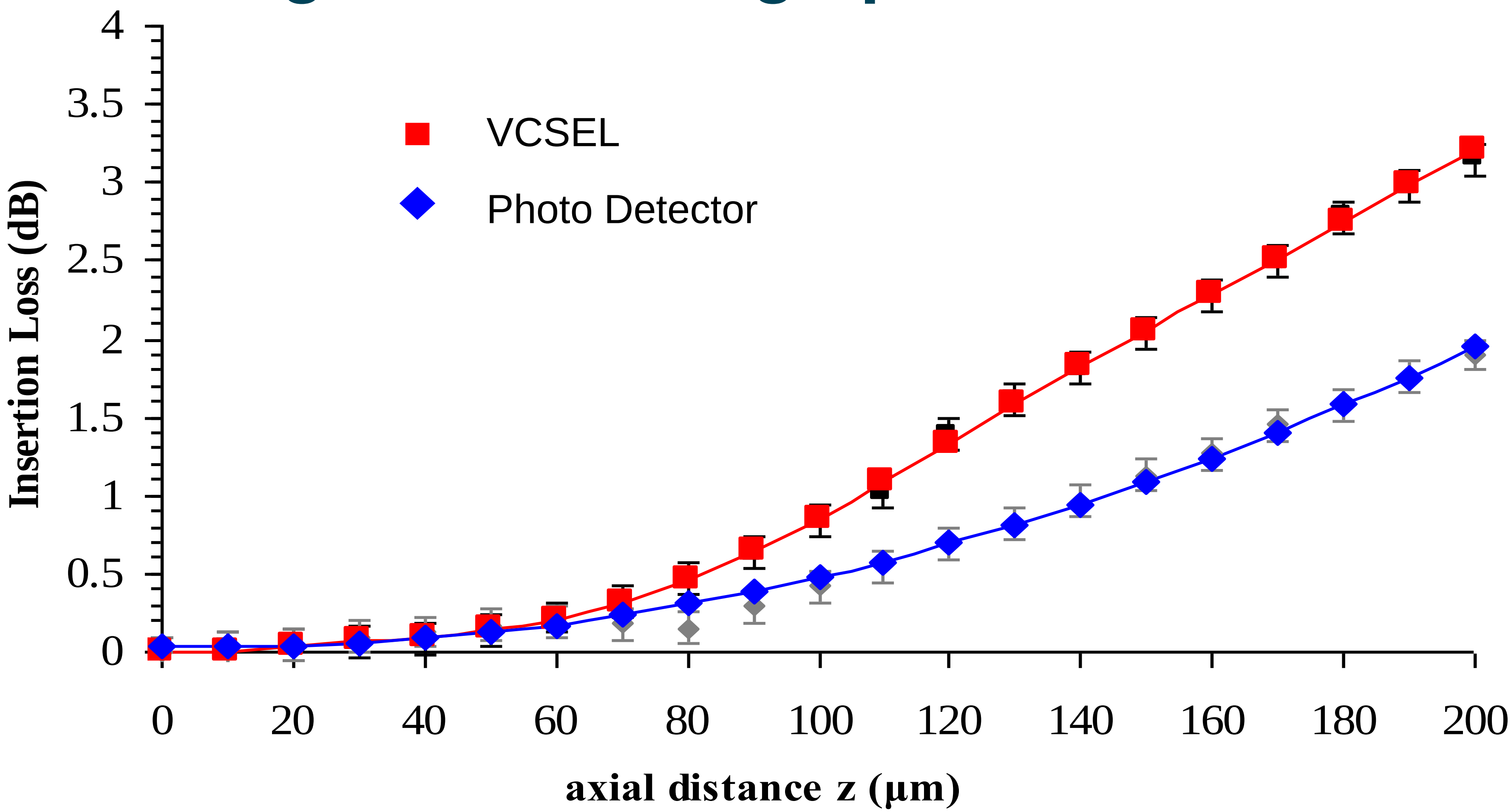
(a) Contour map of relative insertion loss compared to the maximum coupling position for VCSEL misalignment at z = 0.



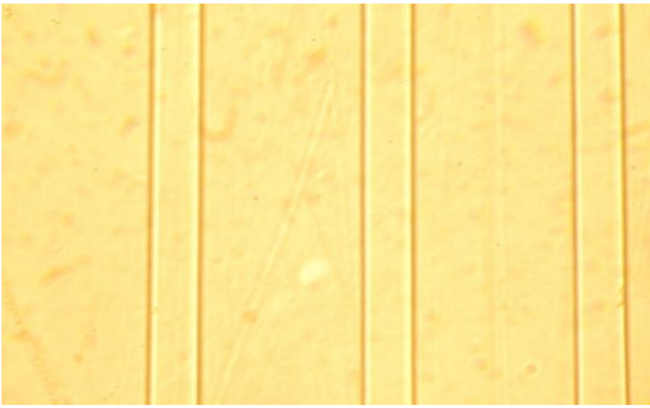
(b) Same for PD misalignment at *z* = 0. Resolution step was $\Delta x = \Delta y = 1$ µm.

- Dashed rectangle is the expected relative insertion loss according to the calculated misalignments along *x* and *y*.
- The minimum insertion loss was 4.4 dB, corresponded to x = 0, y = 0, z = 0

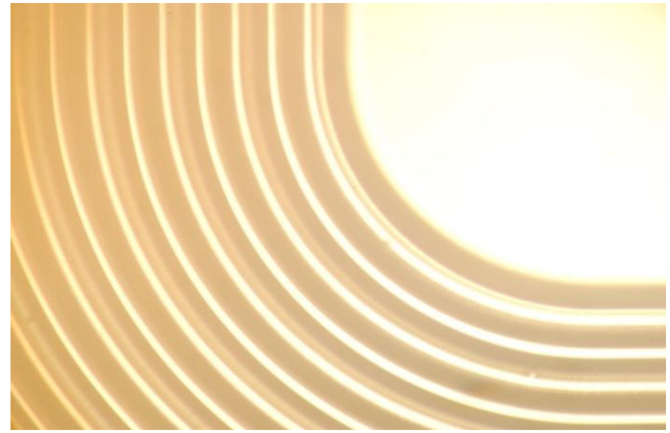
Coupling Loss for VCSEL and PD for misalignments along optic axis



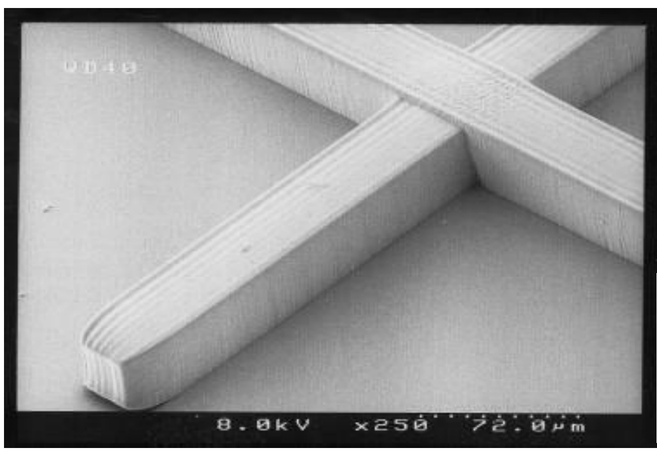
Fabrication Techniques and Waveguides Samples



Straight waveguides – Optical InterLinks



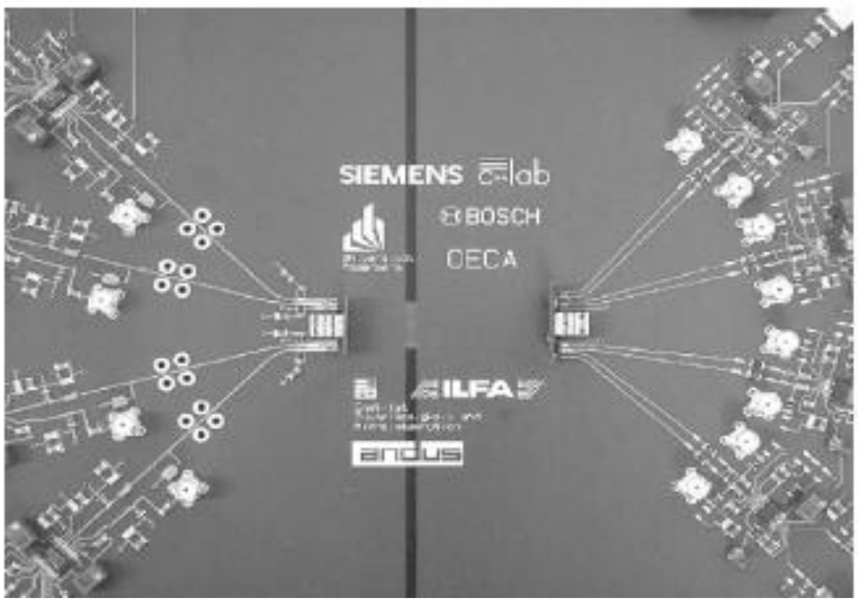
90° Crossings – Dow Corning

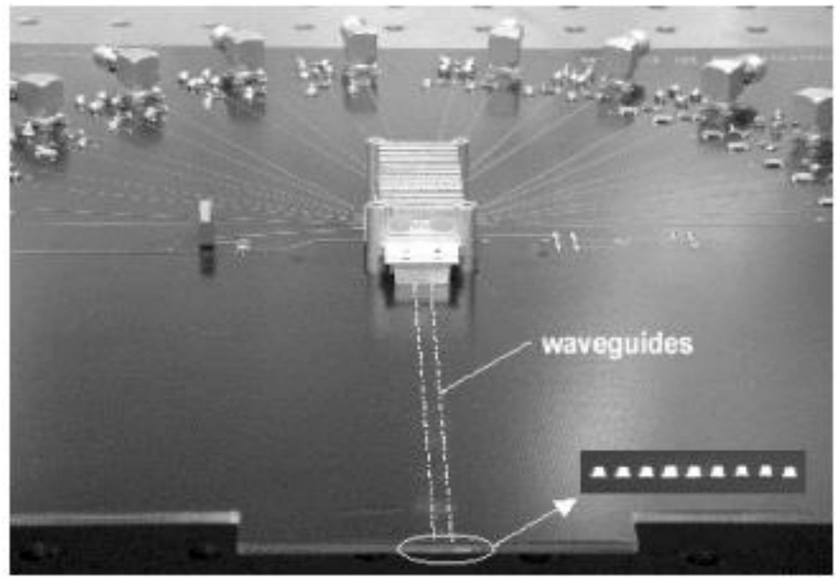


90° Crossings – Heriot Watt University

50° Crossings – Exxelis

Siemens C-Labs Test Board (Griese, 2002)





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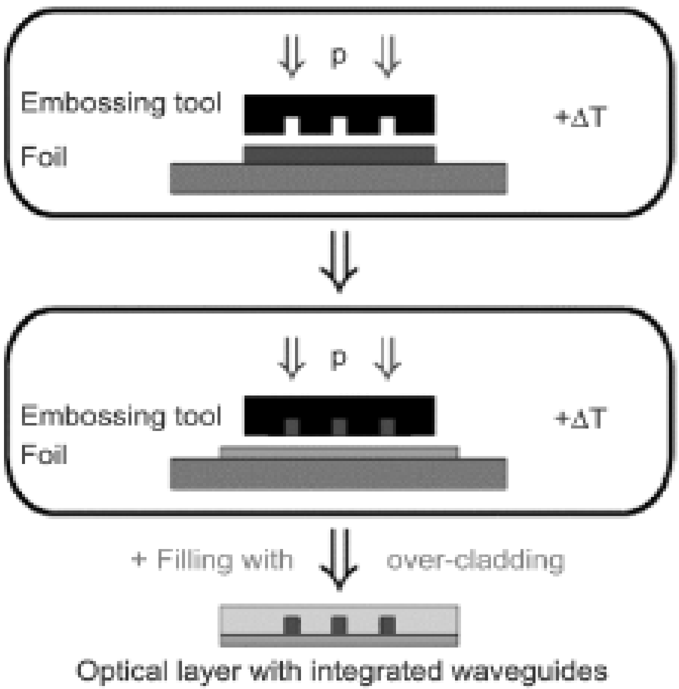
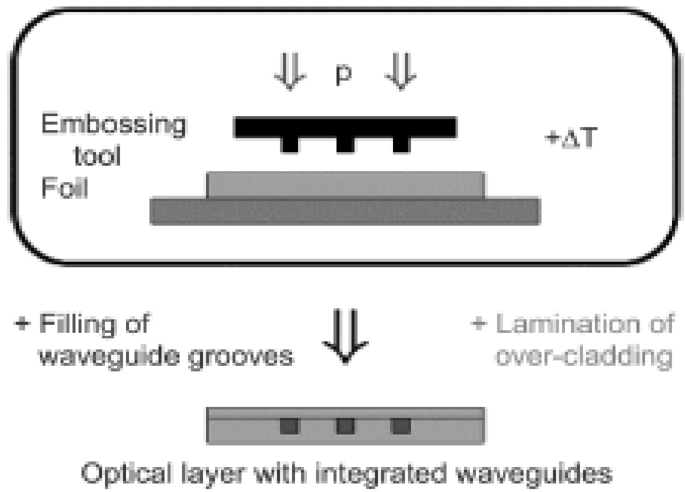
Waveguide Fabrication by Two Hot Embossing Methods (Griese, 2002)

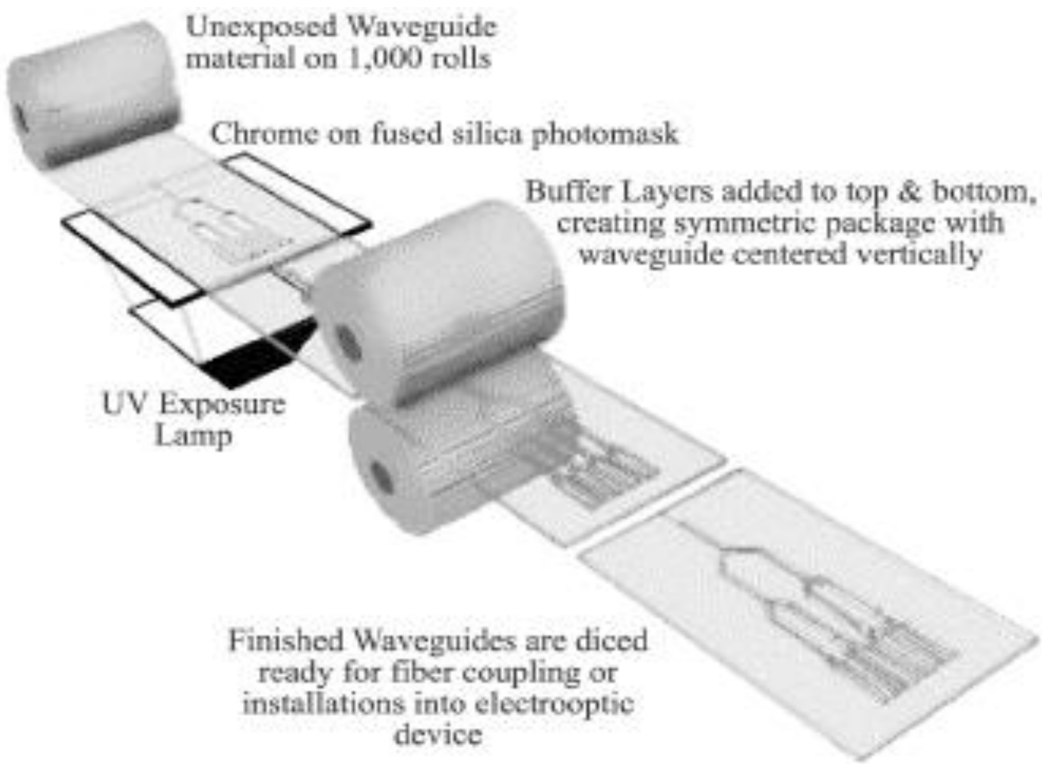


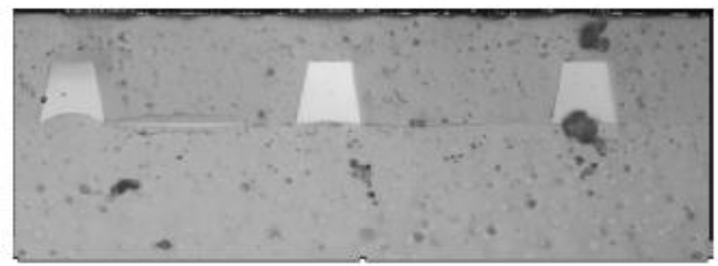
(a)



(b)

TOPCat Polymer optical waveguide cores with overcladding (Watsun 2001)





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TOPCat optical waveguide fabrication process

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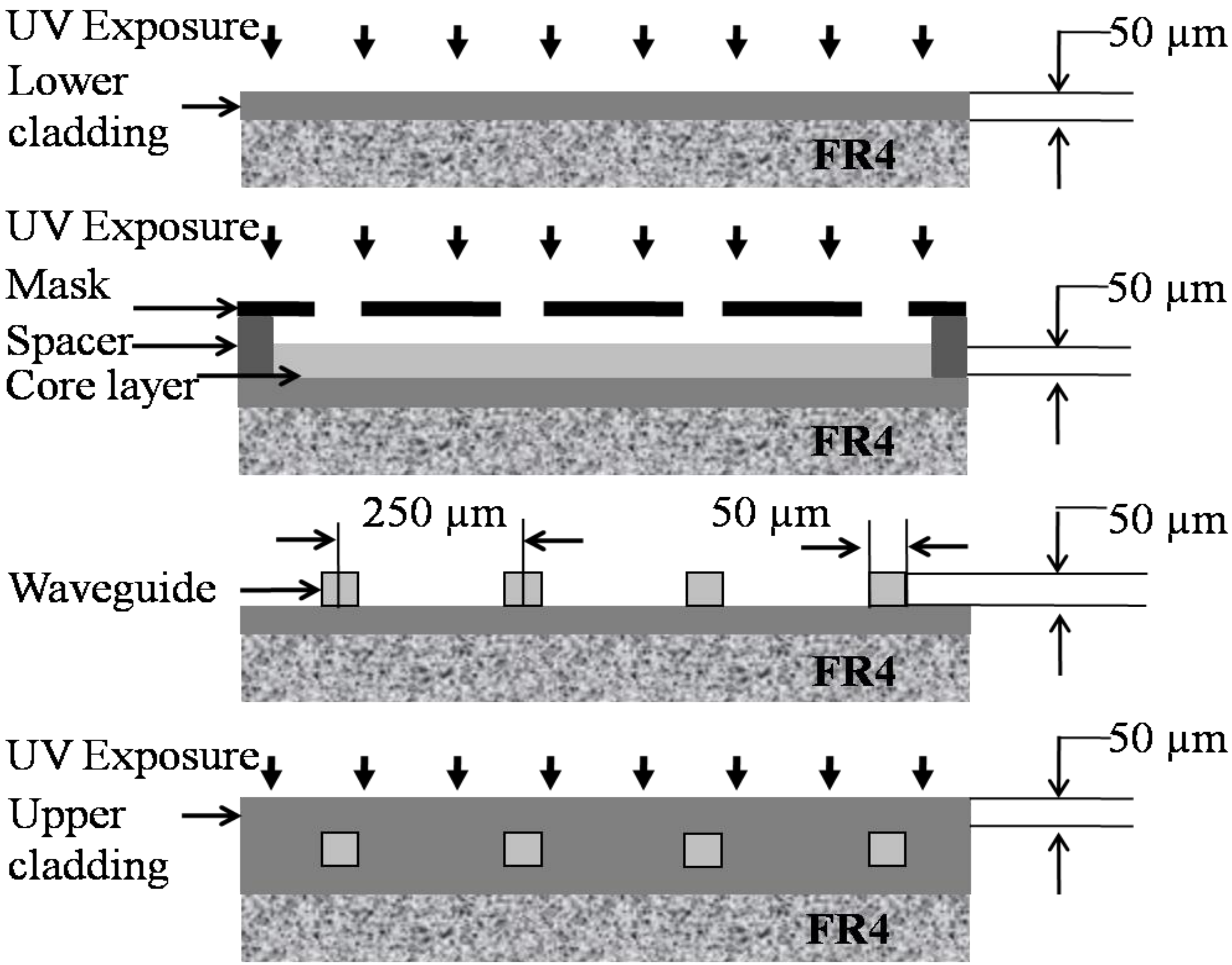
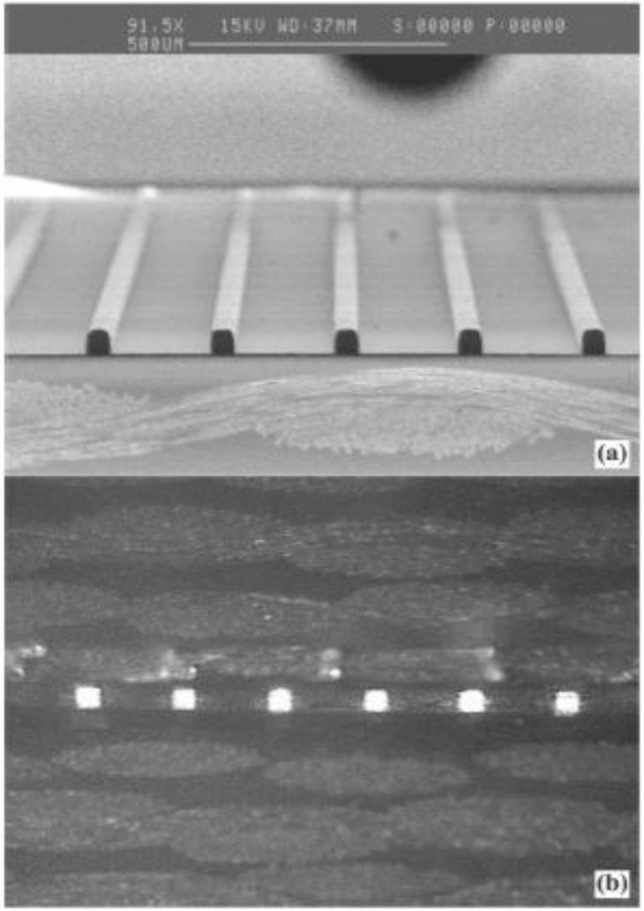
Photolithographic Fabrication of Waveguides



Polymer waveguides formed by Photolithography in Truemode® polymer



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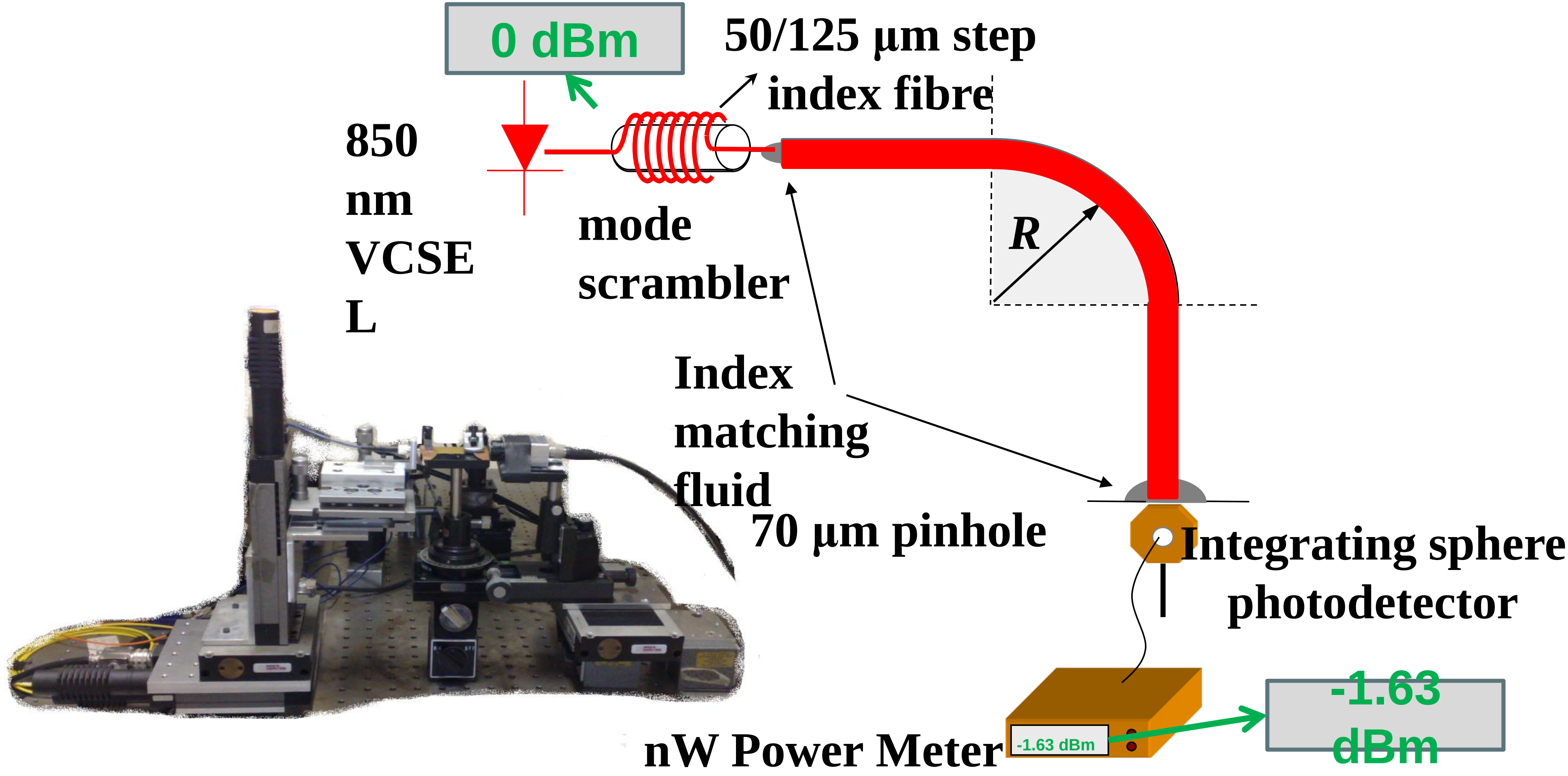
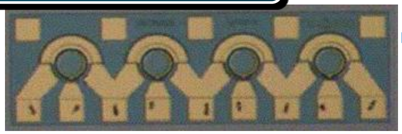
Optical Loss Measurement



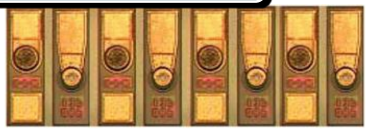
VCSEL Array for Crosstalk Measurement

PIN Array



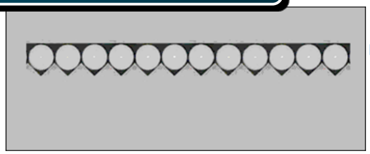
Source: **Microsemi Corporation**

VCSEL Array

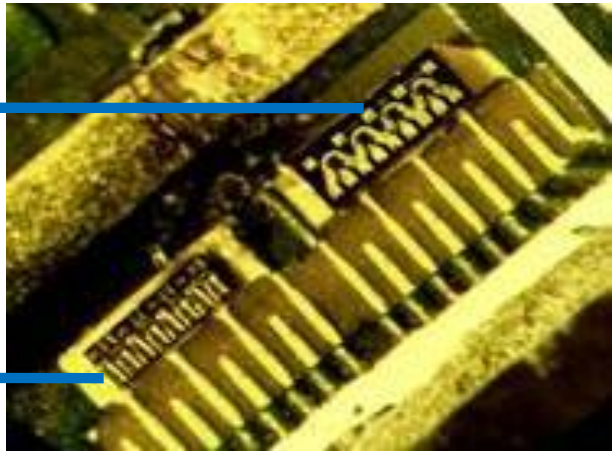


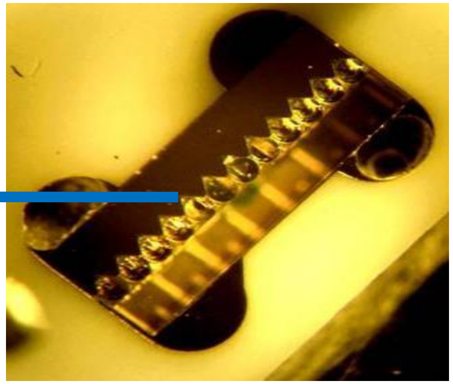
Source: **ULM Photonics GmbH**

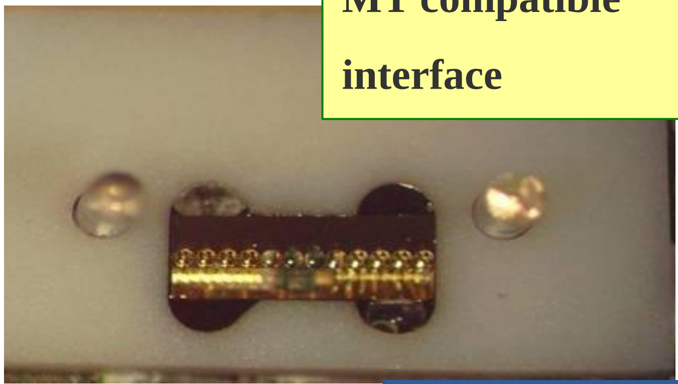
GRIN Lens Array



Source: **GRINTech GmbH**

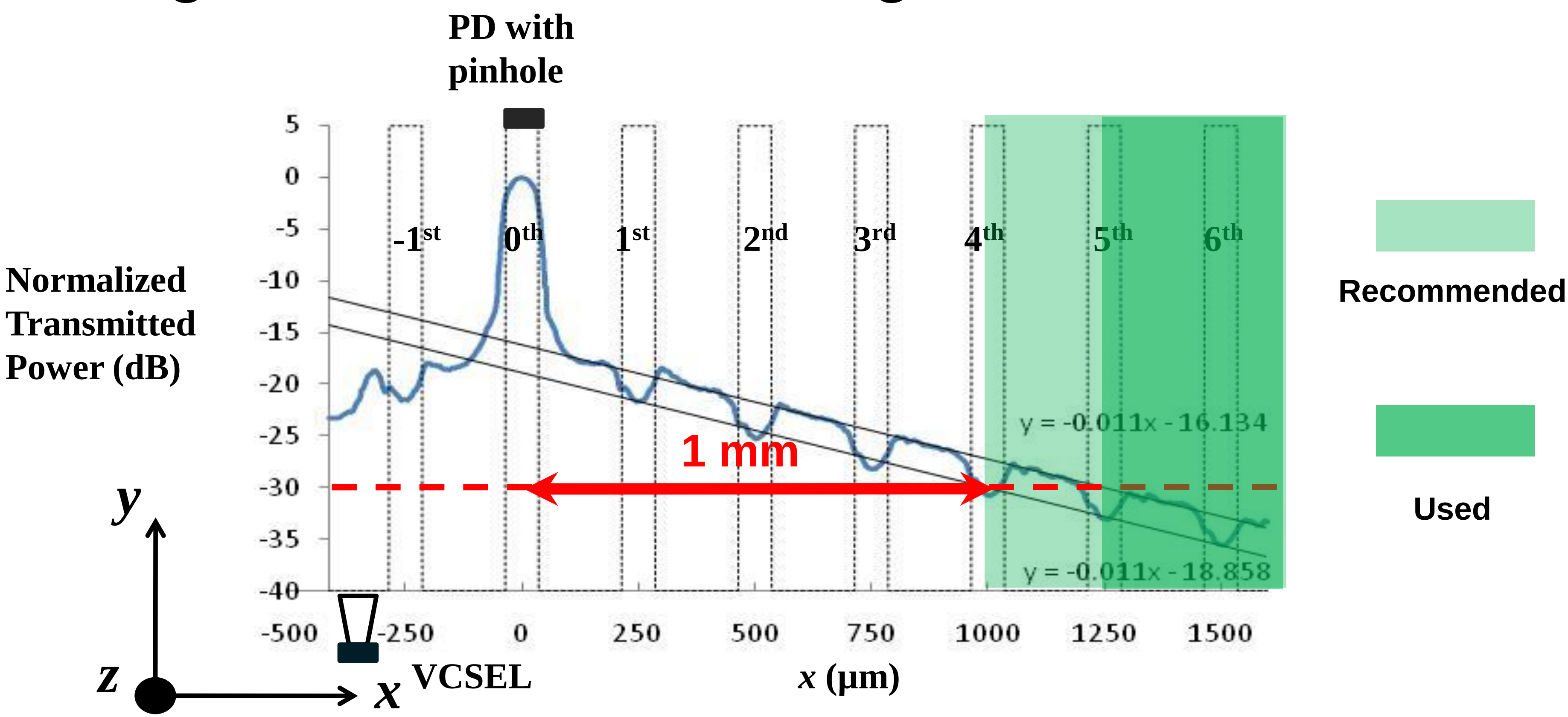






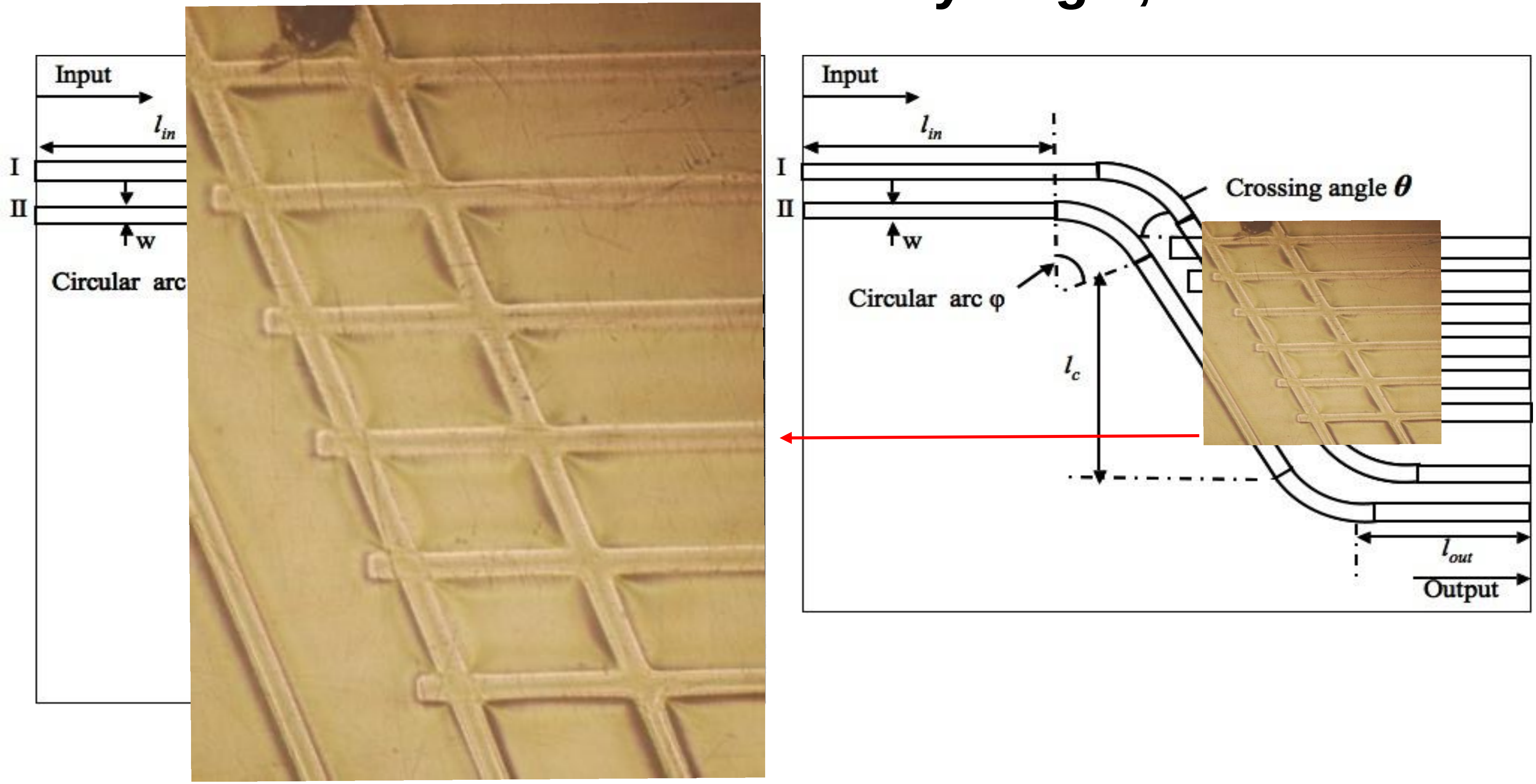
MT compatible interface

Design Rules for Inter-waveguide Cross Talk

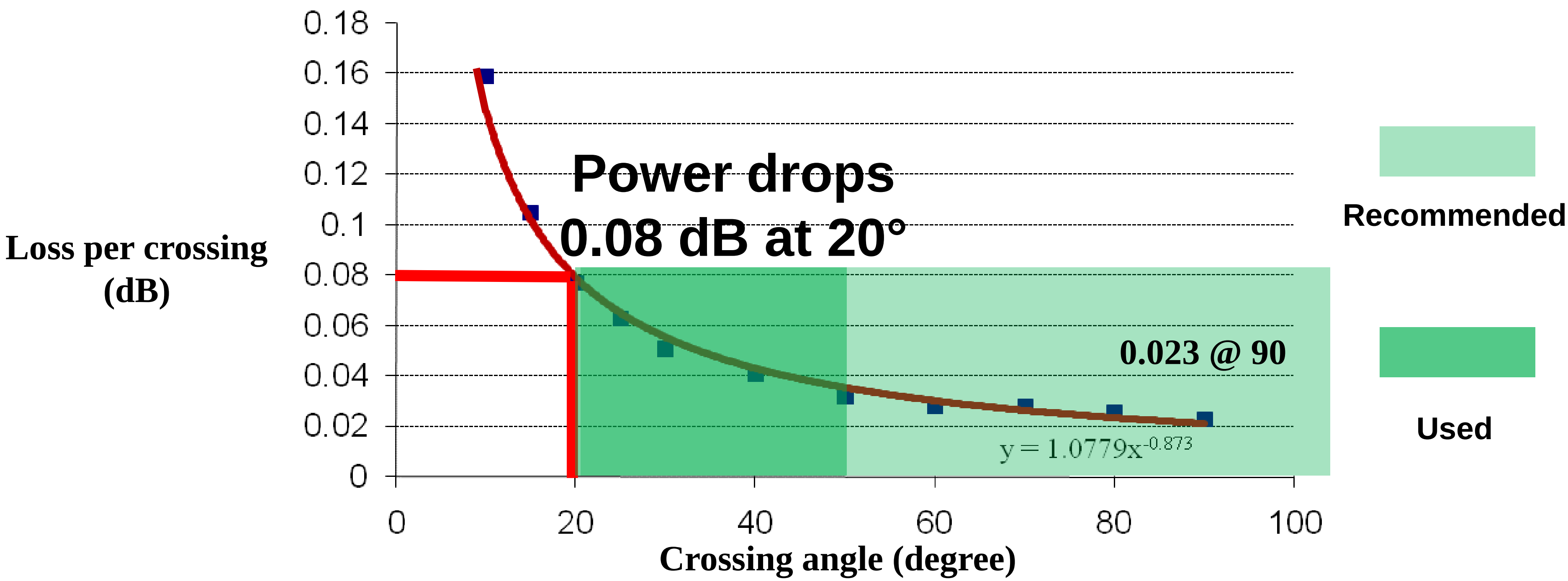


- 70 µm × 70 µm waveguide cross sections and 10 cm long
- In the cladding power drops linearly at a rate of 0.011 dB/µm
- Crosstalk reduced to -30 dB for waveguides 1 mm apart

Schematic Diagram Of Waveguide Crossings at 90° and at an Arbitrary Angle, θ

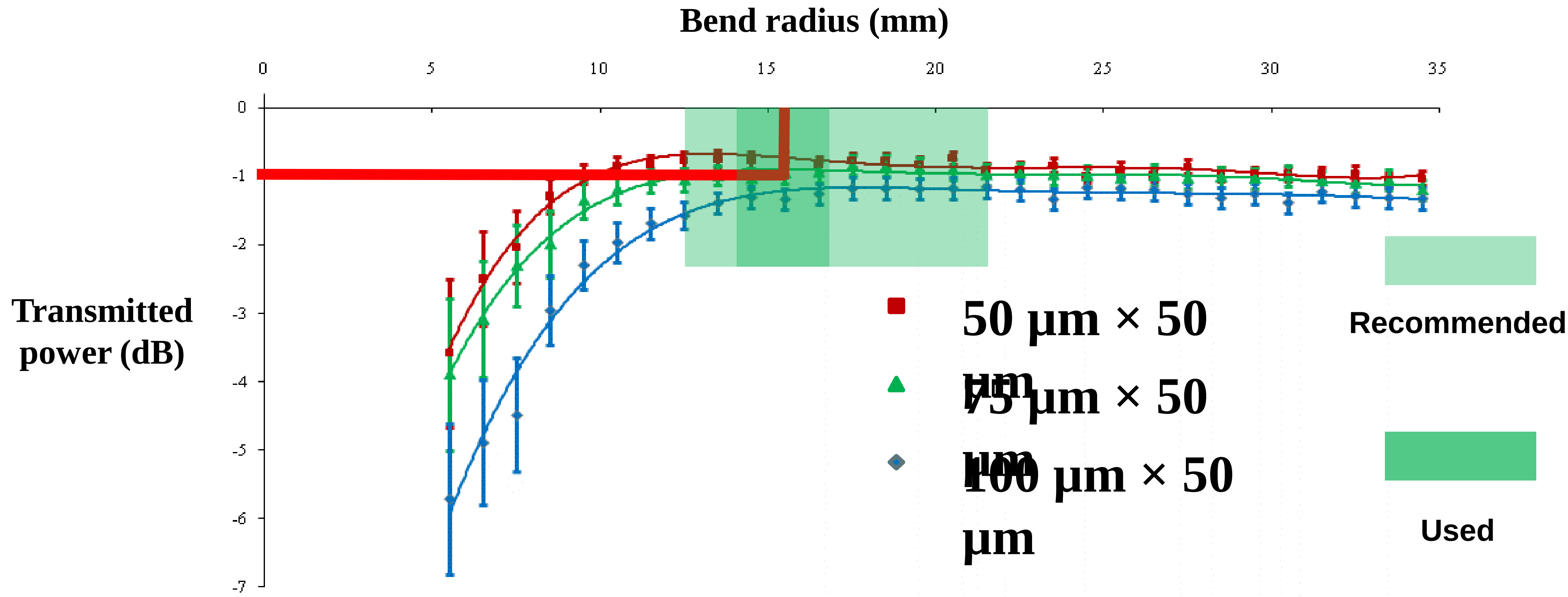


Design Rules for Arbitrary Angle Crossings



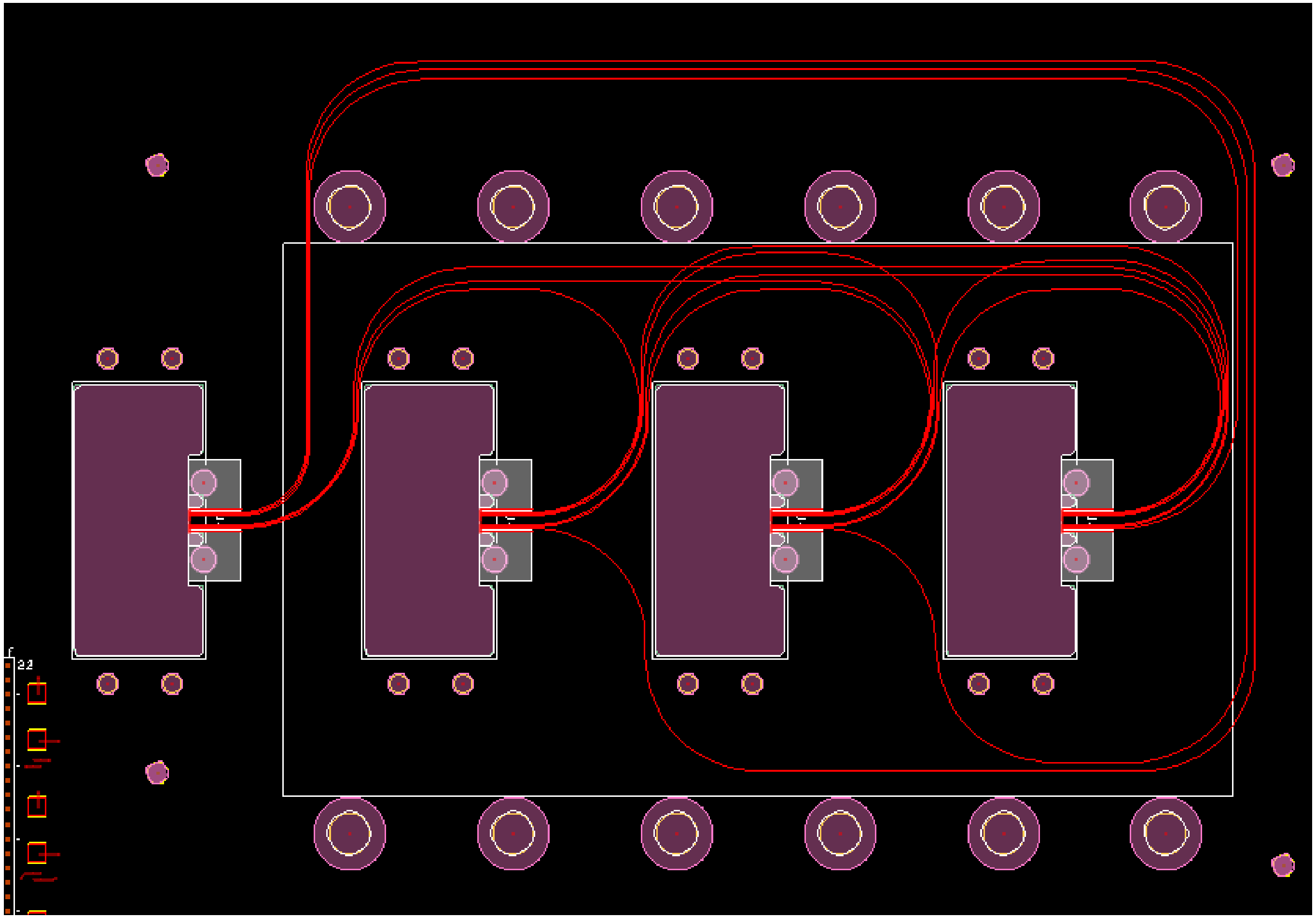
- Loss of 0.023 dB per 90° crossing consistent with other reports
- The output power dropped by 0.5% at each 90° crossing
- The loss per crossing (L_c) depends on crossing angle (θ), $L_c = 1.0779 \cdot \theta^{-0.8727}$.

Loss of Waveguide Bends



Width (µm)	Optimum Radius (mm)	Maximum Power (dB)
50	13.5	-0.74
75	15.3	-0.91
100	17.7	-1.18

System Demonstrator

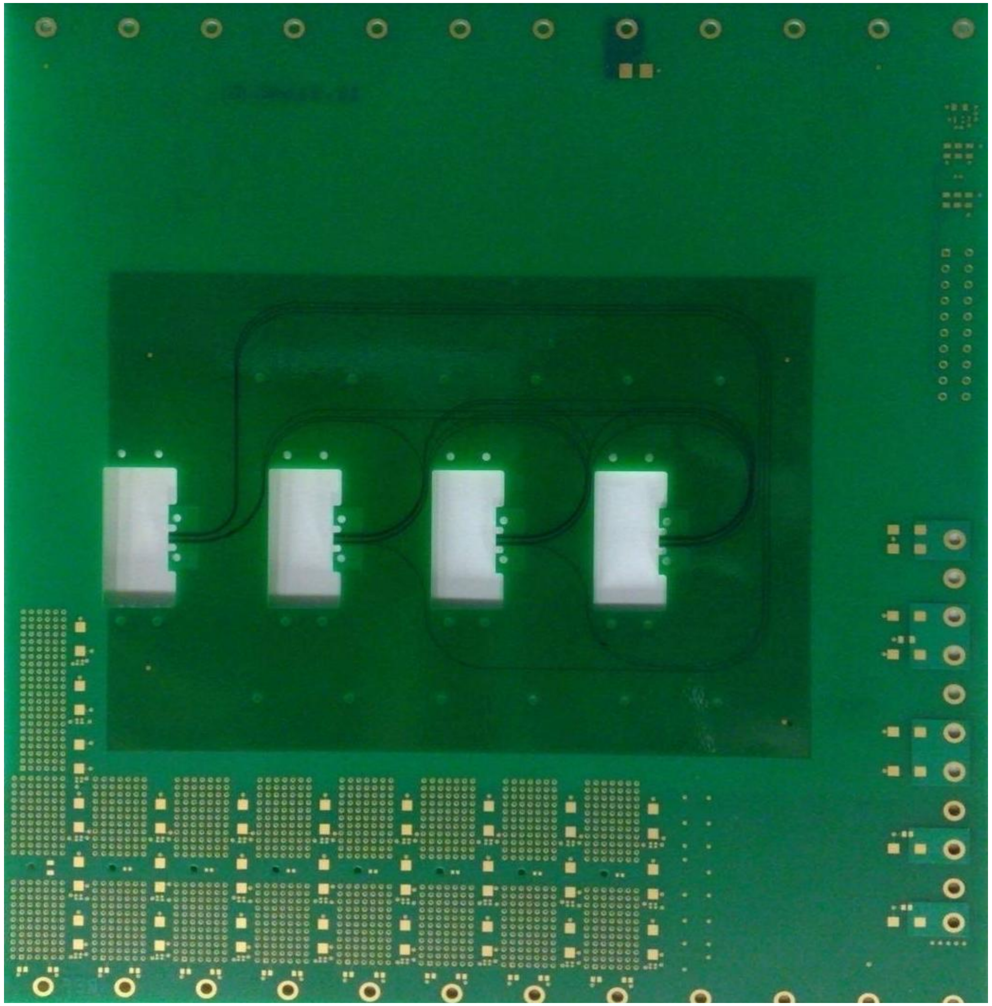


Fully connected waveguide layout using design rules

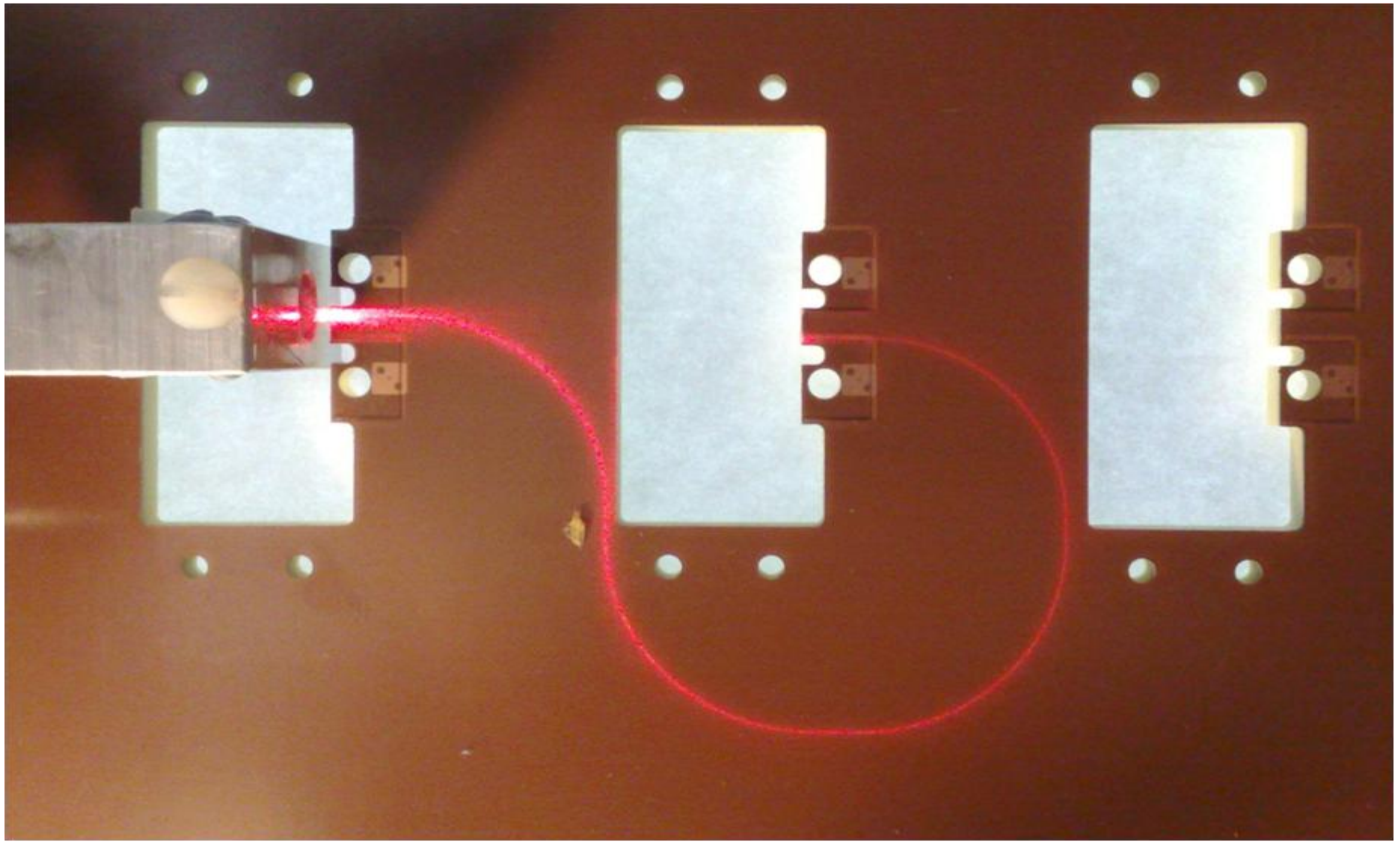
Power Budget

<table>
<tr><td>Input power (dBm/mW)</td><td colspan="30">-2.07 / 0.62</td></tr>
<tr><td></td><td colspan="30">Bend 90°</td></tr>
<tr><td>Radii (mm)</td><td colspan="5">15.000</td><td colspan="5">15.250</td><td colspan="5">15.500</td><td colspan="5">15.725</td><td colspan="5">16.000</td><td colspan="5">16.250</td></tr>
<tr><td>Loss per bend (dB)</td><td colspan="5">0.94</td><td colspan="5">0.91</td><td colspan="5">0.94</td><td colspan="5">0.94</td><td colspan="5">0.95</td><td colspan="5">0.95</td></tr>
<tr><td></td><td colspan="30">Crossings</td></tr>
<tr><td>Crossing angles (°)</td><td colspan="6">22.27</td><td colspan="6">29.45</td><td colspan="6">36.23</td><td colspan="6">42.10</td><td colspan="6">47.36</td></tr>
<tr><td>Loss per crossing (dB)</td><td colspan="6">0.078</td><td colspan="6">0.056</td><td colspan="6">0.047</td><td colspan="6">0.041</td><td colspan="6">0.037</td></tr>
<tr><td>Min. detectable power (dBm)</td><td colspan="30">-15 / 0.03</td></tr>
<tr><td>Min. power no bit error rate</td><td colspan="30">-12 / 0.06</td></tr>
</table>

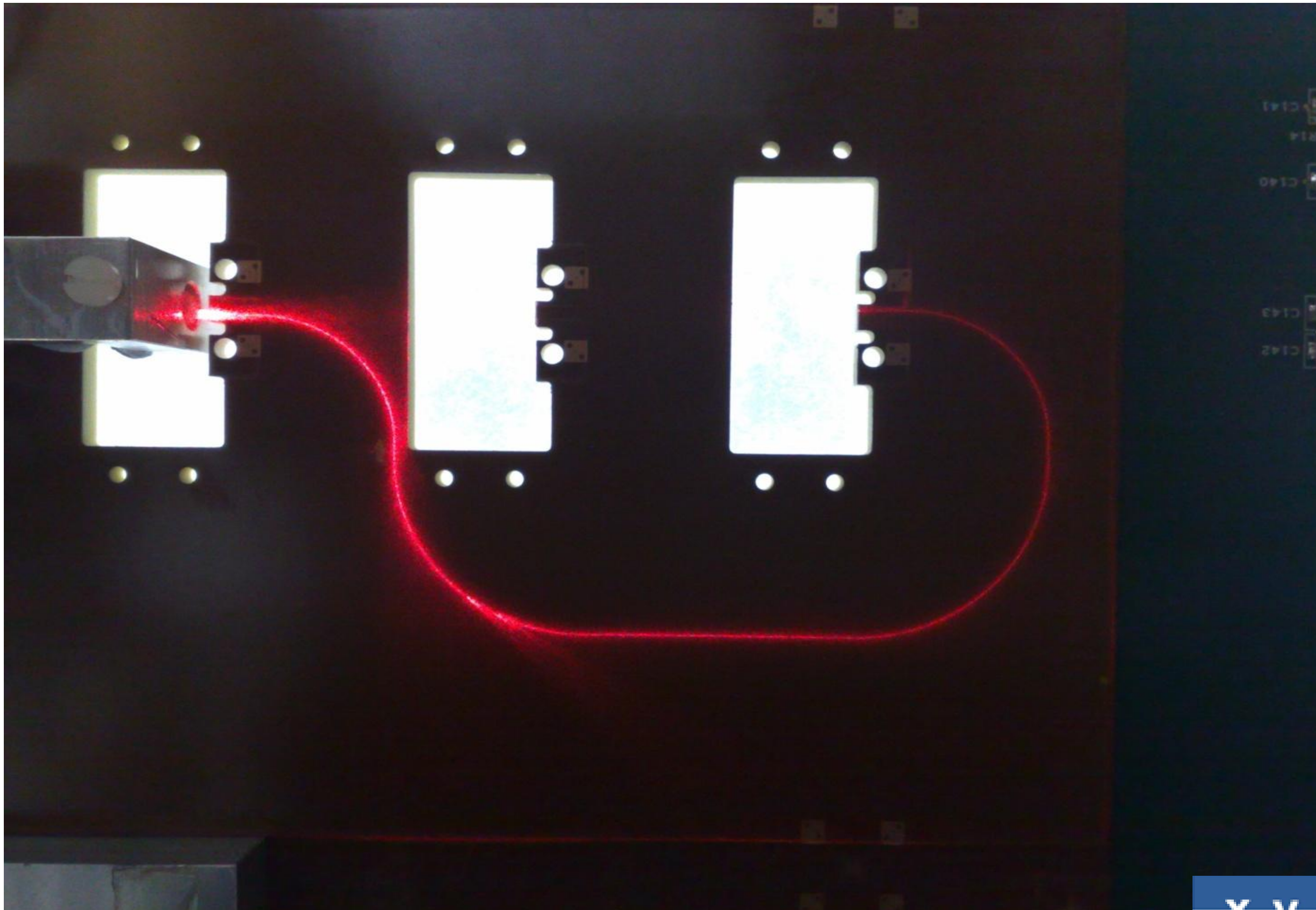
Demonstrator Dummy Board



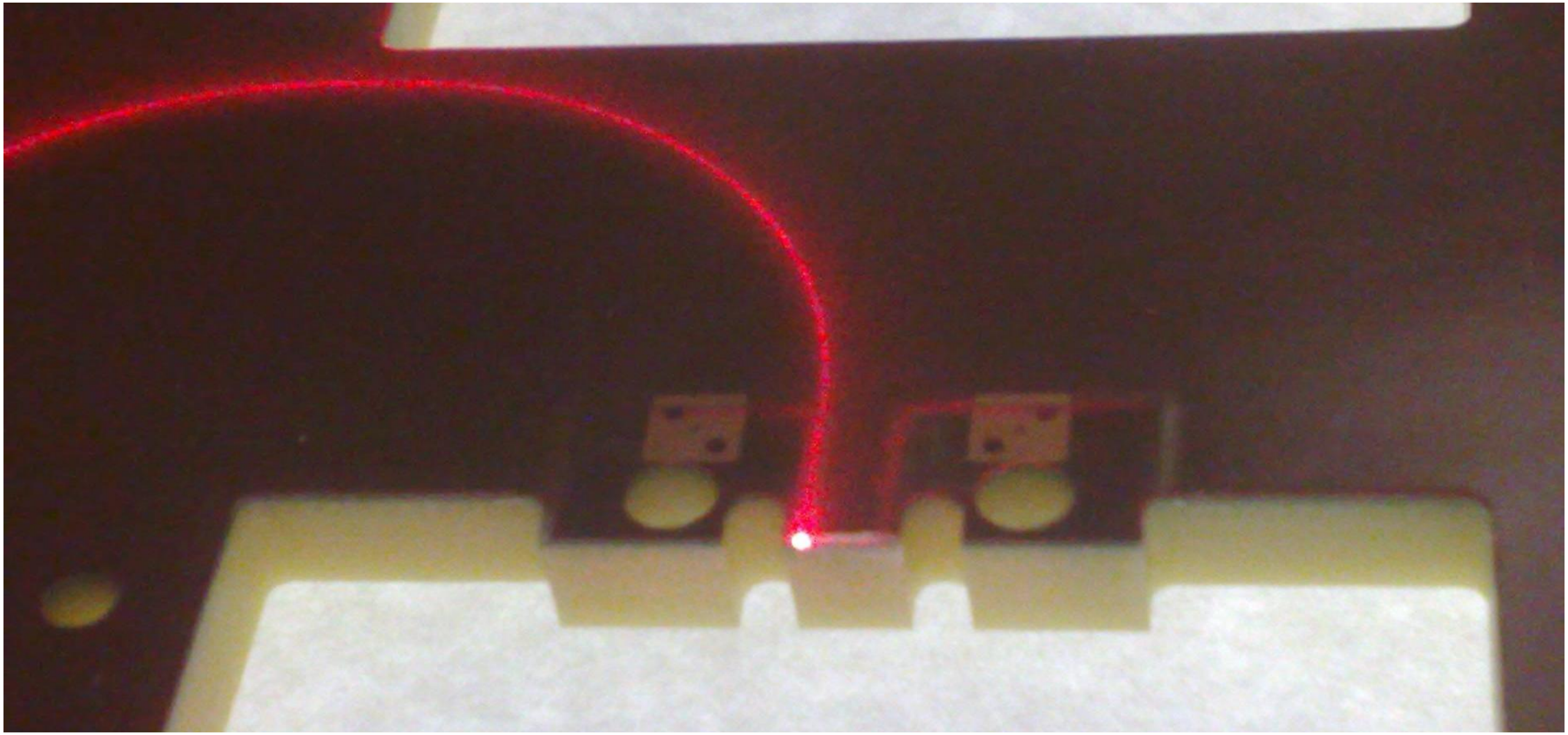
The Shortest Waveguide Illuminated by Red Laser



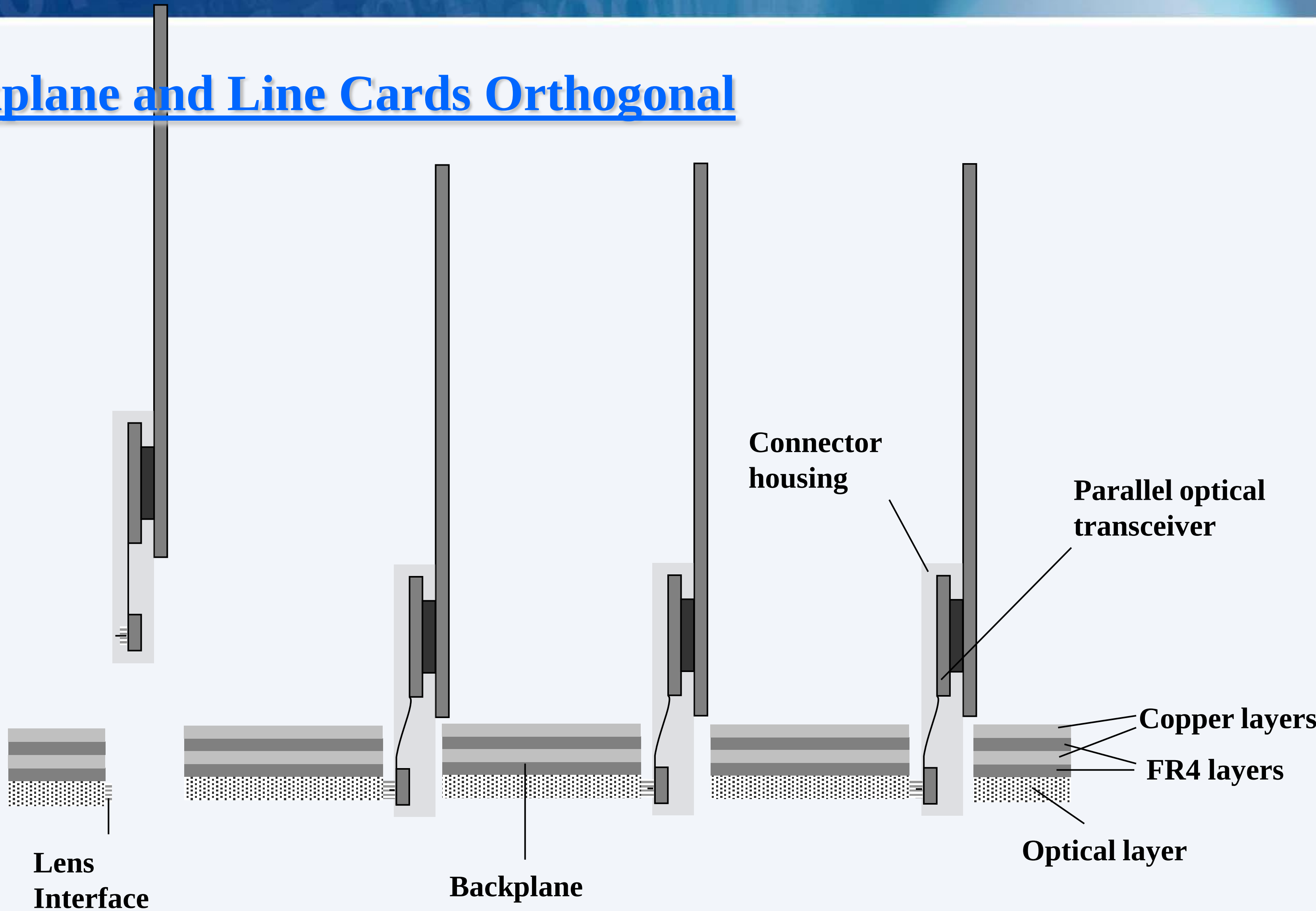
Waveguide with 2 Crossings Connected 1st to 3rd Linecard Interconnect



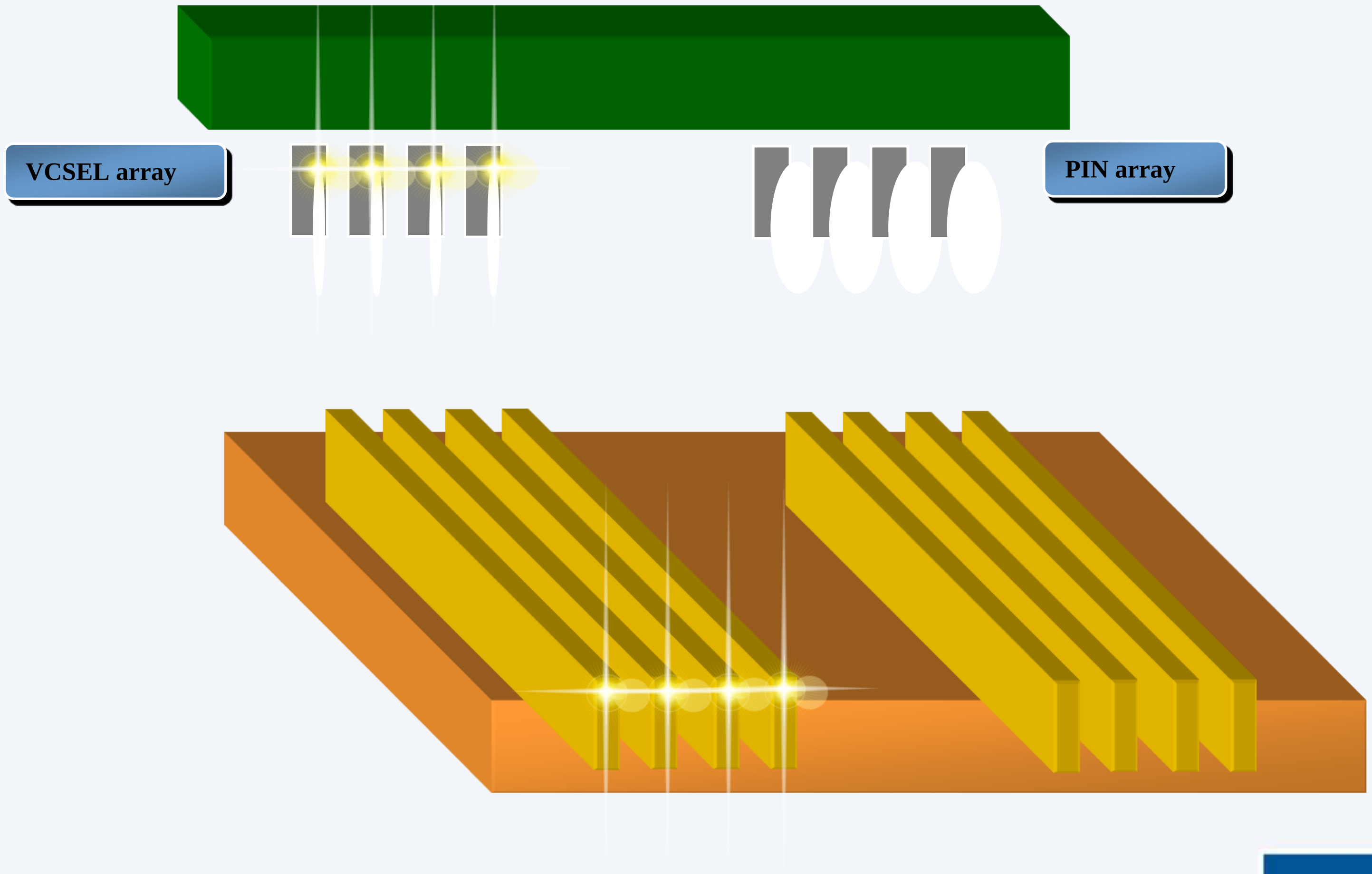
Output Facet of the Waveguide Interconnection

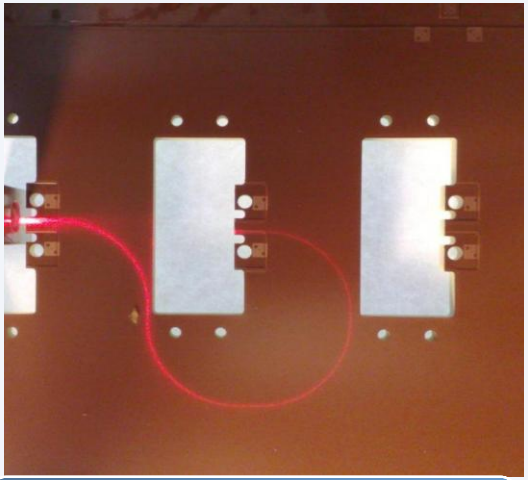


Backplane and Line Cards Orthogonal



Butt-coupled connection approach without 90º deflection optics

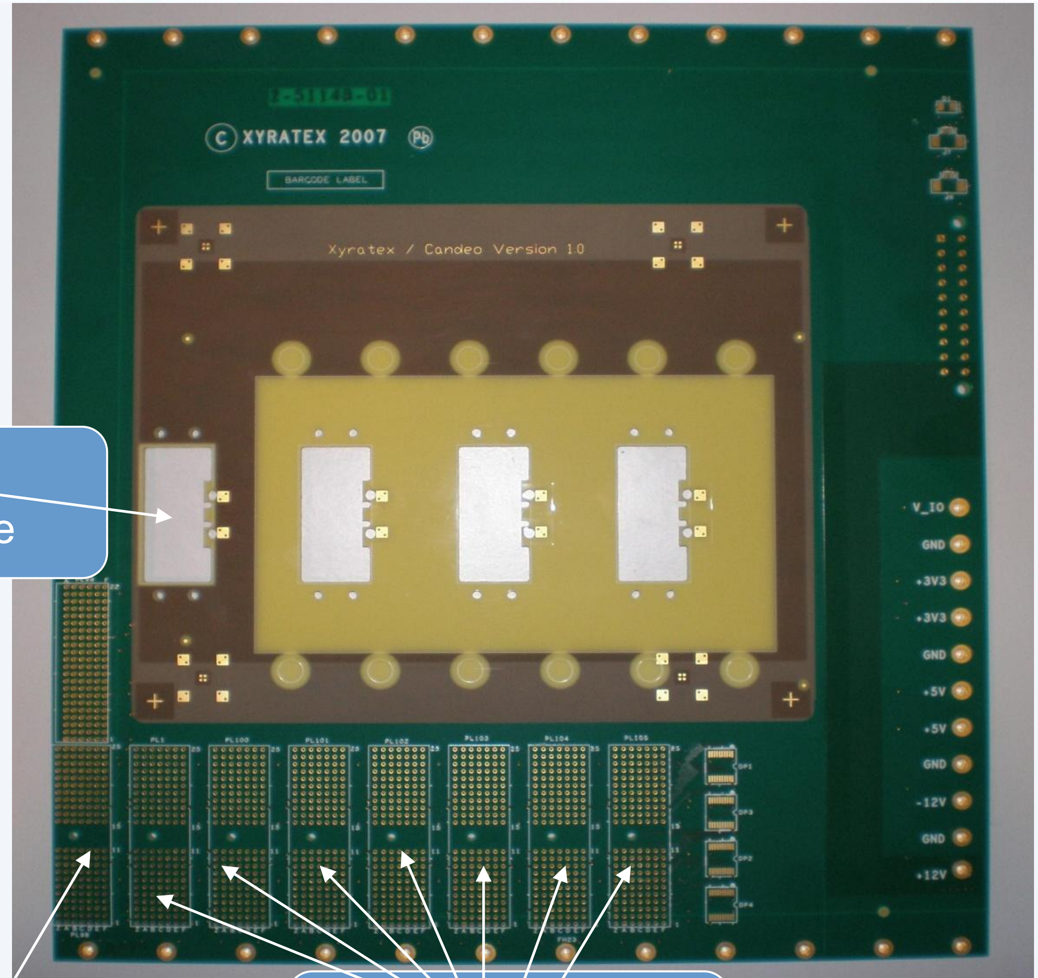




Waveguide illuminated through butt-coupled fibre connection

Hybrid Electro-Optical Printed Circuit Board

- ❑ Standard Compact PCI backplane architecture
- ❑ 12 electrical layers for power and C-PCI signal bus and peripheral connections
- ❑Electrical C-PCI connector slots for SBC and line cards
- ❑ 1 polymeric optical layer for high speed 10 GbE traffic
- ❑ 4 optical connector sites
- ❑ Dedicated point-to-point optical waveguide architecture



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ELECTRO-OPTICAL BACKPLANE

Hybrid Electro-Optical Printed Circuit Board

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- ❑ 12 electrical layers for power and C-PCI signal bus and peripheral connections
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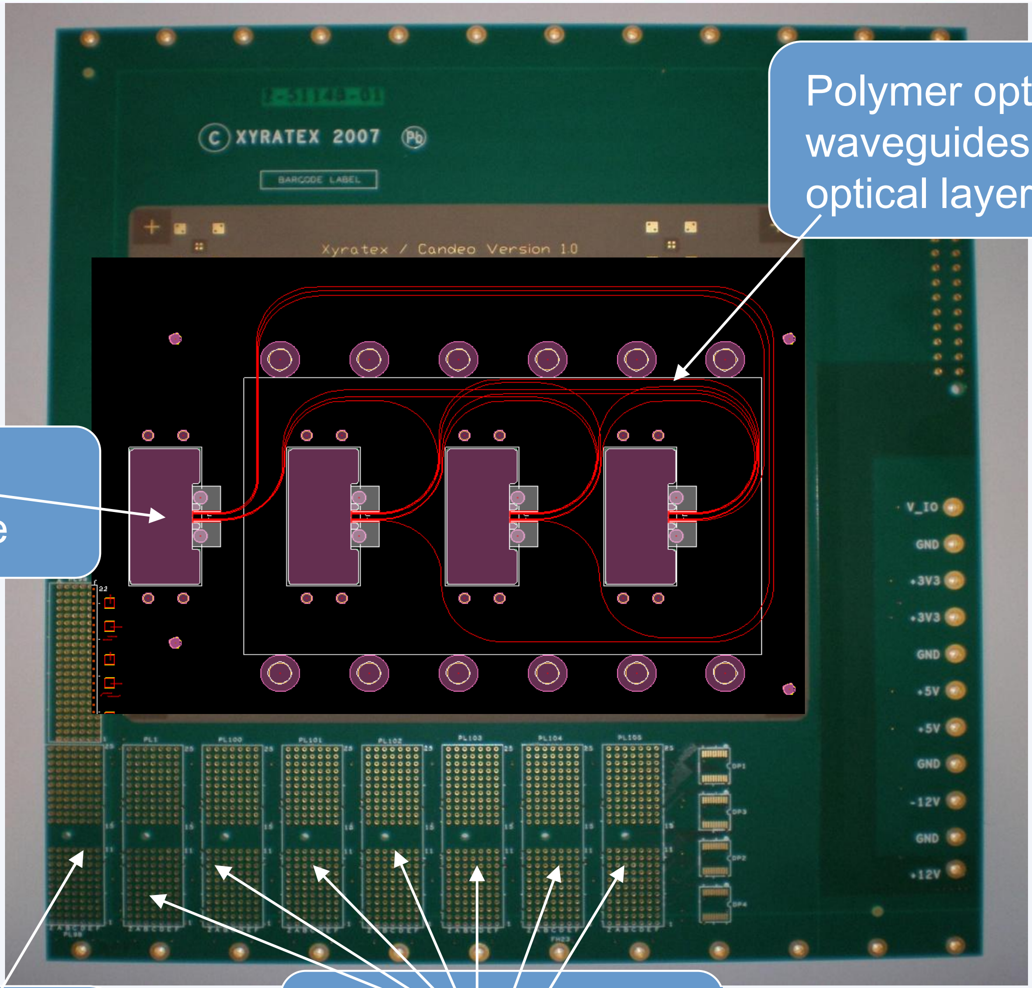


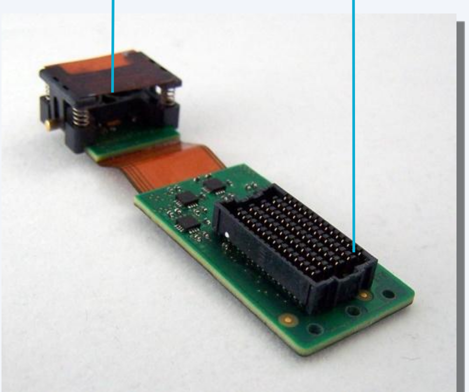
Parallel optical transceiver circuit

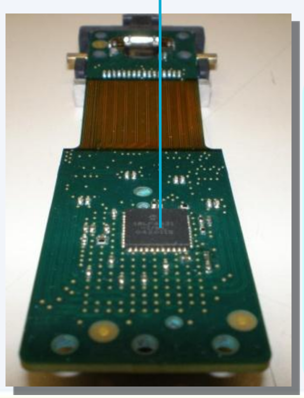
- ❑ Small form factor quad parallel optical transceiver
- ❑ Microcontroller supporting I^2C interface
- ❑ Samtec "*SEARAY™*" open pin field array connector
- ❑ Spring loaded platform for optical engagement mechanism
- ❑ Custom heatsink for photonic drivers

Spring loaded platform

Samtec field array connector

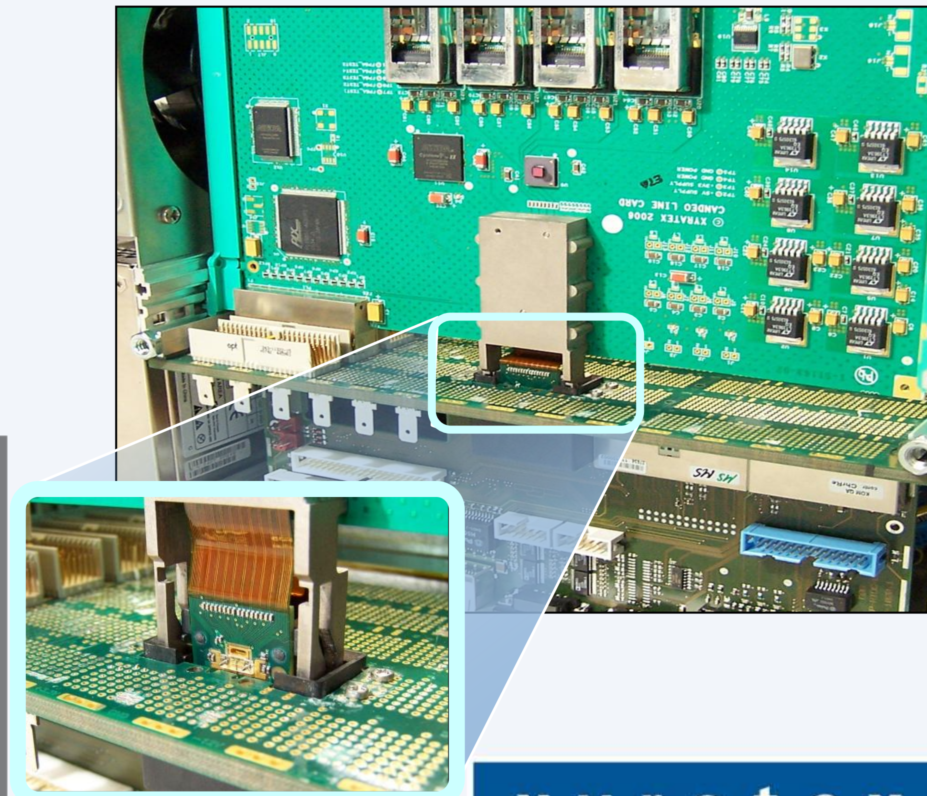
Microcontroller





Backplane connector module

- ❑ Samtec / Xyratex collaborate to develop optical PCB connector
- ❑ 1 stage insertion engagement mechanism developed
- ❑ Xyratex transceiver integrated into connector module



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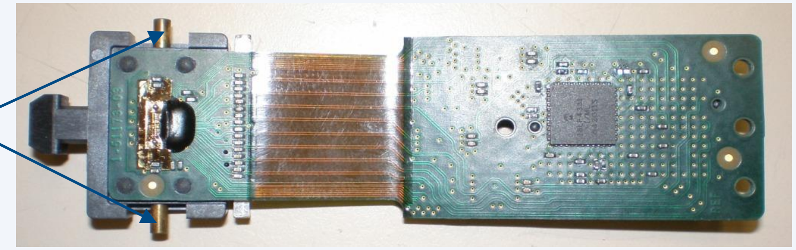
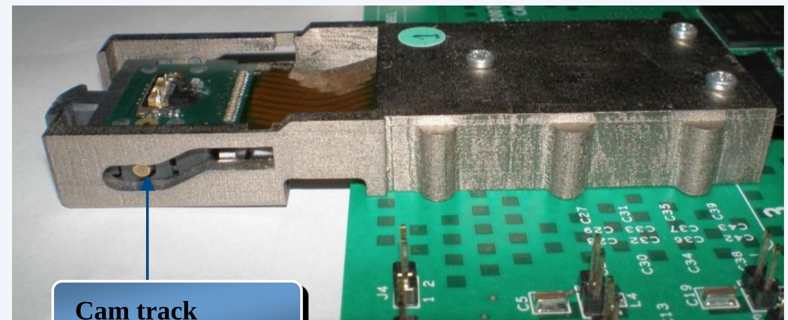
Engagement process

- Optical transceiver interface floats
- Backplane receptacle “funnels” connector
- Cam followers force optical interface up
- Optical transceiver lens butt-couples to backplane lens

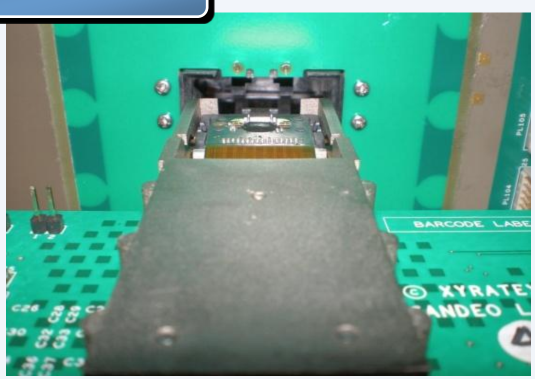
Cam followers



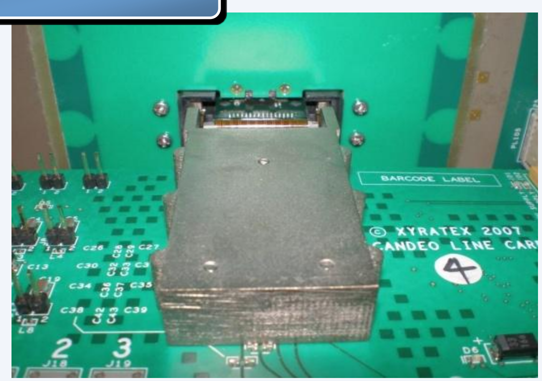


Cam track

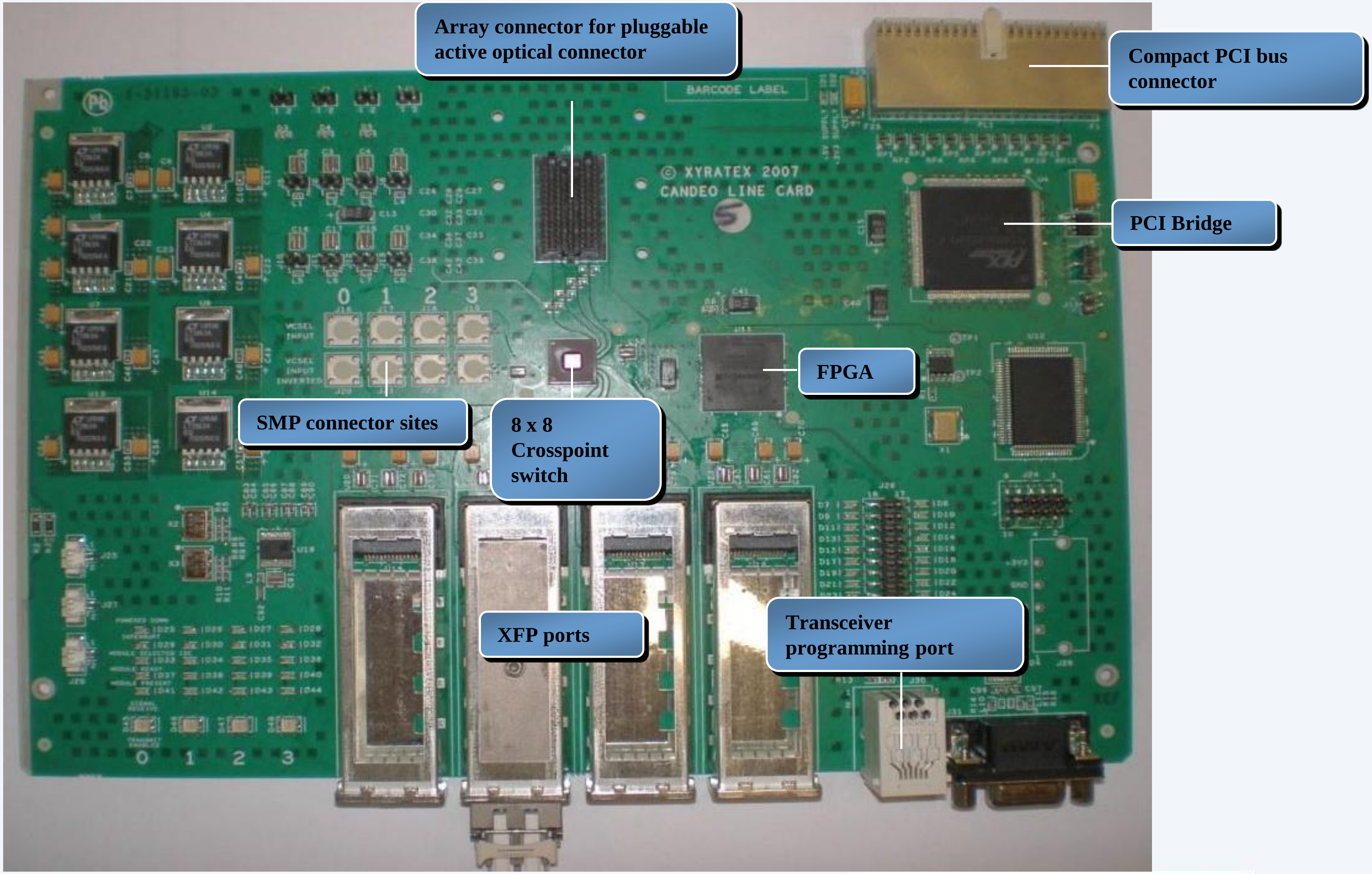
Undocked



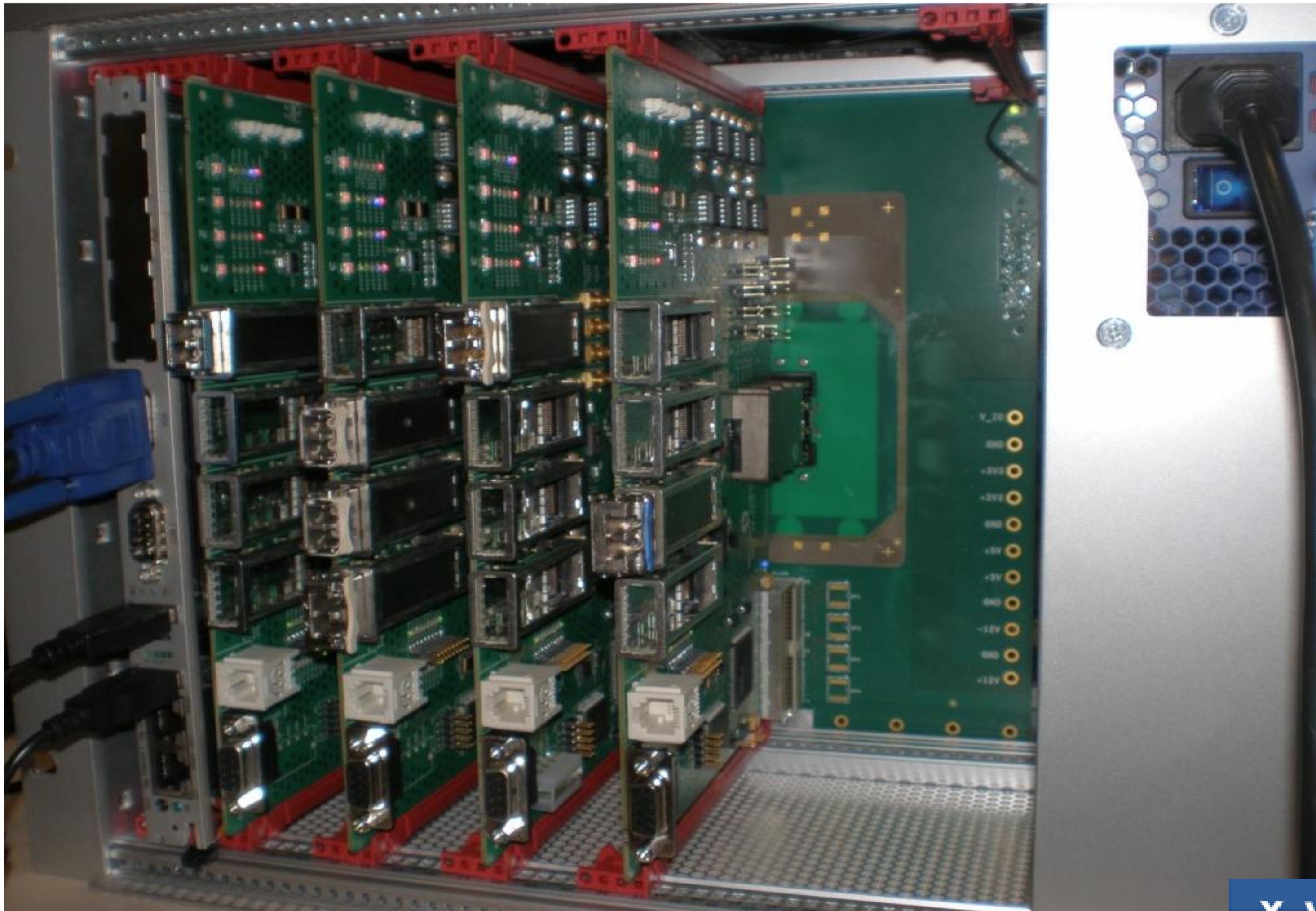
Docked



High Speed Switching Line Card



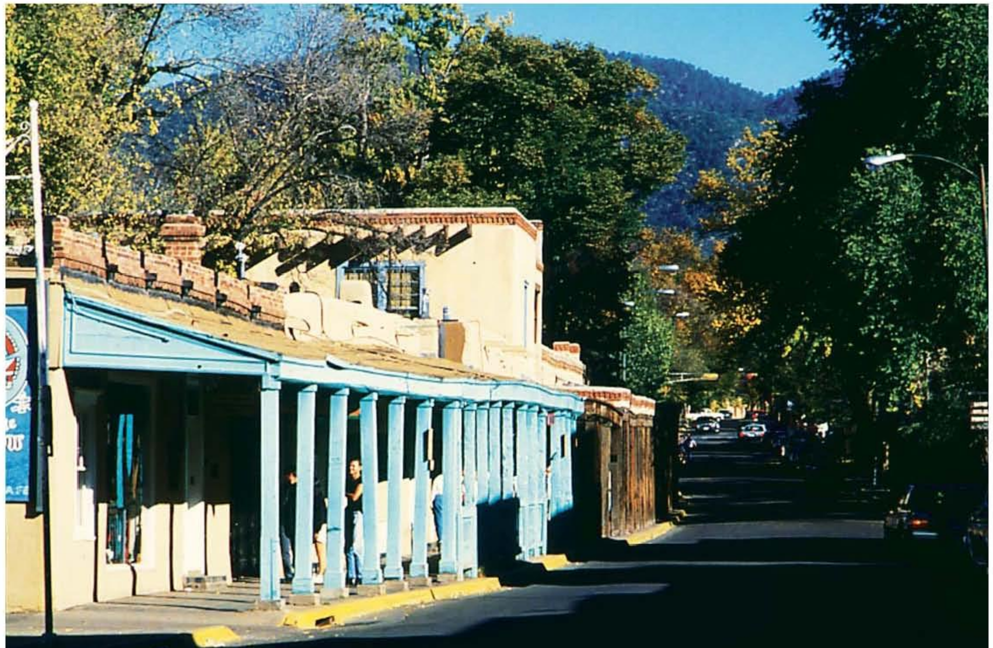
Demonstrator with Optical Interconnects



Demonstration Assembly

Acknowledgments

- **University College London, UK**
  - Kai Wang, Hadi Baghsiahi, F. Aníbal Fernández, Ioannis Papakonstantinou (now at Sharp Labs of Europe Ltd)
- **Loughborough University, UK**
  - David A. Hutt, Paul P. Conway, John Chappell, Shefiu S. Zakariyah
- **Heriot Watt University**
  - Andy C. Walker, Aongus McCarthy, Himanshu Suyal
- **BAE Systems, UK**
  - Henry White
- **Stevenage Circuits Ltd. (SCL), UK**
  - Dougal Stewart, Jonathan Calver, Jeremy Rygate, Steve Payne
- **Xyratex Technology Ltd., UK**
  - Dave Milward, Richard Pitwon, Ken Hopkins
- **Exxelis Ltd**
  - Navin Suyal and Habib Rehman
- **Cadence**
  - Gary Hinde
- **EPSRC and all partner companies for funding**



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20th Annual Workshop on Interconnections Within High Speed Digital Systems

3-6 May 2009

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