injection is reported here. The energy of electrons incident on the Si–SiO$_2$ interface at the moment of injection has a measurable effect on charge trapping and detrapping processes within the oxide. The trapped charge density decreases with increasing p-well bias. The proposed mechanism for this effect is the interaction of hot electrons injected into the conduction band of the SiO$_2$ with trapping sites previously formed in the oxide. The effect is significant in that it allows the possibility of the recovery of degraded devices by further electron injection at higher p-well biases, thus extending the operating lifetime of n-MOSFET devices.

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COMPUTER-GENERATED HOLOGRAM ETCHED IN GaAs FOR OPTICAL INTERCONNECTION OF VLSI CIRCUITS

C. D. Carey, D. R. Selviah, S. K. Lee, S. H. Song and J. E. Midwinter

Indexing terms: Semiconductor optoelectronics, Computer-generated holograms, Optical interconnections

By integrating, on a wafer plane, GaAs semiconductor optoelectronic modulators and detectors with computer-generated holograms between then, the potential for in-plane interconnections is proposed. We report the fabrication and characterisation of a binary-phase relief hologram etched in a GaAs wafer using an averaged Fresnel zone plate design to focus light to 2 × 2 spots for array interconnection. Efficiencies of 28% for this design of binary CGH etched in GaAs have been achieved, close to the theoretical maximum.

Recent developments in the configuration of optical interconnections for electronic circuits have included lens arrays, on-chip lasers, beam splitters and computer-generated hologram (CGH) elements. The use of CGH has certain advantages over other optical imaging methods in terms of ease of miniaturisation and compatibility with the lithographic device production process, and aberration-free imaging as well. We aim to develop a novel in-plane on-wafer interconnection using a mirror element above the surface of the wafer with the optoelectronic components and CGH integrated all on a wafer, as shown in Fig. 1. In most papers, the approach has

been to use one Fresnel zone plate (FZP) for each detector [1], so that an array of CGHs or FZPs are required. To keep the high packaging density of the modulators and detectors for this application, the whole hologram is designed as a single element.
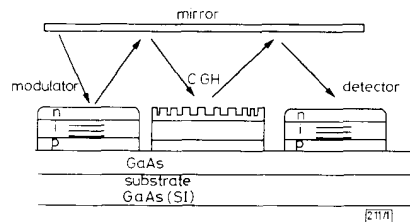

Fig. 1 *Schematic diagram of CGH optical interconnection between modulator/detector on wafer*

In this letter a GaAs wafer has been chosen for the CGH substrate to fully integrate and be compatible with GaAs electroabsorptive multiple-quantum-well (MQW) modulators which show a high contrast ratio in this region [2]. As part of the system shown in Fig. 1, a CGH was designed to focus an incident plane wave to four spots spaced on a spot separation of 62·5 μm in a 2 × 2 spot array format. The design wavelength of IR light at $\lambda = 848$ nm was chosen to match the GaAs optoelectronic components, but the experimental measurements reported were carried out at 633 nm.

A method of 'averaged Fresnel zone plates' was adopted to create the binary-phase Fresnel hologram [3]. The binary-phase FZP hologram was designed by calculating the phase difference between spherical wavefronts from four point sources and the plane wavefront at each point on the hologram plane [4]. Once the phase difference had been calculated and summed for each point, then a threshold value was used to assign either zero or π phase shift. The equation used to calculate the phase of the hologram is as follows:

$$\phi_R = \tan^{-1}$$
$$\times \left\{ \frac{\displaystyle\sum_{i=1}^{4} \sin\left\{ \left[\frac{2\pi}{\lambda} (\sqrt{[(x_i'-x)^2 + (y_i'-y)^2 + z_0^2]} - z_0) \right] + \phi_i \right\}}{\displaystyle\sum_{i=1}^{4} \cos\left\{ \left[\frac{2\pi}{\lambda} (\sqrt{[(x_i'-x)^2 + (y_i'-y)^2 + z_0^2]} - z_0) \right] + \phi_i \right\}} \right\}$$

(1)

where ϕ_R is the phase difference and x_i' and y_i' are the co-ordinates of the ith point source, x, y are the co-ordinates on the hologram, and ϕ_i is the initial phase of the ith point source. For simplicity $\phi_i = 0$.

Fig. 2 shows the binary-phase distribution plotted out on paper with black representing π phase change and white zero phase change. An e-beam mask was written directly from the binary data. Using a lithographic process the hologram mask
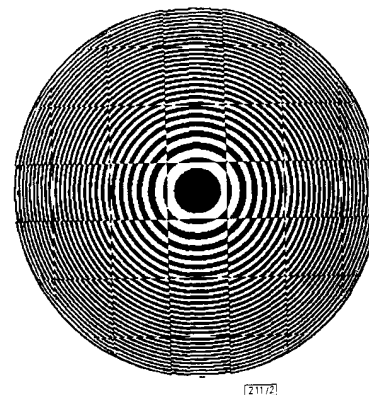

Fig. 2 *Plot of computer-generated hologram*

was copied and then etched on to the GaAs wafer. Both dry and wet etching techniques were successful but only plasma-etched samples were used in the experiments described. This enabled the binary-phase relief hologram to be formed on the surface, and this was then metallised with approximately 20 nm of gold to increase the reflectivity. We fabricated five different depth samples ($\lambda/4$ = 166, 175, 185, 220, 225 nm), all with a diameter of 2·1 mm.
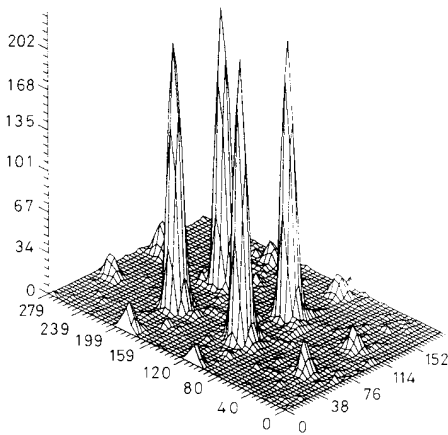

Fig. 3 *Intensity profile plot of focal spots in image plane*

The intensity profile plot of the focal spots was obtained by using a frame grabber to store the image plane from a CCD camera, with the hologram illuminated at normal incidence (Fig. 3). The results of the experimental sample ($\lambda/4$ = 166 nm) and design values ($\lambda/4$ = 158 nm) are presented in Table 1. The efficiency was measured by recording the maximum intensity of the four spots (62·5 μm separation) through a 150 μm pin hole in front of a power meter. The total intensity was measured by positioning a mirror in place of the CGH and measuring the intensity of a 2 mm-diameter spot of light on the detector. The ratio of the 4-spot intensity (± 1 order) and the total intensity from the mirror was used to evaluate the efficiency. The best experimental efficiency was measured to be 28% with an experimental measurement error of 6%, and this result is discussed later. To calibrate the measuring system a USAF-1951 standard resolution target was imaged and the pixel size and tolerance calculated. From these data the uniformity was calculated using $(I_a - \Delta I_{max})/I_a$, where I_a is the average peak intensity and ΔI_{max} is the change in peak intensity. This result (98%), together with the intensity plot in Fig. 3, shows very uniform spot array intensity. The spot separation (60·6 $\pm$ 3 μm) was measured by counting the number of pixels between peak spot values and calculating the dimension. The signal/noise ratio (SNR) of 24 dB was found by taking the ratio of the maximum spot intensity to the average noise level. The focal length and spot diameter were measured to be 35 mm $\pm$ 1 mm and 28·5 μm $\pm$ 3 μm, respectively, both

of which are larger than the design values. This is consistent with the basic focal relationship, with an increase in focal length giving an increase in spot size.

The averaged FZP hologram element can be considered to be a superposition of diffraction gratings in x and y and a Fresnel zone plate, as can be seen in Fig. 2. The zone plate focuses the light to a spot, while the two diffraction gratings in x and y diffract the focal spot to four points at the ± 1 order position in both x and y. The overall efficiency of the averaged Fresnel zone plate lens is given by

$$\eta_T = (2\eta_1)(2\eta_2)(\eta_3) \cos^2(\Delta\phi/2) \qquad (2)$$

and is the product of the efficiency of the diffraction grating elements in x and y (η_1 and η_2) and the zone plate efficiency η_3. The cosine term represents the change in efficiency with variation in grating depth ($\lambda/4$) [5]. The efficiency of each diffraction grating element contains the $+1$ order and -1 order terms, so $2\eta_1$ is required and $\eta_1 = 40·5\%$, which is derived from a sinc function [1]. The zone plate term η_3 also has a maximum efficiency of 40·5%. The maximum theoretical value of the efficiency for this design is 26·6%. Fig. 4 shows a plot of efficiency against phase difference for theoretical values (eqn. 2) and five experimental plots of different quarter-wavelength depth samples. The experimental results match closely the theoretical values, and the measured efficiency, 28%, of the 166 nm sample is close to the maximum theoretical limit of 26·6%.
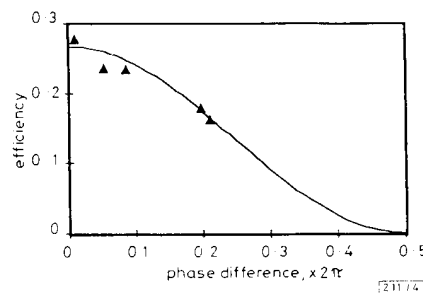

Fig. 4 *Plot of efficiency against phase difference*

In conclusion, we have fabricated averaged FZP binary holograms on a GaAs wafer to focus incident light to a 2 × 2 spot array. The diffraction efficiency (28%) is close to the theoretical maximum, and small spot separations (62 μm), along with high uniformity (98%), have been obtained. With these results we have proposed a method for integrating optical interconnection elements and optoelectronic device arrays on a single GaAs wafer. To implement practical interconnection set-ups it will be necessary to improve the efficiency, increase the number of spot arrays and fabricate off-axis designs. To implement these improvements it is necessary to fabricate multilevel-phase holograms and design elliptical zone plate patterns for off-axis operation.

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Table 1 RESULTS SHOWING EXPERIMENTAL AND DESIGN VALUES

	Experimental values	Design values
Efficiency η, %	28 ± 3	26·63
Uniformity, %	98	100
Spot diameter (full width), μm	28·5 ± 3	24·6
Focus, mm	35 ± 1	33·5
SNR, dB	24	—
Depth ($\lambda/4$) (λ = 633 nm), nm	161·1	158·25
Dia. of HOE, mm	2·1	2·1
Spot separation, μm	60·6 ± 3	62·5

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TWO-DIMENSIONAL OPTICAL AND/OR LOGIC OPERATIONS USING AN OPTOELECTRONIC INTEGRATED FUNCTIONAL DEVICE (OFD) ARRAY

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Indexing terms: Optoelectronic integrated circuits, Optical feedback

An optical logic device based on a *PNPN*-type optoelectronic integrated functional device (OFD) is demonstrated. This device has a reflection-type structure and the ability of long to short wavelength conversion. Two-dimensional optical AND/OR logic operation using a 16 × 16 OFD array is also shown.

Introduction: *PNPN*-type light-emitting thyristors have been studied [1–4] as optoelectronic switches and as two-dimensional optical logic gates for optical computing and parallel image processing. Light-emitting thyristors have several advantages for optical information processing compared with other devices [5, 6], i.e. high on/off ratio, simplicity of structure, compatibility to electronic circuits and high-speed operation. Cascadability to other optical logic gates requires that the wavelength of the input beam to the gate is equal to or shorter than that of the output beam. The thermal stability of the reflection-type gate is superior to that of the transmission-type gate, and it may be mounted on a heat sink.

We have studied an optical logic device based on the *PNPN*-type optoelectronic integrated functional device (OFD) with a reflection-type structure. This device also has the ability of a long-to-short-wavelength conversion. Two-dimensional optical AND/OR logic operation was achieved using a 16 × 16 OFD array.

Principle of operation: The OFD consists of a light-emitting diode and a phototransistor with internal optical feedback from the light-emitting diode to the phototransistor. They are stacked on a substrate alternately. The most important benefit of this device is that the two parts are independently constructed, in contrast with other *PNPN*-type devices [2, 3]. Therefore the device parameters of each part can be optimised independently. Fig. 1 shows the structure and the equivalent circuit of the OFD. Incident light on the OFD reaches through the light-emitting diode to the phototransistor. The bandgap of the active layer of the light-emitting diode is wider than that of the collector and the base layer of the photo-transistor, so that the wavelength of the output light is shorter than the longest wavelength detectable to the phototransistor. Therefore, the optical feedback from the light-emitting diode to the phototransistor appears due to the absorption of emitted light in the phototransistor. This device can also be used as a long-to-short-wavelength convertor. Because of this feedback, the OFD shows light input/output characteristics with a threshold. When the intensity of the light input to the OFD exceeds the threshold value, the light output increases from the OFF-state to the ON-state sustained without light input, due to the optical feedback. When both the light inputs have an intensity above the threshold, the device operates as an optical OR gate. On the other hand, when neither intensity of the two inputs exceeds the threshold and the sum of the two does, the device operates as an optical AND gate.

Experimental results: The OFD array is grown on n-type GaAs substrate using metal organic chemical vapour deposition as follows: an n-GaAs buffer layer ($1.0\,\mu m$, $1 \times 10^{18}\,cm^{-3}$), an $n\text{-Al}_{0.4}\text{Ga}_{0.6}\text{As}$ emitter layer ($1.0\,\mu m$, $1 \times 10^{17}\ cm^{-3}$) a GaAs spacing layer ($0.05\,\mu m$, $5 \times 10^{14}\,cm^{-3}$), a p-GaAs base layer ($0.1\,\mu m$, $3 \times 10^{14}\,cm^{-3}$), an n-GaAs collector layer ($1.0\,\mu m$, $3 \times 10^{15}\,cm^{-3}$), an $n\text{-Al}_{0.4}\text{Ga}_{0.6}\text{As}$ cladding layer ($1.0\,\mu m$, $2 \times 10^{17}\,cm^{-3}$), an $n\text{-Al}_{0.4}\text{Ga}_{0.6}\text{As}$ active layer ($0.2\,\mu m$, $8 \times 10^{16}\,cm^{-3}$) a $p\text{-Al}_{0.4}\text{Ga}_{0.6}\text{As}$ cladding layer ($1.0\,\mu m$, $1 \times 10^{19}\,cm^{-3}$), and a p-GaAs contact layer ($0.2\,\mu m$, $1 \times 10^{19}\,cm^{-3}$). A $130\,\mu m \times 130\,\mu m$ mesa structure is made by conventional wet etching. AuZu/Au metal is used as the contact on the p-GaAs contact layer. The n-type contact of AuGe/Ni/Au metal is used on the back side of the wafer. The light input/output window opens on reaching the p-cladding layer, which is $60\,\mu m$ in size, and the distance between the adjacent devices is $30\,\mu m$. The 16×16 OFD array size is about $2.7\,mm \times 2.7\,mm$ including bonding pads.
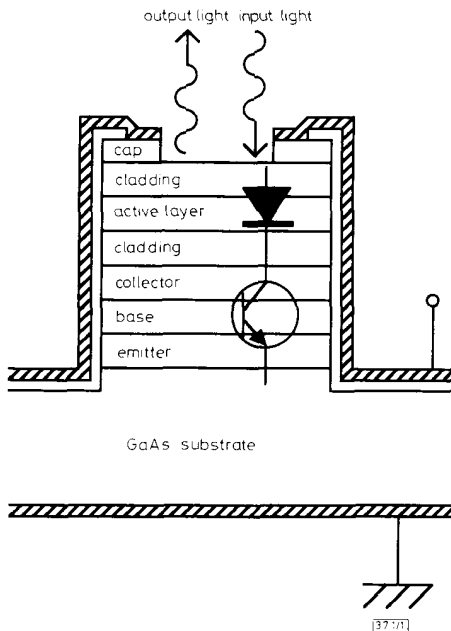

Fig. 1 *Schematic cross-section and equivalent circuit of OFD device*

The single-element OFD typically represents 745 nm peak wavelength of the light output, a break-over voltage of 5·5 V and a holding current of $150\,\mu A$. Here, the break-over voltage is defined as the maximum voltage which holds the device in the OFF-state, and the holding current as the minimum current which holds the device in the ON-state. When each element of the OFD array is irradiated individually, the standard deviation of the light input to turn on each device is about 6% subject to the condition that the applied voltage and the load resistance are fixed. While all the elements of the OFD array are irradiated simultaneously, the average holding current of an OFD element is about $660\,\mu A$, which is about four times larger than that irradiated individually. This is because of the nonuniformity of the current supplied from the bonding pads through the p-type contact metal to each element of the OFD array, i.e. the current flows easily through the OFD in the peripheral area near the bonding pads, but it does not flow easily through the OFD in the centre of an array far from the pads, since the resistance of the p-type contact metal connecting each device increases with the distance from the pads. As a result, the average holding current for each element of the OFD array is nominally increased.

Fig. 2 shows the optical system set-up used to perform optical logic. The incident beams from two laser diodes are collimated with a lens, pass through a mask (SM1, SM2),