A 32-by-32 CMOS Microelectrode Array for Capacitive Biosensing and Impedance Spectroscopy

Virgilio Valente and Andreas Demosthenous
Department of Electronic and Electrical Engineering,
University College London, WC1E 7JE, London, United Kingdom.
Contact Email: v.valente@ucl.ac.uk

***Abstract*—This paper presents the design of a 1024-channel dual-modality CMOS biosensor suitable for both capacitive sensing and impedance spectroscopy. The chip serves as a platform for detection, localization and monitoring of bacteria and can can be adopted for affinity-based assays. The chip features a 32x32 array of unpassivated metal electrodes formed on the top metal of a 0.18μm CMOS process, with an overall sensing area of 2.06 mm^2. The system design is based on a shared in-pixel integrator that can be used as a charge amplifier for capacitive sensing or as part of a transimpedance amplifier for impedance spectroscopy. The CS mode is capable of a operation bandwidth of 50 MHz at a current consumption of 82 μA per pixel. The EIS channel operates over a bandwidth between 100 Hz and 1 MHz with a total input-referred current noise of 48 pA$_{RMS}$ and a current consumption of 210 μA per channel .**

I. Introduction

Lab-on-chip devices have gained widespread interest in electrochemical and biomedical research as a tool to study the electrical and physical properties of biological interfaces and provide valuable diagnostic information about potential pathological condition of biological cells, tissues and organs.
Integrated impedance biosensors represent the latest trend in the development of label-free and cost-effective diagnostic devices with remarkable sensitivity to bacterial cells towards single-cell detection [1]. These types of sensors combine arrays of hundreds or thousands of microelectrodes formed in the top metal layer of a CMOS process, thus enabling the realiisation of miniaturized, high-throughput and portable point-of-care diagnostic tools.
Among the preferred sensing methods, capacitive sensing (CS) has been extensively adopted to detect and image micro and nanoparticles, cell localization and bacteria growth monitoring [2]–[4]. CS operates by measuring the changes in permittivity in the solution at frequencies at which the cell acts predominantly as a capacitor. Electrical impedance spectroscopy can be used as a complementary approach to CS, but also extended to affinity-based assays where changes in cell impedance are related to the presence of target analytes, including enzymes, antibodies and DNA [5]–[7].
The main benefit of EIS stems from its non-invasive and non-destructive nature, based on the application of small voltage or currents to the biological environment, which have very little impact on the measured properties. EIS systems can now provide simultaneous analysis of several biological parameters by combining on-chip electrode arrays and different sensing modalities on the same chip.
This paper presents the design of a 1024-channel dual-modality impedance biosensor, suitable for both high-frequency capacitive sensing and impedance spectroscopy. The system adopts an in-pixel integrating amplifier that can be used both as a charge amplifier in CS modality or as part of a transimpedance amplifier in EIS modality. The next sections will provide details on the design of the system with simulated operation and summary of performance.

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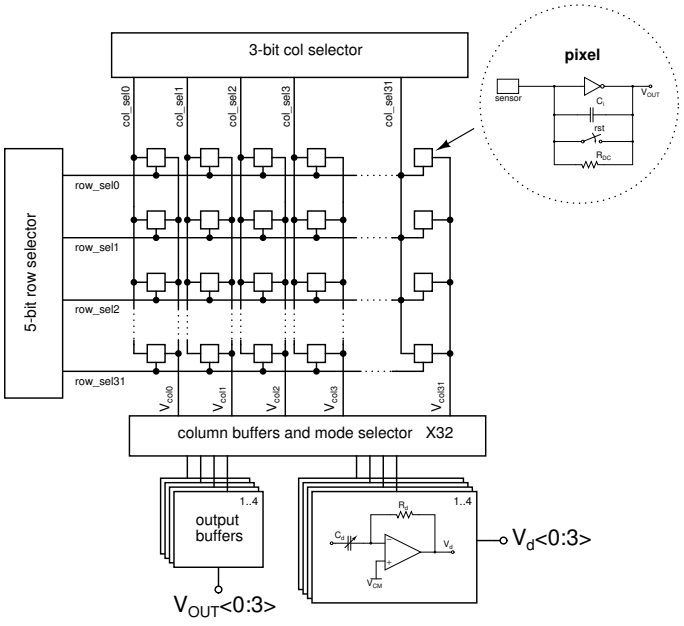

Fig. 1: ASIC architecture.

II. System Architecture

The architecture of the CMOS MEA sensor chip is shown in Fig. 1. The chip comprises an array of 1024 active pixels, consisting of a set of planar electrodes and a charge amplifier, shown in the inset of Fig. 1. Four pixels can be addressed concurrently using a 5-bit row decoder and a 3-bit column decoder. Each column has a dedicated column buffer and a sampler. The output of the column buffer, $V_{\mathrm{col}i}$, can be either connected to a set of 4 output buffers (in CS mode) or to 4 differentiators and programmable gain amplifiers (in EIS mode).
The chip can be operated by a microcontroller thanks to the on-chip serial-to-peripheral interface (SPI) using only 3 lines. The SPI consists of 2 16-bit registers that control the chip enable signals, differentiator gain and PGA gain. The analog

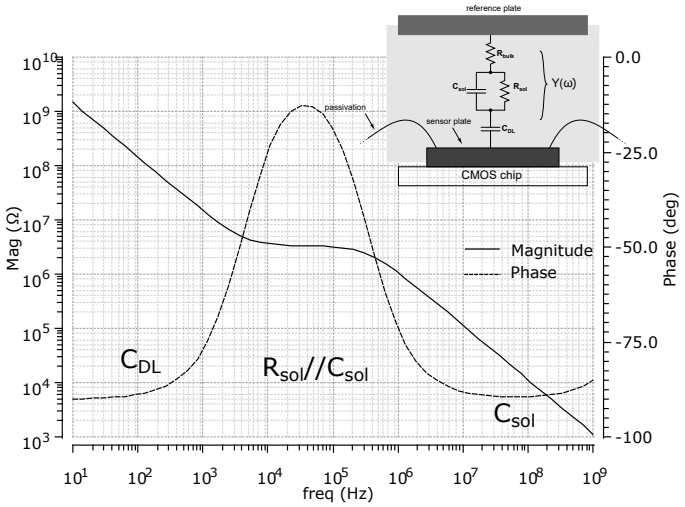

Fig. 2: Electrode cell model.

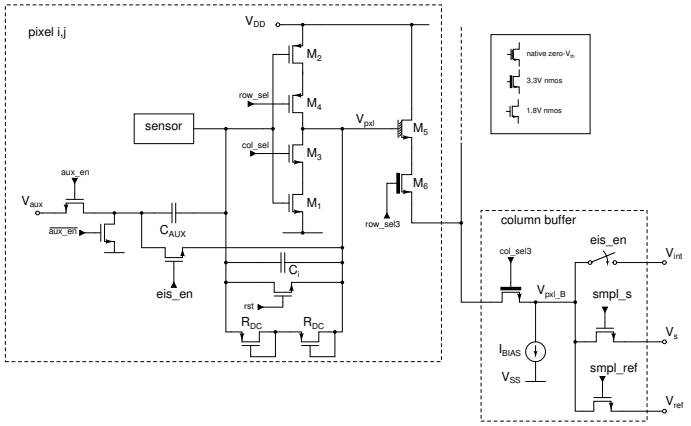

Fig. 3: Schematic of a pixel and column buffer.

output of each channel is buffered internally and available at pinout.

The specifications of the design are based on a simplified model of the cell behaviour reported in the inset of Figure 2. The model consists of a capacitor formed by a reference plate and a sensor plate, and a frequency-dependent complex impedance that represents the double-layer capacitance, C_{DL} between the sensor plate and the solution, a parallel combination of the solution resistance, R_{sol} and capacitance, C_{sol}, in series with the bulk resistance, R_{bulk}. Three main regions can be identified by plotting the impedance magnitude and phase of the cell model. At low frequencies the impedance is dominated by C_{DL}. In the frequency mid-range, the impedance is mainly represented byR_{sol} with the phase approaching 0°. At frequencies higher than the solution cutoff frequency of $(2\pi R_{\mathrm{sol}} \cdot C_{\mathrm{sol}})^{-1}$, the solution is predominantly capacitive.

A. Pixel Circuit

The in-pixel circuitry consists of an inverter-based integrator architecture [2]. The pixel circuit differs from conventional charge-based amplifiers in that it can be used for both capacitive sensing, and as the first stage of a integrator-differentiator TIA to perform impedance spectroscopy. Transistor M_1 and M_2 form a class-AB inverting amplifier. The cascode transistors M_3 and M_4 serve to increase the amplifier open-loop gain as well as switches to address individual pixel. The integrator capacitor C_{i} is implemented as an interdigitated structure in a single metal layer with a nominal extracted capacitance of 57 fF and a parasitic capacitance of 13 fF.

In order to extend the output dynamic range an auxiliary capacitor, C_{aux} of 100fF is used in both CS and EIS modes. A silicon capacitor was used in order to maximize the capacitance to area ratio. In CS mode a small offset charge, proportional to the applied voltage, V_{aux} is removed from the output node, reducing the output voltage below the nominal inverter threshold, prior to applying an excitation voltage, V_{EXT} to the reference plate [2]. Is EIS mode, the auxiliary capacitor is connected in parallel to C_{i}, thus reducing the integrator gain and avoiding saturation of the amplifier when operated at lower frequencies. A feedback resistor is included to provide a dc current path during EIS operation. The resistor is implemented by 2 mos pseudoresistors in series with a simulated equivalent resistance of 1 TΩ. The integrator output is buffered by a column line driver formed by a zero-$\mathrm{V_{TH}}$ native transistor, M_5, two 3.3V switches, M_{6-7} and a 20 μA bias current, I_{BIAS}. The native transistor was chosen in order to obtain a wide dynamic range between 0.3V (overdrive of the bias current) and 1.5V (buffer saturation). The use of 3.3V switches ensures correct operation when the source voltage of M_5 is large and the V_{GS} of the switches is reduced.

The sensor dimensions are defined by un unpassivated area measuring 15μm by 15μm. This size was chosen as the smaller possible region of unpassivated top metal (AlCu of thickness of 880 nm) according to the foundry's design guidelines. The extracted parasitic capacitance of the sensor is in the order of 3.7 fF.

In EIS mode, the in-pixel integrator represents the first stage of an integrator-differentiator TIA, as shown in Figure 4. The TIA transfer function is given by:

$$H(s) = \frac{R_{DC} R_d C_d s^2}{(R_{DC} C_i s + 1)(R_d C_{FB} s + 1)}, \qquad (1)$$

where R_{d} and C_{d} are the differentiator resistor and capacitor and C_{FB} is the differentiator feedback capacitor (100 fF) that ensures stability. The differentiator is implemented by a folded-cascode opamp in order to accommodate the high input voltage range supplied by the integrator and provide large open-loop gain. The simulated open-loop gain of the differentiator opamp is 83dB with a bandwidth of 28 MHz and a phase margin of 65°. The simulated thermal noise floor of the opamp is 18 nV/$\sqrt{\mathrm{Hz}}$. The differentiator resistor is set to 1 MΩ and the differentiator capacitor is implemented in a 3-bit programmable array (control signal b) with capacitance range between 500 fF and 4 pF.

The simulated frequency response of the integrator and the TIA is shown in Figure 5. The TIA achieves a mid-band programmable gain between 130dB and 150dB. The low cutoff frequency, f_{L} is 10 Hz, while the high-frequency cutoff, f_{H} is slightly affected by the parasitics of the gain setting capacitors and has a nominal value of 1.6 MHz. The operation of the TIA

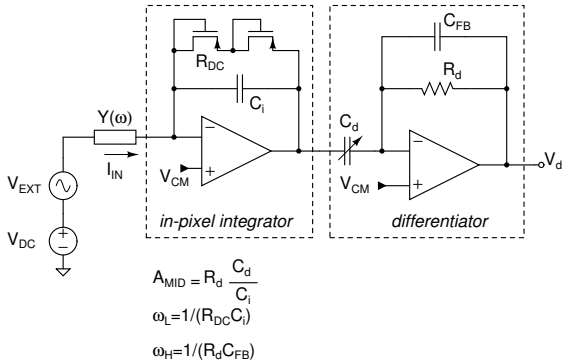

Fig. 4: Implementation of a TIA based on an integrator-differentiator structure.

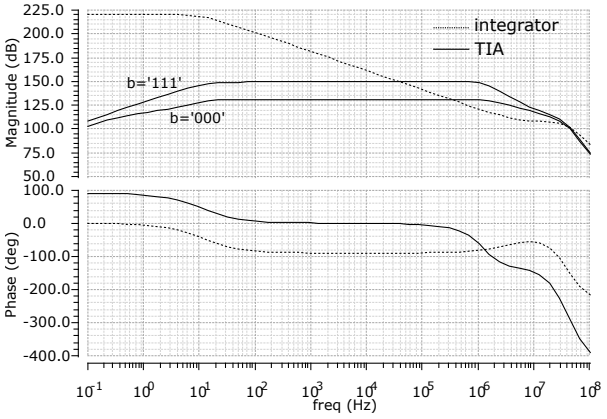

Fig. 5: Simulated in-pixel integrator and TIA gain.

at low frequency is limited by the large gain of the integrator, which exceeds 200dB at frequencies below 100 Hz.

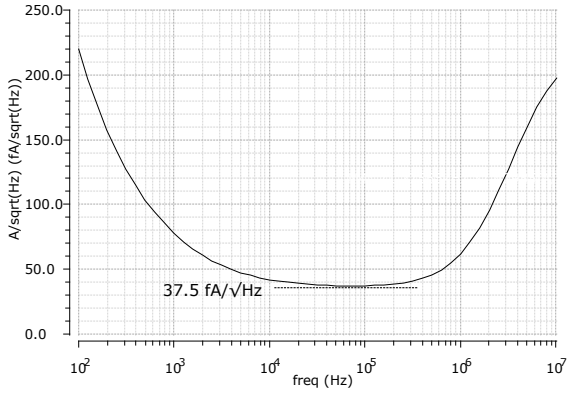

Fig. 6: Simulated input referred TIA noise.

The TIA noise was simulated in a bandwidth between 100 Hz and 10 MHz. Figure 6 shows the TIA total input-referred current noise. The simulated TIA thermal noise is 38 fA/$\sqrt{\text{Hz}}$ and the total integrated r.m.s noise over a bandwidth between 100 Hz and 1 MHz is 48 pA_{RMS}. This corresponds to approximately 316 pA_{pp}. Assuming an excitation voltage, V_{EXT}, of 10 mV_{pp} applied to the reference plate, this system has the potential to resolve admittances, $Y(\omega)$, as low as 32 nS.

TABLE I: Summary of Simulated Performance.

PARAMETER	UNITS	VALUE
Technology	-	0.18μm CMOS
Number of pads	-	64
Chip area (incl.pads)	mm^2	10
Supply voltage	V	1.8
Pixel array		
Number of pixels	-	1024
Sensor area	μm^2	15x15
Pixel area	μm^2	45x45
Fill ratio	-	11%
Sensing area	mm^2	1.46x1.41
CS		
Channels		4
Bandwidth	MHz	50
DR	V	0.3 - 1.5
Current consumption/channel	μA	82
EIS		
Channels		4
TIA Gain	MΩ	3.5 - 29
PGA 1 Gain	V/V	1 to 8
PGA 2 Gain	V/V	1, 10, 100
TIA integrated noise 100Hz-1MHz	pA_{RMS}	48
TIA thermal noise	$\text{fA/Hz}^{1/2}$	38
Current consumption/channel (at 10 kHz)	μA	210

III. Chip Operation

The chip was designed in a 0.18μm 6-metal CMOS technology. It consists of 64 pads for a total area of 3.154-by-3.154 mm^2. The chip layout is shown in Fig. 7 along with the layout of a pixel in the inset of the figure. The performance of the chip was simulated in Cadence Spectre. The key performance parameters are summarized in Table I.

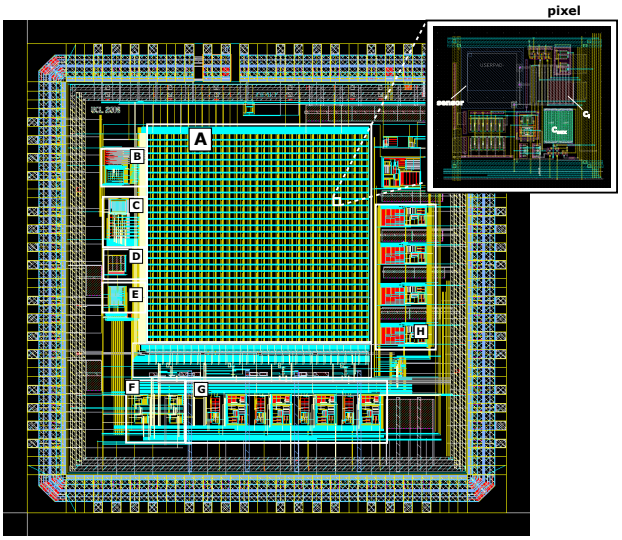

Fig. 7: Chip layout. **A**. Pixel array. **B**. Row decoder. **C**. Column decoder. **D**. POR. **E** SPI. **F**. Output buffers. **G**. Differentiators. **H**. PGAs.

The transient operation of the chip in CS mode is shown in Figure 8 with the solution capacitance, C_{sol} set to 140 fF. A global reset, rst, shorts the input and output of the integrator amplifiers which settle to approximately the mid-supply value, V_{ref}, of 0.95V. The reference voltage is sampled by enabling the addressed column buffer (*smpl_ref*) and stored

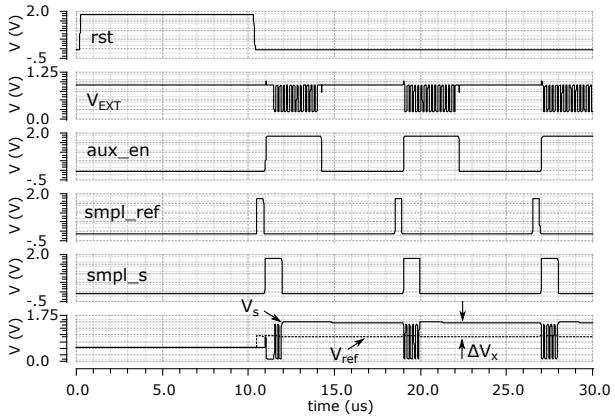

Fig. 8: Transient simulation of chip operation in CS mode.

on a 100 fF capacitor. A 200 mV pulse, V_{EXT}, is applied to the reference plate at a frequency of 10 MHz, where the solution is purely capacitive. The auxiliary capacitor is then enabled by turning on the *aux_en* switch and applying a voltage V_{aux} of 800 mV. This reduces the integrator output voltage, V_{s}, below the inverter threshold voltage to approximately 200 mV. This voltage is sensed and stored on a 100 fF capacitor after *smpl_s* is pulled low. After the sampling, V_{s} equals 1.48 V and V_{ref} equals 0.95 V, resulting in a difference, ΔV_{X}, of 530 mV. The solution capacitance is then determined as $\Delta V_{\mathrm{X}}/V_{\mathrm{EXT}} \cdot C_{\mathrm{i}}$ and equals 145 fF, which is within 3.5% of the expected value. The sensitivity of the CS circuit was simulated to be 20 mV/fF. This is limited by the integrator gain, set by the feedback capacitor C_i and can be increased by reducing the value of the capacitor at the expense of reduced dynamic range of the EIS channel.

Figure 9 shows the performance of the TIA in response to a peak-to-peak input current, I_{IN} of 1nA at a frequency of 10 kHz. Figure 9a shows the transient waveforms of the input current, the integrator output, V_{int} and the TIA output, V_d. Any offset and drift of the integrator output voltage due to dc current charging the feedback capacitor is cancelled by the intrinsic ac coupling of the differentiator as shown in the the V_{d} trace. Figure 9b shows a 1024-point FFT of the output of the TIA with the first 3 harmonics. The fundamental component is at -49 dB (A_{MID}=150dB), while the amplitude of the first harmonic is -84dB, giving a dynamic range of 35dB. The total harmonic distortion was calculated with the first 5 tones to be 2% at a frequency of 10 kHz. The dynamic range of the EIS channel is extended with the aid of a 2-stage resistive feedback PGAs with the gain of the first stage between 1 V/V and 8 V/V and the gain of the second stage selectable between 1, 10 and 100.

IV. Conclusion

This paper has presented the design of an integrated impedimetric biosensor chip in a CMOS process, which is currently in fabrication. To the authors' knowledge, this is the first chip featuring 1024 integrated sensors, which is suitable for performing dual-modality capacitive sensing and impedance spectroscopy. The chip lends itself to the development of low-cost multiplexed interfaces for detection, imaging and analysis of bacterial cultures and affinity-based assays.

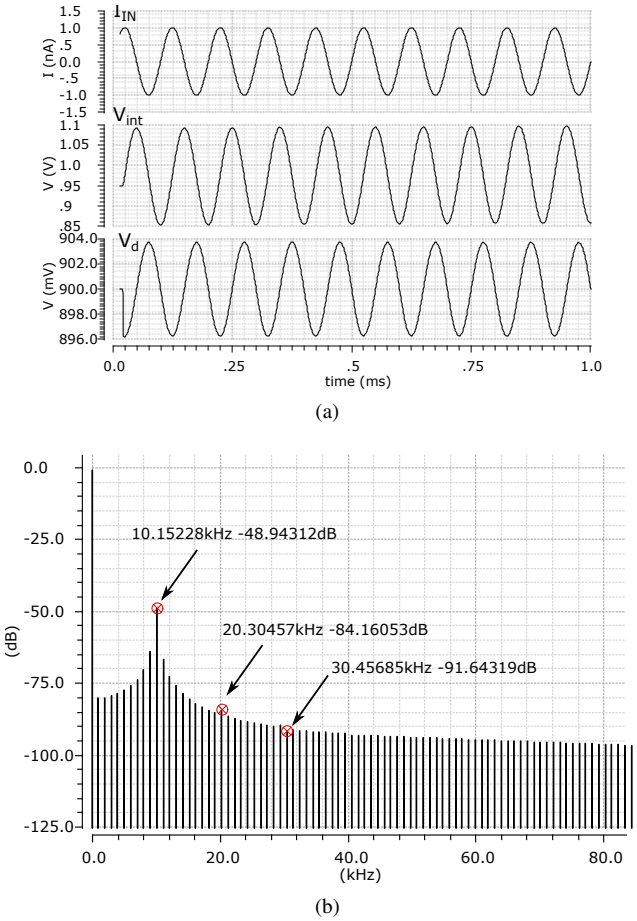

Fig. 9: Transient simulation of one EIS channel in response to a 1nA input current at a frequency of 1 kHz. (a) Transient waveforms. (b) 1024-point FFT of the output of the TIA.

References

[1] Couniot, N., Francis, L.A. & Flandre, D., 2016. A 16 x 16 CMOS Capacitive Biosensor Array Towards Detection of Single Bacterial Cell. IEEE Transactions on Biomedical Circuits and Systems, 10(2), pp.364374.

[2] Romani, A. et al., 2004. Capacitive sensor array for localization of bioparticles in CMOS lab-on-a-chip. In 2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No.04CH37519). IEEE, pp. 224225.

[3] Ghafar-Zadeh, E. et al., 2010. Bacteria Growth Monitoring Through a Differential CMOS Capacitive Sensor. IEEE Transactions on Biomedical Circuits and Systems, 4(4), pp.232238.

[4] Laborde, C. et al., 2015. Real-time imaging of microparticles and living cells with CMOS nanocapacitor arrays. Nature Nanotechnology, 10(9), pp.791795.

[5] Jafari, H., Soleymani, L., and Genov, R. (2012). 16-channel CMOS impedance spectroscopy DNA analyzer with dual-slope multiplying ADCs. IEEE Transactions on Biomedical Circuits and Systems, 6(5), 468-478.

[6] Katz, E., & Willner, I. (2003). Probing biomolecular interactions at conductive and semiconductive surfaces by impedance spectroscopy: Routes to impedimetric immunosensors, DNA-sensors, and enzyme biosensors. Electroanalysis, 15(11), 913947.

[7] Manickam, A., Chevalier, A., McDermott, M., Ellington, A. D., & Hassibi, A. (2010). A CMOS Electrochemical Impedance Spectroscopy (EIS) Biosensor Array. IEEE Transactions on Biomedical Circuits and Systems, 4(6), 37990.