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Effect of rapid thermal annealing on threading dislocation density in III-V epilayers monolithically grown on silicon

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In this work, we give a direct interpretation of micrographs of the 60° and 90° defect core at the GaAs/Si interface using aberration corrected scanning transmission electron microscopy. We investigate the post-growth annealing effects on dislocation rearrangement at the interface as well as the threading dislocations in buffer layers; finally, the density of threading dislocations has been calculated as a function of annealing temperature. https://doi.org/10.1063/1.5011161

I. INTRODUCTION

There are currently considerable efforts to achieve monolithically grown GaAs on a Si substrate with low defect density driven by a desire for an efficient integration into an established Si platform and subsequent reduced processing complexity.[1–5] But there are still a number of issues associated with epitaxial growth of GaAs on a Si substrate, such as the formation of anti-phase domains (APD) caused by the growth of polar on non-polar materials, the 4% lattice mismatch, and the 60% difference in thermal expansion coefficient between GaAs and Si.[6,7] The nature of the lattice defects that nucleate at the interface plays a very important role in the quality of the subsequent GaAs/Si epitaxial layers and the final device characteristics. These defects can be Lomer (90°) and 60° defects, as well as stacking faults and APDs.[6] It has been demonstrated that the formation of APDs and stacking faults can be minimized by utilizing a Si(001) substrate offcut towards [110] orientation by 4°–6°.[8,9] Lomer defects have Burgers vector of $\frac{1}{2}[011]$ or $\frac{1}{2}[01\bar{1}]$ and lie on the (100) plane. Since the Burger vector of Lomer defects is parallel to the GaAs/Si interface and therefore has no component in the $\langle 100 \rangle$ direction, it is not easy for these defects to glide towards the film surface. In contrast to Lomer defects, 60° defects only have an extra lattice fringe along the {111}direction. They have Burgers vector of $\frac{1}{2}[101]$, $\frac{1}{2}[10\bar{1}]$, $\frac{1}{2}[110]$, $\frac{1}{2}[1\bar{1}0]$, which form a 45° angle with the GaAs/Si interface and lie on {111} slip planes and hence can easily glide towards the film surface. Therefore, 60° defects can be a highly active source of threading dislocations (TDs) in the GaAs grown on Si. TDs that propagate into the active region act as non-radiative carrier recombination centers,[5,9] reducing minority-carrier lifetime and hence degrade the properties of the photonic device. Therefore, the means reduction or elimination of such propagating defects is a key precursor to the future commercialization of high performance GaAs/Si light emitting devices.[5,9]

Structural defect analysis performance by Otsuka *et al.*,[10] Narayan and Oktyabrsky,[11] and Vila *et al.*[12,13] was limited to model GaAs/Si interfaces in thin films; however, extended analysis in fully grown structures, particularly those in tilted GaAs/Si interfaces, is less well documented.[14,15] In this work, we investigated the effect of post growth thermal annealing (between 650 and 800 °C) on the evolution of 60° and Lomer defects at the GaAs/Si interface for a full laser diode structure (thickness > 6 μm). We apply high-resolution transmission electron microscopy (TEM) and aberration corrected scanning transmission electron microscopy (STEM) to evaluate the subsequent propagation of TDs into the overlaying epilayers and study the defect structure directly at the GaAs/Si interface.

II. EXPERIMENTAL

A. Sample growth

The InAs/GaAs quantum dots (QDs) sample was grown on a Si (100) substrate having a 4° offcut towards the $[01\bar{1}]$ plane by solid-source molecular beam epitaxy. The schematic layer structure is shown in Fig. 1(a) Oxide desorption of the Si substrate was performed at a temperature of 900 °C for 10 min. The substrate was then cooled down to 400 °C for the growth of a 30 nm GaAs nucleation layer. Two repeats of InGaAs/GaAs dislocation filter layers (DFL), consisting of 5 periods of 10-nm $In_{0.15}Ga_{0.85}As$/10-nm GaAs dislocation filter layers (DFLs) and 300-nm spacing layers, were grown on the top of an additional 770-nm GaAs buffer layer. Above this, 50 periods of the 2-nm GaAs/2-nm $Al_{0.4}Ga_{0.6}As$ superlattice complete the buffer layer. A typical five-layer InAs/InGaAs dot-in-a-well (DWELL) structure was sandwiched by two 50-nm AlGaAs layers and 50-nm GaAs layers, grown at optimized conditions described previously.[16,17] The DWELLs separated by 45-nm GaAs spacer layers and each DWELL layer consist of 3 monolayers of InAs grown on 2 nm of $In_{0.15}Ga_{0.85}As$ and capped by 6 nm of $In_{0.15}Ga_{0.85}As$.

B. Sample preparation

For the thermal annealing process, samples were first capped with a layer of the plasma-enhanced chemical-vapor deposited (PECVD) SiO_2 film. The rapid thermal annealing treatment (RTA) was carried out at 650 °C, 700 °C, 750 °C, and 800 °C for 30 s.

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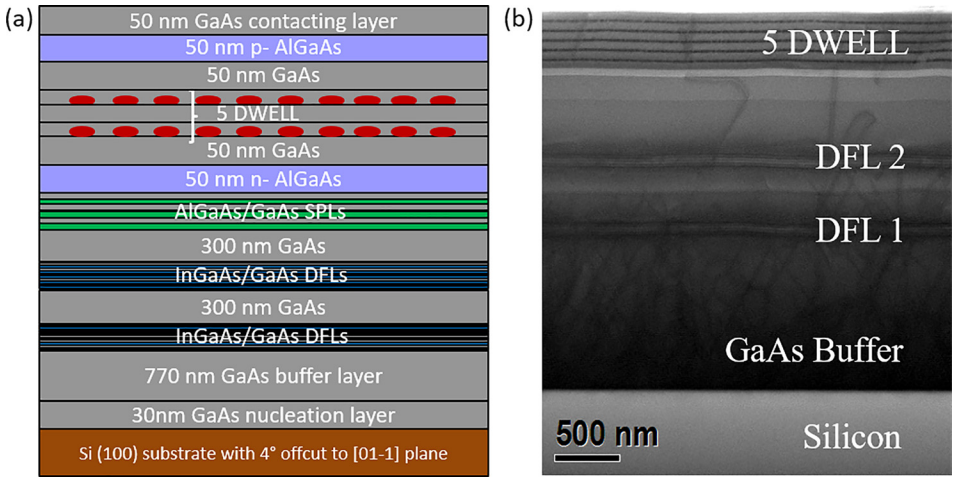

FIG. 1. (a) Schematic of the InAs/InGaAs dot-in-well structure monolithically grown on a Si substrate (b) Cross-sectional STEM BF image of the as grown InAs/InGaAs DWELL grown on a Si substrate.

Cross-sectional samples for TEM and STEM imaging were prepared parallel to the $[01\bar{1}]$ plane by the conventional grinding and mechanical polishing method, followed by Ar-ion milling (Fischione 1010 system, 3 kV Ar+ and incident angle of 6°–12°) to electron transparency.

C. Characterization methods

A series of initial bright-field STEM images were obtained using a JEOL 2010F field-emission gun TEM operating at 200 kV. Characterization of interface and defects in the GaAs/Si interface was performed by high resolution TEM and STEM imaging using a JEOL R005 double aberration corrected TEM/STEM operating at 300 kV. Lattice resolved STEM high angle annular dark field (HAADF) Z-contrast images were obtained with a convergence semi-angle of 21 mrads and a STEM inner annular collection angle of 62 mrads.

The dislocation density was measured from the bright field (BF) STEM images using a method proposed by Ham[18] and developed from papers by Bailey *et al.*[19] The dislocation density was calculated by introducing grid lines to the image and we measured the length of the grid lines, the thickness of the samples, and the number of the intersections of dislocations and grid lines. The way of calculating the density can be presented by the equation: $\rho = 2N/Lt$ in which ρ is the dislocation density, N is the intersection of dislocations with the projected grid lines, L is the length of lines in the image, and t is the thickness, which was obtained from analysis of the low-loss region of the Electron Energy Loss (EELS) spectrum.[20] As conventional TEM sample preparation inevitably produces an electron transparent region that is wedge shaped with respect to the thickness, over larger regions of interest the local thickness will vary. To allow for this, the specimen thickness was estimated at a number of locations within the region of interest and the mean thickness used in the TD density calculation for that region. The TD density was subsequently determined between the substrate interface and the first SLS1 and between SLS1 and SLS2 to enable a direct comparison for the influence of the different annealing temperatures.

III. RESULTS

Figure 1(b) shows the cross-section bright field (BF) STEM image of the as grown sample. The image clearly illustrates the high density of TDs that generate from the interface of GaAs and the Si substrate as a result of the large lattice mismatch and pass towards the surface. Even though the GaAs buffer layers and dislocation filter layers suppress the propagation of TDs to a great extent, there is still a significantly high density of TDs propagating into the active layer, which can contribute to the formation of non-radiative carrier recombination centers.[6,10]

The interface of the GaAs nucleation layer and Si substrate was analyzed in detail using aberration corrected TEM. Figures 2(a) and 2(b) show high-resolution images of the GaAs/Si interface with the Si substrate offcut 4° towards

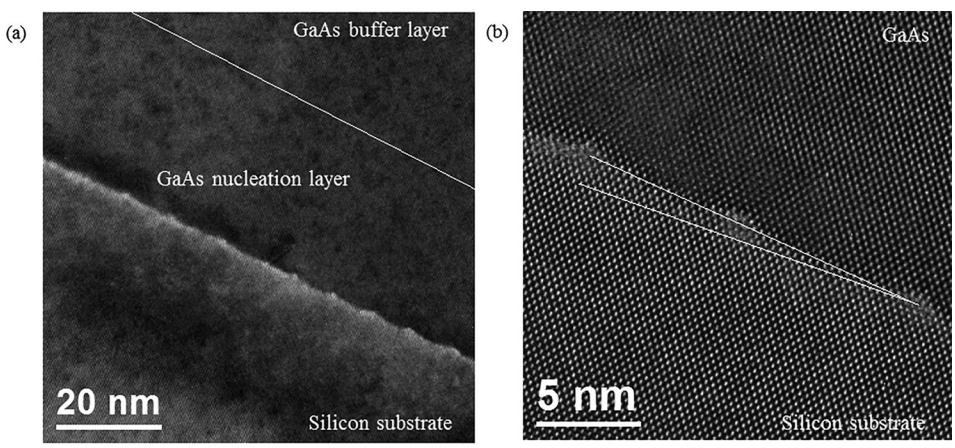

FIG. 2. [110] Cross-section HREM image of the as grown GaAs/Si interface.

the $[01\bar{1}]$ plane. In Fig. 2(a), Si surface steps generated by offcut of the substrate surface to the $[01\bar{1}]$ plane appear as a light spot localized at the interface. In the higher-resolution image of Fig. 2(b), the angle offcut from the (100) plane towards $[01\bar{1}]$ has been measured, as being $4^\circ \pm 0.5^\circ$ in good agreement with the corresponding wafer specification.

At the GaAs/Si interface, it has been proposed that the 4% lattice mismatch is relaxed mainly by misfit dislocations located at the interface,[11,19] as shown in Fig. 3, where the HAADF STEM image of the interface in the as-grown sample is observed along the $[01\bar{1}]$ zone axis. 60° defects and Lomer (90°) defects are clearly seen in the image as 60° defects marked as "/" or "\" along the terminating {111} planes and 90° defects marked as "⋀" by highlighting the two extra {111} half planes. In addition, the closely spaced (1∼2 nm) pairs of 60° defects [Fig. 3(b)] in which the two additional {111} planes do not terminate in one atomic ring have been observed.[12]

A more thorough analysis of the two types of dislocation core structures is illustrated in Fig. 4. The screw components and strain fields of dislocations introduce local crystal rotations to make it more difficult to determine the atomic positions inside the defect cores using conventional BF TEM imaging.[21] Aberration corrected STEM imaging on the other hand offers a significant improvement in the spatial resolution and therefore opens the opportunity to direct imaging of the atomic positions within defect structures. The dumbbell shaped spots observed in Figs. 4(a) and 4(b) correspond to the projection of the (004) atomic columns of Ga-As or Si-Si

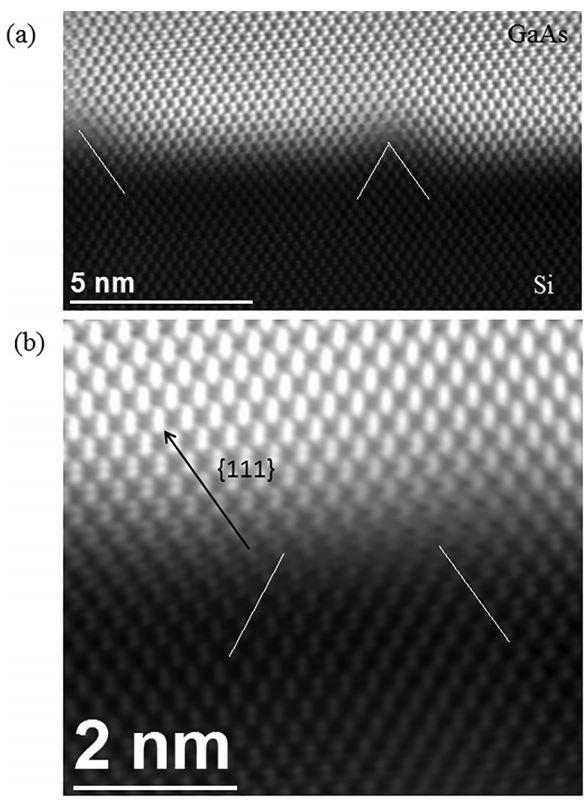

FIG. 3. (a) [110] Cross-section HR HAADF STEM image of the as grown GaAs/Si interface. "/", "\", and "⋀" marked the extra {111} half planes. (b) An example of the 60° defect pair at the GaAs/Si interface.

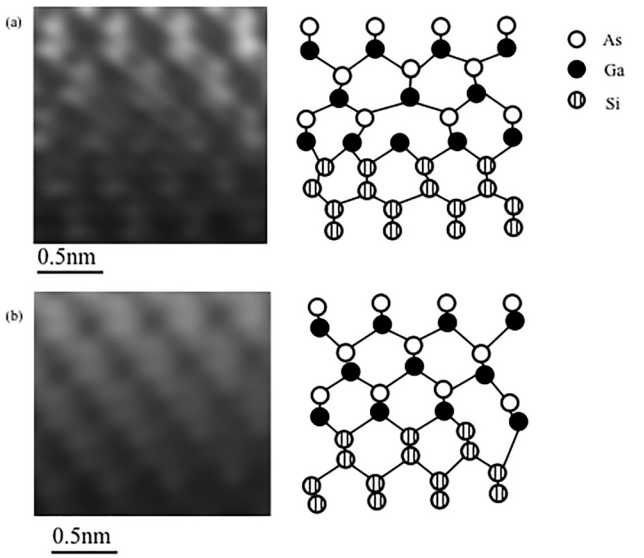

FIG. 4. Atomic resolution HAADF STEM image shows (a) the 90° and (b) 60° dislocation core in GaAs/Si interfaces and the corresponding schematic configuration.

viewed along the $[01\bar{1}]$ direction. As the imaging intensity in HAADF imaging is approximately proportional to the square of the mean atomic number Z (Z_{Ga}=31, Z_{As}=33, Z_{Si}=14),[22] the Ga-As atomic columns will appear brighter than Si-Si atomic columns. In addition, the As columns should in theory appear brighter than the Ga columns assuming that the ordering is not mixed in the projection of the electron probe.[23,24] In this way, the atomic ordering at the interface can be distinguished and the structure of two defects types at the GaAs/Si interface was revealed.

Figure 4(a) presents an atomic resolution HAADF STEM image of a 90° defect core and possible structural model. The atomic position shows good agreement with the model predicted by anisotropital elasticity proposed by Vilà.[13] The 90° dislocation core is a symmetrical 8-atom ring configuration with a single Ga atomic column at the centre of the defect core.[13,21] In contrast to the 90° defect cores, the 60° defect cores at the GaAs/Si interface are asymmetric and are obtained by adding an atomic couple to a standard six-atom ring to form an eight-sided configuration. The model for the 60° defect core in bulk materials[21] and in the heterostructure has been proposed by Vila.[12] In Fig. 4(b), the high resolution HAADF STEM image shows a 60° defect core containing a single column of the As dangling bond, consistent with the expected structure for the 60° defect core.

Post-growth annealing provides the energy for threading dislocations to interact with each other and SLSs. TDs move to edge and interface; TDs with opposite Burgers vectors meet each other under high thermal stress and annealing temperature and annihilation are assumed. To demonstrate the effect of rapid thermal annealing on threading dislocations, low magnified cross-sectional STEM images of the buffer layers and two DFLs were observed from the as-grown and annealed samples under similar magnification conditions. As seen, in Fig. 5(a), owing to the large lattice mismatch and different thermal expansion coefficient between GaAs and

Si, a high density of dislocations is nucleated at the GaAs/Si interface and propagated towards the film surface. Although the two-step low temperature growth technique and SLSs act as dislocation filters, with most of the dislocations being confined before the first SLSs, the density of TD propagating towards the active region nevertheless remains unacceptably high in the as grown sample. As shown in Fig. 5(b) 650 °C, 5(c) 700 °C, 5(d) 750 °C, and 5(e) 800 °C, the TDs in the annealed samples are markedly reduced as a function of annealing temperature and the continuous threading dislocations become discontinuous after annealing. In addition, a clear increase in the TDs running parallel to the DFLs can be observed which suggests that rapid thermal annealing enhanced the role of SLSs, bending the TDs into the growth plane.[25,26]

Figure 6 shows the measured threading dislocation density (TDD) in buffer layer of the as-grown and annealed samples. The density of TDs in the as-grown sample is $\sim(6.9 \pm 1.8)\times 10^9\,\mathrm{cm}^{-2}$. The TDD has been markedly reduced to $\sim (1.3 \pm 0.3)\times 10^9\,\mathrm{cm}^{-2}$ after 800 °C rapid thermal annealing. The density of TDs during annealing has been shown to be approximately exponential as a function of annealing temperature when the annealing time is fixed at 30s, consistent with the theory present by Farrell *et al.*[27] The TDD in the region before the DFL1 area can almost approximately fit in the equation: $y = 820.82 \times \exp(-0.00799x)$. As shown in Fig. 6, the TDD in the area between DFL1 and DFL2 decreases from $\sim(1.83 \pm 0.45)\times 10^9$ to $(0.446 \pm 0.03) \times 10^9$ after 800 °C annealing. However, the number of TDs in the area between DFL1 and DFL2 is much less than the

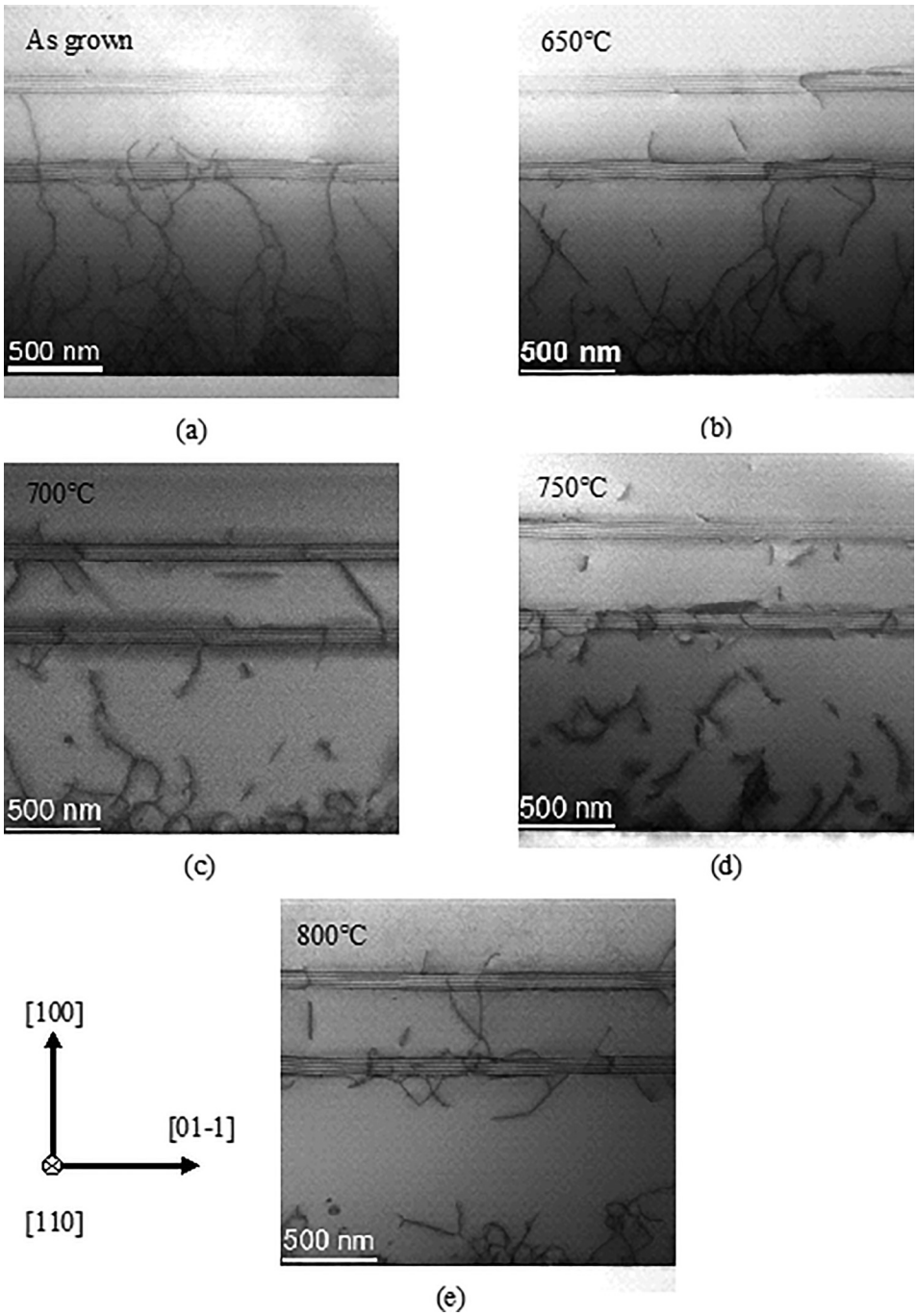

FIG. 5. Cross-section STEM images of DFLs illustrate the effect of annealing on threading dislocation under different temperature conditions.

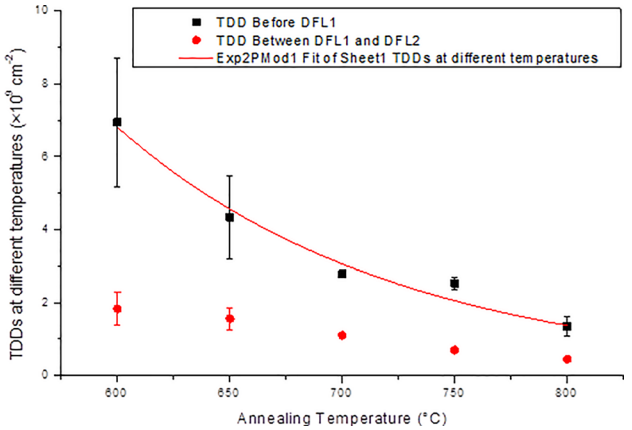

FIG. 6. The density of TDs after annealing at different temperatures.

one in the GaAs buffer layer; the TDD after the first DFL does not change obviously.

From the analysis of a series of HAADF STEM images, the number of isolated 60° defects was established as being of a similar magnitude to that of the Lomer defects at the GaAs/Si interface in the as-grown sample. This was reduced to one seventh of the total number of defects observed after 800 °C annealing. On the other hand, the number of 90° defects exhibited was a little increased after 800 °C annealing. The number of 60° defect pairs observed remained relatively constant after 800 °C rapid thermal annealing. It has been proposed by Narayan[12] that these types of defects cannot be annealed out, (note that[18] Tsai and Lee considered 60° defects pairs instead of 90° defects) because of their parallel screw components.[12] It is apparent from Table. I that the isolated 60° defects can react to form 90° defects, which can also be explained as the following equation:

$$\frac{1}{2}[110](111) + \frac{1}{2}[10\bar{1}](\bar{1}\bar{1}\bar{1}) = \frac{1}{2}[110](100).$$

IV. DISCUSSION

The threading dislocation density in the GaAs buffer layers has been shown to be significantly reduced by high-temperature annealing. The post-growth annealing provides the energy for threading dislocations to interact with each other and the DFLs. Threading dislocations with opposite burgers vectors meet each other under high thermal stress and annealing temperature; annihilation is assumed.[10,28] The effectiveness of the SLSs in bending threading dislocations is improved.[29] In Fig. 5, it is apparent that an increased number of TDs are observed parallel to the GaAs/Si interface and SLSs in the buffer layer after rapid thermal annealing.

TABLE I. Percentage of different types of defects at the GaAs/Si interface observed before and after 800 °C annealing.

	As grown	After 800 °C annealing
Type I (90°)	36%	57%
Type II (60°)	35%	11%
60° dislocation pairs	29%	32%

Therefore, fewer TDs propagate towards the active layer, with the density of TDs in upper layers above the first DFL significantly less than in the buffer layer as illustrated in Fig. 6.

The velocity of dislocation glide motion and the concentration of vacancies which enhance the motion of dislocations are exponentially increased with an increase in temperature. Therefore, the TD density is reduced more effectively when the rapid annealing temperature is increased. However, it should not be forgotten that post-growth annealing also influences the active layer. When annealing temperature increases up to 850 °C, the DWELL structure appears like a quantum well structure and optical properties of DWELL degrade seriously. So, annealing temperatures have been controlled in a range of 650 °C to 800 °C. At 800 °C, rapid thermal annealing shows an effective method of improving the quality of epilayer wafer, lighting the way of in-situ thermal cycle annealing.

V. CONCLUSIONS

The effects of rapid thermal annealing on the GaAs/Si interface and threading dislocation density were investigated in GaAs monolithically grown on a Si (100) substrate offcut 4° towards the $[01\bar{1}]$. High resolution Z contrast scanning transmission electron microscopy images have revealed the structure of 60° and 90° defects cores at the Si/GaAs interface. It was found that isolated 60° defects react to form 90° defects during rapid thermal annealing up to 800 °C. The TD density was remarkably reduced in GaAs epilayers as a result of the thermal annealing. This was caused by the reaction and the annihilation of dislocations and also the easy-glide isolated 60° defects react to form 90° defects with subsequent burgers vectors parallel to interface. We therefore have demonstrated a potential route of in-situ thermal annealing to generate improved quality GaAs epilayers monolithically grown on Si.

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