Intermittent Excitation of High-Q Resonators for Low-Power High-Speed Clock Generation

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***Abstract*—There is growing demand for circuits that can provide ever greater performance from a minimal power budget. Example applications include wireless sensor nodes, mobile devices, and biomedical implants. High speed clock circuits are an integral part of such systems, playing roles such as providing digital processor clocks, or generating wireless carrier signals; this clock generation can often take a large part of a system's power budget. Common techniques to reduce power consumption generally involve reducing the clock speed, and/or complex designs using a large circuit area. This paper proposes an alternative method of clock generation based on driving a high-Q resonator with a periodic chain of impulses. In this way, power consumption is reduced when compared to traditional resonator based designs; this power reduction comes at the cost of increased period jitter. A circuit was designed and laid out in 0.18μm CMOS, and was simulated in order to test the technique. Simulation results suggest that the circuit can achieve a FoM of 4.89GHz/mW, with a peak period jitter of 10.2ps at 2.015GHz, using a model resonator with a Q-factor of 126.**

I. Introduction

In the realm of low power devices, such as those designed for biomedical, mobile, or IoT applications, there is an ever growing demand for increased functionality within a power budget that is as small as possible [1], [2]. Clock sources are a crucial component of such devices, examples include digital processor master clocks, and wireless carrier generation. As such, a circuit that can generate a clock signal, particularly at high speeds, with a low power footprint is very desirable. Many strategies exist to tackle this problem, since for the given target of reduced power consumption, it is generally possible to make compromises in other areas (circuit area, clock speed, jitter, etc.) depending on the application. For instance, the work in [3] describes a Digitally Controlled Oscillator (DCO) design, that runs at a relatively low frequency (5.8MHz - 13.9MHz). For sensor nodes that perform only basic computations, or for generating a 13.56MHz carrier for RFID, this frequency range would be acceptable. Such low-frequency DCOs can be further adapted to improve performance through more complex implementations at the cost of circuit area. For example, [4] describes two complementary DCOs, a low power 100nW DCO locks to an accurate 1μW DCO periodically, so as to correct for drift over time in the 100nW DCO. This allows for a 100kHz clock to be generated with an effective power consumption of 150nW. DCOs are not limited to low-frequency operation, for example a wide range 5MHz - 2.4GHz synthesizer based on a frequency locked loop is presented in [5]. However this high speed comes at the cost of high power consumption. For the case of a high speed clock, for example 2.4GHz for a WiFi carrier, DCOs require similar amounts of power as cross-coupled LC oscillators or PLL-based designs, which usually require several mW. Even in the case of an aggressively scaled low-power PLL circuit [6], the power consumption is still 1.82mW at 2.2GHz.

This work presents an alternative approach to high-speed low-power clock generation, that is based on periodic excitation of a high-Q resonator. In the case of a traditional resonator-based oscillator, positive feedback allows for continuous oscillation at the fundamental frequency of the resonator. By contrast, this work proposes driving the resonator periodically with sharp impulses in order to generate a continuous sequence of damped oscillations. This allows for a significant reduction in power consumption in exchange for increased period jitter. The technique can be adjusted as necessary so as to optimize the tradeoff between power consumption and period jitter depending on application.

The paper is organised as follows: Section II describes the fundamental theory of the proposed method, Section III describes the design of the circuits necessary to implement the method. Section IV presents simulation results of the designed circuit, and Section V concludes the paper.

II. Theory

A. Impulse-Driven Resonators

A generic model of a parallel LC resonator with series loss is shown in Fig. 1. This model is a good representation of a standard wirewound inductor, where L is the inductance, R_S is the series loss of the coil, and C_P is the parallel capacitance. The rest of the paper assumes an inductor based resonator of

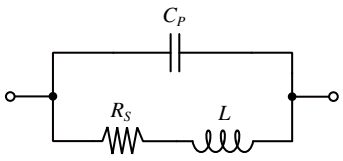

Fig. 1: Simple parallel resonator model.

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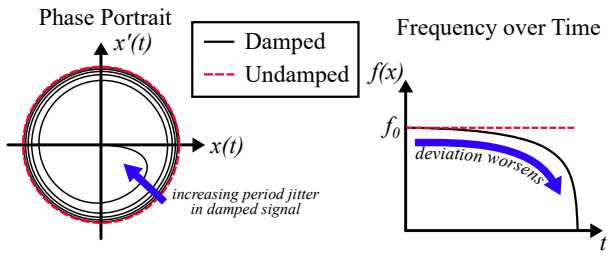

Fig. 2: Damped vs continuous oscillations. $x(t)$ is the resonator current, $f(x)$ is the instantaneous frequency.

this type, but the theory still applies to other parallel resonant devices, such as quartz crystals, high-Q MEMS devices [7], or quarter-wave resonators.

When designing circuits with such resonators, it is generally sufficient to consider the fundamental frequency f_0, approximated by (1):

$$f_0 \approx \frac{1}{2\pi\sqrt{LC_P}} \tag{1}$$

In accordance with 1 the oscillator output frequency can be defined as $f_{osc} = f_0$. If the resonator is driven with an impulse however, the oscillation frequency will decrease over time as the oscillation amplitude decays.

The principles of decaying self-oscillation are discussed in detail by Groszkowski [8]; the most useful parameter to take from this analysis is the damping factor α, defined as:

$$\alpha = \frac{R_S}{2L} \tag{2}$$

The damping factor α defines the rate at which the damped oscillation decays, and is inversely proportional to the Q-factor. The difference between an undamped continuous oscillation and a damped oscillation is illustrated in Fig. 2.

Fig. 2 shows that the damped oscillation frequency begins very close to f_0, but diverges over time, with a reduction in frequency until it eventually stops. This divergence can be considered analogous to increasing period jitter with respect to the original period $1/f_0$. This is in contrast to the undamped case, which can be approximated by a regular harmonic oscillator, where (in the ideal case) the gain of the oscillator can be considered to cancel the loss R_S, allowing a continuous oscillation at f_0. The rate of this divergence over time is proportional to the damping factor α. Therefore, the higher the Q factor, the longer a damped oscillation will remain close to f_0. This fact forms the basis of the proposed clock-generation technique.

B. Approximating Continuous Oscillation

The proposed technique involves approximating a continuous oscillation by generating a sequence of damped oscillations, by driving a resonator with a series of sharp impulses. By applying an impulse to a resonator periodically with a switched MOSFET, less power is consumed than from driving a resonator every cycle with a feedback circuit with MOSFETs

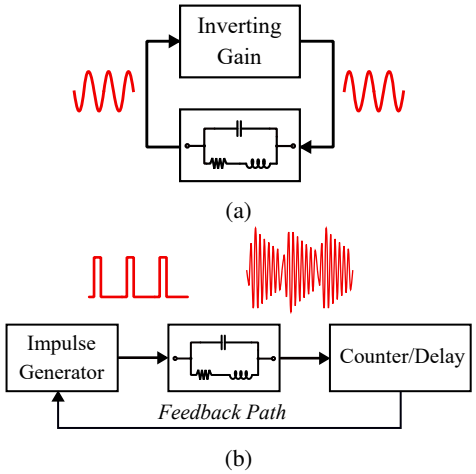

Fig. 3: Comparison between a traditional harmonic oscillator (3a), and the impulse-driven technique (3b).

in saturation, as in traditional harmonic oscillators. Fig. 3 illustrates the technique, and the theory of action is described as follows. Once the circuit starts, the impulse generator excites the resonator with a sharp impulse, and the resonator will begin a damped oscillation. The counter and delay block should then count a set number of cycles, wait for a specified delay time, then re-trigger the impulse generator to refresh the oscillations in the resonator. The counter target determines how often the impulse generator should trigger, refreshing the resonator oscillations. By adjusting the counter target, it is possible to adjust the tradeoff between power consumption and period jitter. A higher count target gives more time for the oscillation to decay, and thus more period jitter, but will require less power for impulse generation, and vice versa. As the Q of the resonator increases, less frequent impulses are required in order to maintain a constant level of period jitter. The purpose of the delay before triggering the impulse generator is to fine-tune the exact point at which the resonator is re-excited. If the impulse occurs too early or too late, the current oscillatory period will be either cut short or over extended, creating a sudden burst in instantaneous period jitter. It is imperative therefore that the delay be tuned precisely to minimize this potential side-effect.

III. Circuit Design

Fig. 4 shows the circuit designed to test the principle. To force the circuit to start reliably, a simple startup circuit generates a ramp as long as V_{reset} is low, this eventually sends a rising edge to the impulse generator. The impulse generator circuit is shown in Fig. 5. By taking the difference between an incoming rising edge and a delayed version of that edge, it is capable of producing pulses with a width of ≈ 300ps. The impulse generator drives M_0 as a switch, which is used to excite the resonator. M_0 should be sized appropriately, such that when driven by an impulse, the voltage at V_{res} comes as close to 0V as possible without distortion. The goal when sizing M_0 is to optimize for a maximum oscillation amplitude

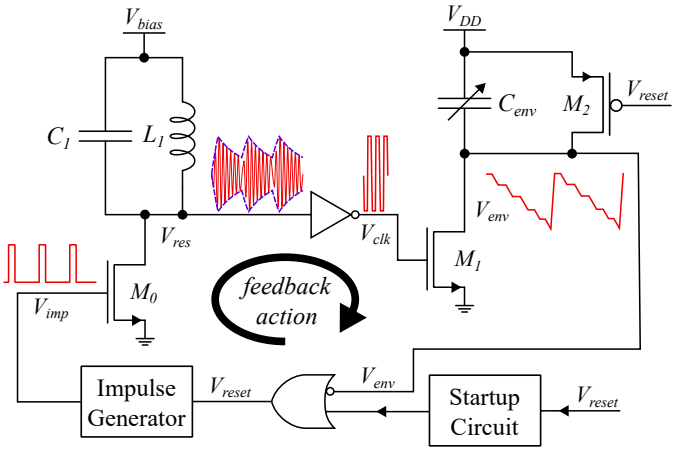

Fig. 4: Simplified circuit diagram of the impulse-driven clock circuit.

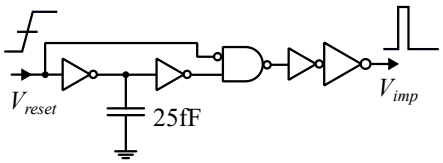

Fig. 5: Detail of the impulse generator subcircuit used in Fig. 4.

with minimal impulse current. By setting V_{bias} to the crossover voltage of the inverter, the decaying sinusoid bursts at V_{res} can be converted into a square clock signal at V_{clk}. The counter and delay function is implemented by M_1, C_{env}, and M_2. For each pulse at V_{clk}, M_1 adds a charge to C_{env}. Once sufficient charge has been added to force V_{env} to cross the logic level, V_{reset} is triggered, triggering the impulse generator and resetting V_{env} back to V_{DD}. Both the count target and the delay are controlled by the combination of the size of M_1 and the size of C_{env}.

To determine a first order approximation of the behaviour of the counter/delay circuit, begin by defining I_{M_1} as the current drawn by M_1 when its gate is pulled to V_DD. Since the duty cycle of V_{clk} should be close to 50%, the waveform can be considered as a sawtooth, with the time of each ramp-down τ_{env} being defined as follows:

$$\tau_{env} = \frac{2C_{env}(V_{DD} - V_t)}{I_{M_1}} \tag{3}$$

where V_t is the logic threshold. The relation in (3) can be used to approximate the number of cycles to be generated by the resonator until the next impulse is sent, by comparing τ_{env} with the period $1/f_0$.

A. Jitter and C_{env}

In order to tune τ_{env}, either the current sourced by M_1 or the value of C_{env} should be tunable. In this case C_{env} was designed as a tunable on-chip capacitor. Since C_{env} is also in control of the delay part of the scheme, it is important that it can be finely tuned such that period jitter can be minimized. To this end, C_{env} was designed with the goal of having the smallest tuning steps achievable.

TABLE I: Resonator parameters in accordance with Fig. 1.

Parameter	*Value*
L	80nH
C_P	50fF
R_S	10Ω

Before determining the size of C_{env}, the resonator parameters must first be known. For this design an example resonator was specified with the parameters listed in Table I, targeting an f_0 of approximately 2.5GHz, with a Q (at f_0) of 126.5.

Through schematic simulation of the circuit illustrated in Fig. 4, it was determined that a C_{env} value of 6.55fF would allow for 8 cycles to pass and correctly set the delay for the impulse to refresh the resonator. This translates to a τ_{env} of approximately 2.89ns, computing $8/\tau_{env}$ suggests an average clock frequency of 2.77GHz. There is error here since the rise time of V_{env} is not considered, as well as the additional capacitance seen at the resonator from the circuit, leading to a final average simulated clock frequency of 2.1GHz for $C_{env} =$ 6.55fF.

The deterministic jitter due to α was assessed in terms of mean absolute derivative period jitter ϕ_{avg}:

$$\phi_{avg} = mean\left(\left|\frac{d(\tau_{pj}(V_{clk}))}{dt}\right|\right) \tag{4}$$

where $\tau_{pj}(V_{clk})$ is the instantaneous period jitter of V_{clk} in seconds, taken with reference to the average frequency. ϕ_{avg} is a unitless quantity, where an ideal continuous oscillation would have $\phi_{avg} = 0$. For $C_{env} = 6.55$fF the schematic simulation resulted in a ϕ_{avg} value of 0.0064, derived from a peak $\tau_{pj}(V_{clk})$ of $\approx$ 8ps ($\approx$ 1.7% of the period 476ps $= (2.1\text{GHz})^{-1}$).

The jitter τ_{pj} is very sensitive to the value of C_{env}. Therefore, C_{env} was designed iteratively through manual layout adjustments, with the goal of sub-10aF per bit resolution. The final design was realised by combining a 7-bit capacitor for coarse tuning and a 4-bit capacitor for fine tuning. This resulted in an effective 11-bit resolution. In order to force monotonicity in C_{env}, all the possible control codes and their resultant capacitances were simulated, and the results were sorted. In this way a lookup table describes how to control the capacitor such that it behaves monotonically. The final result therefore was a capacitor with an average step resolution of 0.8aF, and an output range of 4.145fF - 5.812fF. This combines with extra parasitic capacitance in the layout to reach the desired 6.88fF nominal target.

IV. Postlayout Simulation Results

With C_{env} designed, the rest of the circuit was laid out in 0.18μm CMOS. Since the design is sensitive to parasitic capacitances (recall earlier that C_{env} requires an additional 1-2fF from parasitics) the layout was refined through iterations of postlayout simulation. The layout is shown in Fig. 7, with

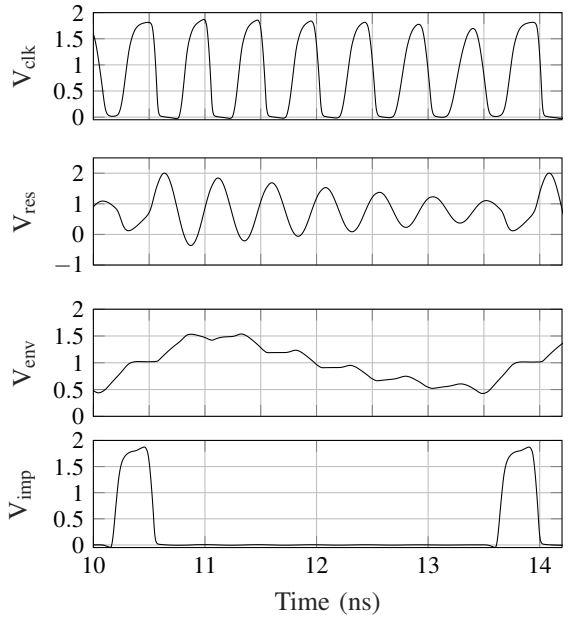

Fig. 6: Postlayout simulation waveforms showing key signals.

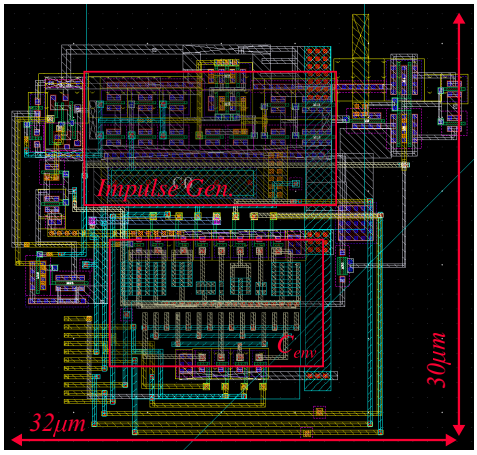

Fig. 7: Circuit layout.

dimensions of $32\mu\text{m} \times 30\mu\text{m}$; most of the area is taken by the impulse generator and C_{env}.

Postlayout simulations were run (using the same resonator model from Table I) in order to determine the effect of layout on the circuit performance. The key simulation results are summarized in Table II, with the circuit operating from a 1.8V supply. The results show that the circuit is capable of generating a 2GHz clock signal while dissipating only 412μW from a 1.8V supply. This translates to a FoM of 4.89GHz/mW,

TABLE II: Key simulation results.

	Average Frequency	*Supply Current*	ϕ_{avg}
Schematic	2.106GHz	173μA	0.0064
Postlayout	2.015GHz	229μA	0.0177

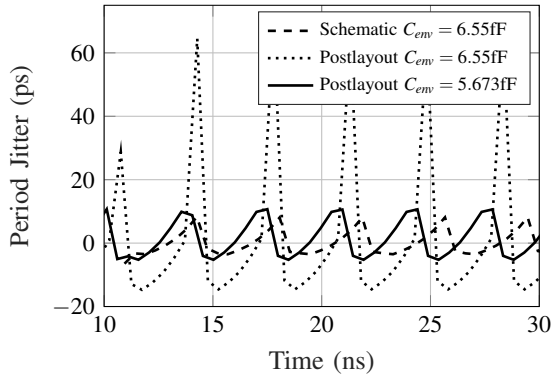

Fig. 8: Instantaneous period jitter $\tau_{pj}(V_{CLK})$ for differing values of C_{env}.

which compares favourably with other contemporary designs [5], [6].

Fig. 8 shows the importance of C_{env} being finely controllable; a difference of 0.879fF is enough to reduce the peak period jitter τ_{pj} from 63ps to 10.6ps.

V. Conclusion

A technique for clock generation through periodic pulsing of a high-Q resonator has been developed, and an accompanying circuit has been designed and presented. The circuit was designed in 0.18μm CMOS and simulated, with the results suggesting operation at a frequency of 2GHz, with a power consumption of less than 0.5mW is possible from a 1.8V supply. This technique could prove particularly applicable for low power applications such as wireless carrier generation or processor clock synthesis for low power sensor nodes or biomedical devices. Future work would include fabrication of the circuit and testing with resonators of varying Q-factor, to aid in determining the limits to which the power savings can scale with increasing Q-factor.

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