A CMOS dynamic random access architecture for radio-frequency readout of quantum devices

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As quantum processors become more complex, they will require efficient interfaces to deliver signals for control and readout while keeping the number of inputs manageable. Complementary metal-oxide-semiconductor (CMOS) electronics offers established solutions to signal routing and dynamic access, and the use of a CMOS platform for the qubits themselves offers the attractive proposition of integrating classical and quantum devices on-chip. Here we report a CMOS dynamic random access (DRAM) architecture for readout of multiple quantum devices operating at millikelvin temperatures. Our circuit is divided into cells, each containing a control field-effect transistor and a quantum dot (QD) device, formed in the channel of a nanowire transistor. This setup allows selective readout of the QD and charge storage on the QD gate, similar to one-transistor-one-capacitor (1T-1C) DRAM technology. We demonstrate dynamic readout of two cells by interfacing them with a single radio-frequency resonator. Our approach provides a path to reduce the number of input lines per qubit and allow large-scale device arrays to be addressed.

Quantum computers could be used to solve problems that seem intractable with conventional computers [1]. Several different physical implementations of a quantum computer are being developed [2] and state-of-the-art processors are approaching the level of 50 to 100 quantum bits (qubits), a point at which quantum computers are expected to demonstrate capabilities beyond conventional computers for specific tasks [3].

For most physical realisations, quantum processors require cryogenic temperatures to operate, precise low-noise control signals [4] to manipulate the information, and highly sensitive readout techniques to extract the results – all without disturbing the fragile quantum states. In current solid-state quantum processors, signals are generated using general-purpose instruments at room temperature and delivered to the quantum processor at low temperatures. The physical qubits across all platforms are controlled directly with at least one control line per qubit. However, as the size of quantum processors continues to increase, the one-qubit-one-input approach will be unsustainable [5], especially if we consider that a large-scale fault-tolerant quantum computer might ultimately require 10^8 qubits to solve computationally demanding algorithms [6]. Efficiently delivering control and readout signals to increasingly more complex quantum circuits, while reducing the number of inputs per qubit, is a key challenge in developing a large-scale universal quantum computer. Integrated electronics provide a solution to these problems. Some of the challenges that face large-scale quantum computing resemble those that have already been solved for conventional computing. For example, controlling billions of transistors with just a few thousands of input-output connections. Moreover, integrated electronics allows signal generation, data flow management, low-level feedback and high-level operations locally. Therefore, to relax wiring requirements and reduce the latency of solid-state quantum computers, the integration of conventional electronics with quantum devices at cryogenic temperatures could be a promising strategy [7, 8]. However, to apply this approach, understanding the behaviour of integrated circuits at cryogenic temperatures is vital [9].

Digital information processing devices are typically manufactured using silicon as the base material. Coincidentally, electron spins in silicon are amongst the most promising candidates for large-scale quantum computing due to their small footprint (sub 100 nm dimensions) and very long coherence times, particularly in isotopically purified ^{28}Si [10, 11]. Silicon-based spin qubits benefit from a variety of qubit designs and different coupling strategies [12–19] and can be read out dispersively using Pauli spin-blockade [20–22]. To date, operation of one-dimensional arrays has been demonstrated [23], high-fidelity single qubit gates [10, 24–26] and two qubit gates [12, 19] have been achieved and a programmable two-qubit silicon-based processor has been created [18].

Recently, it was shown that CMOS transistors can be used as the basis for spin qubits [27, 28]. Several other silicon-based quantum devices could, in principle, be realised in a manner compatible with industrial CMOS pro-

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cesses, with the potential of large-scale, high-yield fabrication. It seems natural, then, to explore the direct integration of silicon quantum devices and conventional CMOS technology to tackle the challenges in addressing, controlling and reading multi-qubit circuits. Blueprints of such all-silicon systems integrating quantum and classical components have emerged [29–31] and basic demonstrations of direct integration have been reported [32].

In this Article, we report a CMOS dynamic random access architecture for readout of multiple quantum devices. Our design is inspired by the square arrays found in one-transistor-one-capacitor (1T-1C) dynamic random access memory (DRAM) and allows on-demand routing of static and radio-frequency (RF) signals to individual devices. The architecture is composed of individual cells each containing a control field-effect transistor (FET) and a quantum dot (QD) device. In our experiments, the QDs are themselves formed in the channel of a nanowire FET, integrated on the same chip as the control FETs and fabricated using the same CMOS processes. When not addressed, each cell can be used as a node to store charge on the QD device gate that allows trapping single-electrons in the QD device with a time constant approaching 1 s. We demonstrate random access and readout of two individual cells at cryogenic temperatures using capacitive gate-based RF reflectometry [33–35]. We obtain a readout bandwidth of 13 MHz measured from the frequency overlap of two individually addressed cells, and find optimal operation voltage levels for the control transistor. Moreover, we show dynamic readout of the cells and obtain charge stability maps sequentially. Finally, we provide guidelines for scaling the approach by developing an equivalent DC and RF circuit model of the cell, and a 2D architecture with a quadratic reduction in the number of inputs.

CIRCUIT CHARACTERISATION

We show the sequential access circuit in Fig. 1a. It consists of two CMOS single-electron memory cells [32] (cell 1(2) in green(orange)) connected to a lumped-element RF resonator for readout and a single bias line. Each memory cell is made from two transistors which we refer to as Q_i and T_i. Q_i is a 60-nm-wide silicon nanowire transistor with a short gate length (25 and 30 nm for cell 1 and 2 respectively). Such devices are routinely used to trap single-electrons in QDs that form at the top most corners of the nanowire channel when operated in the sub-threshold regime at cryogenic temperatures [36]. Transistor T_i is a wider device with a channel width of 10 μm and gate length of 25 nm and 30 nm for cell 1 and 2 respectively which we refer to as the control FET. The four transistors are manufactured using fully-depleted silicon-on-insulator (FD-SOI) technology following standard CMOS processes. They are located on the same chip and are connected via bond wires (see Methods for details of the fabrication and Fig. 1a for a schematic).

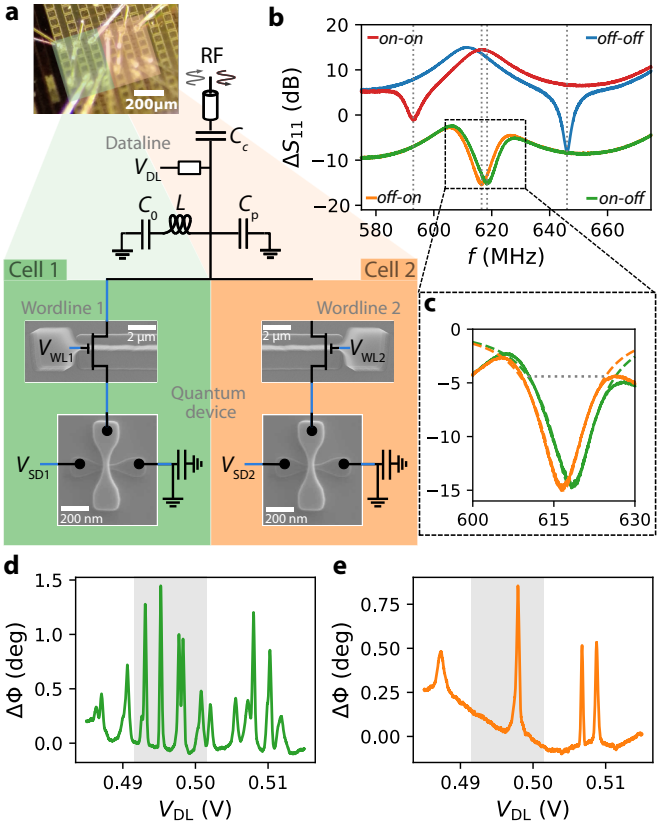

FIG. 1. **Setup and individual device characterisation.** **a**, Sequential access circuit for gate-based RF readout with optical microscope image of parts of the circuit as inset. A single high frequency line and readout resonator is connected to two cells (green and orange) consisting of one control FET, T_i, and quantum device, Q_i, per cell. T_i enables selective readout of Q_i. Electrical connections made via bond wires are represented by blue lines. **b**, Reflection coefficient spectrum of the circuit for different control FET states (T_1 - T_2). Spectra for addressing a single cell have been shifted down by 15 dB for clarity. **c**, Enlarged view of *on-off* and *off-on* state configurations with a spectral overlap and resonance fits indicated (by dashed lines). **d**, Phase response of Q_1 as a function of V_{DL} for $V_{WL1} = 1.2$ V and $V_{WL2} = 0$ V. **e**, Phase response of Q_2 as a function of V_{DL} for $V_{WL1} = 0$ V and $V_{WL2} = 1.2$ V. The regions in grey highlight charge transitions we focus on in further measurements.

We label the primary inputs of the circuit as data and word lines in analogy with memory chips. Each cell has one word line, with voltage V_{WLi}, which connects to the gate of the control FET T_i allowing control over the channel resistance. The data line, with voltage V_{DL}, is shared among the two cells and allows control over the gate voltage on Q_i conditional on the state of T_i. Additionally, a voltage applied to the silicon substrate, V_{BG}, acts as a back-gate. Switching T_i to the *on* state while keeping all the remaining T_j *off* allows for individual addressing of a single quantum device Q_i. Multiple devices can

be addressed sequentially by timing the voltages on T_i accordingly, as we demonstrate further below.

To read the quantum state of the devices, we connect a lumped-element LC resonator in parallel with the memory cells and use RF reflectometry to probe the resonant state of the combined circuit [32]. We couple the RF signal into the data line via the coupling capacitor C_c. The natural frequency of the resonator f_0 is given by $f_0 = 1/2\pi\sqrt{LC_\mathrm{T}}$ where C_T is the total capacitance of the system that includes, in particular, the state-dependent quantum or tunnelling capacitance of any quantum device [37] which is connected to the LC circuit via the control FETs. The whole circuit is operated in a dilution refrigerator with a base temperature of 15 mK.

Next, we show the frequency dependence of the circuit's reflection coefficient S_{11} in Fig. 1b for the four possible states of the two control FETs. A dip in the reflection coefficient occurs when we drive the resonator at its natural frequency of oscillation. This frequency shifts towards lower values (by approximately 28 MHz) for each T_i in the *on* state due to the additional circuit capacitance introduced by the enabled cell. In Supplementary Table 1 we report a comprehensive list of circuit parameters describing the resonance conditions depending on the logic state of each cell. Most importantly, we observe a large spectral overlap of 13 MHz with 3 dB readout bandwidth in the enlarged view in Fig. 1c when addressing one cell at a time. Spectral overlap is vital to dynamical multi-qubit readout as it means that both cells can be read using the same input frequency, while the degree of overlap determines the readout bandwidth of the architecture. In addition to the resonance frequency shift, we observe a reduction in the loaded quality factor Q_L from a value of 96, when both T_1 or T_2 are in the *off* state, to a value of 40, when either T_1 or T_2 are in the *on* state. An *on* state Q_L of 40 is comparable to previous experiments with [32] and without [34] control circuit.

Based on the spectra shown in Fig. 1c, we select a carrier frequency $f_c = 615$ MHz to probe the state of the quantum devices. When using RF reflectometry, changes in the complex impedance of the circuit are probed by driving the circuit close to resonance (using a small signal of -90 dBm) while monitoring the phase and magnitude of the reflected signal (see Methods for details of the circuit). Changes in the capacitance of the quantum device ΔC_G, attributed to tunneling of single electrons, are detected through changes in the reflected phase $\Delta\phi = -2Q_L\Delta C_\mathrm{G}/C_\mathrm{T}$ [35]. In Fig. 1d-e, we observe phase shift peaks as we change V_DL that corresponds to regions of charge instability in Q_i. At these voltages, single electrons cyclically tunnel between the QDs in the channel and the source or drain electron reservoirs in Q_i. For each measurement only one T_i is set to the *on* state while the other is *off*. Next, we discuss measurements focusing on a particular region of this stability diagram (highlighted in grey in Fig. 1d-e) for both quantum devices with the aim to find optimal operation voltage levels for the control transistors.

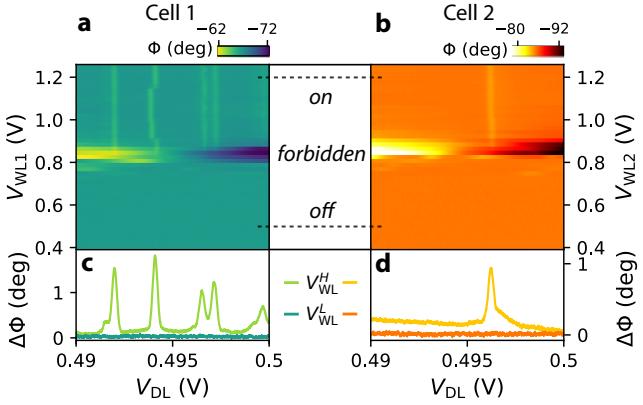

FIG. 2. **Control transistor logic states. a**, Phase response of Q_1 as a function of V_{WL1} and V_DL ($V_{WL2} = 0$ V). **b**, Phase response of Q_2 as a function of V_{WL2} and V_DL ($V_{WL1} = 0$ V). For both cells we observe QD-to-reservoir transitions at large V_WL corresponding to the logical *on* state of the digital transistor. A *forbidden* region of large background signal is found upon approaching the control FET threshold voltage. A region of no signal below threshold corresponds to the *off* state. **c-d**, Line cuts at $V_\mathrm{WL}^\mathrm{L} = 0.5$ V and $V_\mathrm{WL}^\mathrm{H} = 1.2$ V, indicated by dashed lines in (a-b), that highlight the difference between the two digital states for each device.

For a dynamical random-access readout scheme, T_i should fulfil several requirements: In the *on* state, T_i should be sufficiently conductive to allow high-sensitivity gate-based readout of the selected quantum device. In the *off* state, T_i should be sufficiently resistive to block the RF signal towards deselected cells and retain the charge on Q_i's gate for the time operations are being performed in other cells.

As a first step towards dynamically operating the circuit, we identify suitable *on* and *off* state voltages for the control FET gate (i.e. the *high*, $V_{\mathrm{WL}i}^\mathrm{H}$, and *low*, $V_{\mathrm{WL}i}^\mathrm{L}$, signal levels). In Fig. 2a-b, we show the phase of the reflected signal from the resonator as a function of V_DL and $V_{\mathrm{WL}i}$. We can identify three regions: The *on* region for $V_{\mathrm{WL}i} > 0.9$ V, where we observe single electron tunnelling, the *off* region for $V_{\mathrm{WL}i} < 0.7$ V, where we observe no transitions and finally, for $0.7\ \mathrm{V} < V_{\mathrm{WL}i} < 0.9$ V the *forbidden* region. In the latter, T_i is in the depletion regime, where, due to the voltage-dependent gate capacitance of the control FET, the phase varies largely [38]. This region should be avoided when assigning voltage levels. To highlight the different response of the resonator in the digital *on* and *off* states, we show the phase change $\Delta\phi$ as a function of V_DL for cell 1 and 2 in Fig. 2c-d, respectively, at $V_{\mathrm{WL}i}^{\mathrm{L(H)}} = 0.5(1.2)$ V.

We note the close similarity between the operation voltage levels of both T_i for addressing the quantum devices Q_i at millikelvin temperature. In a scaled up architecture, with increasing circuit complexity, reproducible electrical characteristics between cells will be essential.

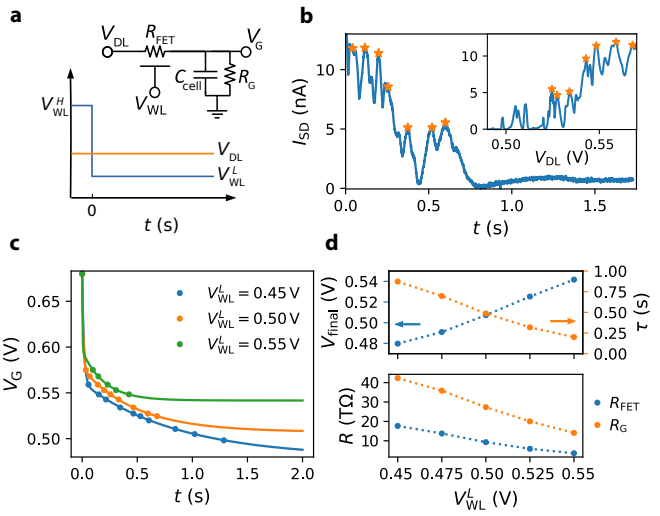

FIG. 3. **Charge retention analysis.** **a**, Equivalent circuit of a single memory cell and pulsing scheme for charge retention analysis. **b**, Source-drain current I_{SD} through the quantum device as a function of time after switching the control transistor to the *off* state $V^L_{WL} = 0.5$ V ($V_{SD} = 2$ mV, $V_{DL} = 0.68$ V). Single electron transitions are observed and peak positions are indicated by stars. The inset shows I_{SD} as a function of V_{DL} where the same transitions are observed and indicated by stars. **c**, Decay of the voltage on the QD gate V_G as a function of time once the control transistor is switched off. Data-points (circles) are obtained from the peak positions (stars) in I_{SD} and solid lines are fits to a double exponential function as described in the text. **d**, Top panel: Quasi-static gate voltage V_{final} and time constant τ as a function of V^L_{WL} obtained from the exponential decay fits (see Eq. 1). Bottom panel: R_{FET} and R_G extracted from τ and V_{final} using Eq. 1. Dashed lines are guides to the eye.

DYNAMIC OPERATION

Random access of a single cell can be achieved by switching the selected T_i *on* while all other T_j are *off*. Since the data line voltage V_{DL} is shared among the cells, the gate voltage on all deselected Q_j floats and decays over time while addressing cell i. Floating gate charge storage is an important feature of dynamic readout and its associated charge retention time sets the maximum time to perform operations on other cells before the information is lost. Charge locking is an established mechanism that is routinely used in dynamic RAM chips and it has recently been used to multiplex the access to GaAs quantum dots [39, 40]. Here, we combine charge locking with gate-based RF readout.

First, we characterise the discharge of one cell in order to determine an appropriate voltage refresh rate. We consider a simplified equivalent circuit model of the memory cell as shown in Fig. 3a. It consist of the FET *off* state channel resistance R_{FET}, the gate leakage resistance R_G, and the cell capacitance C_{cell}. R_G combines the FET and QD gate leakages and C_{cell} is the parallel sum of the QD gate capacitance C_G and the interconnect capacitance C_S, with the latter being dominant in this experiment. The voltage on the QD gate V_G decays over time as

$$V_G(t) = V_{final}\left[1 + \frac{R_{FET}}{R_G}\exp\left(-\frac{t}{\tau}\right)\right] \qquad (1)$$

when the FET is switched to the *off* state. Here $\tau = \frac{C_{cell}R_G R_{FET}}{R_G + R_{FET}}$ is the circuit time constant and $V_{final} = \frac{V_{DL}R_G}{(R_{FET}+R_G)}$ is the equilibrium voltage at the gate of the QD at $t \to \infty$. Since τ and V_{final} depend on R_{FET}, and thus on the operation voltage level V_{WL}, we proceed by investigating their functional dependence to find the optimal voltage operation point that maximises the charge retention time.

We monitor the discharge of the cell in a pulsed experiment by measuring the source-drain current I_{SD} through the QD over time. As shown in Fig. 3a, we keep $V_{DL} = 0.68$ V constant while V_{WL} switches from the *high* level (V^H_{WL}) to a *low* level (V^L_{WL}) at $t = 0$. We set the pulse amplitude to 0.5 V and vary the pulse offset ensuring that the transistor remains *on* in the *high* part of the pulse. We show an exemplary discharge measurement for $V^L_{WL} = 0.5$ V in Fig. 3b, where several single electron transitions (indicated by stars) can be observed in I_{SD} over time. After 1.5 s the current settles to a value determined by V_{final}. We compare the discharge data with a measurement of the same single electron transitions of the device as a function of V_{DL} in quasi-static conditions as shown in the inset of Fig. 3b. By matching peaks in the decay over time to peaks as a function of V_{DL} we reproduce the dynamics of the voltage on the QD gate $V_G(t)$ as shown in Fig. 3c for multiple values of V^L_{WL}. At $t = 0$, we observe an initial fast decay, possibly due to charge-injection and clock-feedthrough [41], followed by a slow decay characterised by Eq. 1. We fit a double exponential to capture the fast and slow dynamics (see Supplementary Equation 1) and extract V_{final} and τ from the slow decay which we show in Fig. 3d as a function of V^L_{WL}. We observe that as V^L_{WL} increases (R_{FET} decreases) V_{final} becomes larger due to the voltage divider characteristic of the cell. In the case of τ, we observe a reduction from 0.9 s to 0.2 s. We note that the time constant could be increased by increasing C_{cell}. The resistance values R_{FET} and R_G extracted from these measurements based on a cell capacitance $C_{cell} = 70$ fF (see Supplementary Table 1) are on the order of $10^{13}\,\Omega$. We can see that R_G increases as V_{WL} decreases which indicates that there is a V_{WL} dependent contribution towards R_G. To summarise, we find that the discharge model fits the data and shows a decrease(increase) in $\tau(V_{final})$ as V_{WL} is increased from 0.45 V to 0.55 V, as expected. Moreover, R_G and R_{FET} decrease by a factor of 3 and 5 respectively as V_{WL} increases.

While initially it may seem beneficial to select a low V^L_{WL} level to maximise τ, one needs to consider that the retention or refresh time is determined by the maximum tolerable gate voltage drop of the cell, δV, which has to

be assessed given a specific qubit implementation. For an optimised circuit with reduced crosstalk and defining the voltage drop ratio $a = \delta V/V_{\rm DL}$ and the resistance ratio $r = (R_{\rm FET} + R_{\rm G})/R_{\rm FET}$, we find that the retention time is given by $t_{\rm r} = R_{\rm G}C_{\rm cell}\ln[(1-ar)^{-1}]/r$ which is a monotonically increasing function of r, given $R_{\rm G}$ varies weakly with r. Then, $t_{\rm r}$ is maximised by operating at large $V_{\rm WL}^{\rm L}$ while remaining in the *off* regime where RF readout of the selected cell is not disturbed. Using circuit simulations we find that as long as $R_{\rm FET} > 10\,{\rm M}\Omega$, the effect of a deselected cell on the readout of a selected cell becomes negligible which is compatible with operating closely below the forbidden region shown in Fig. 2 (see Supplementary Figure 3). Additionally, we note that at $R_{\rm FET} > 10\,{\rm M}\Omega$ the fraction of the RF signal delivered to the deselected cell is $< 1\%$ due to the low-pass filter formed by $R_{\rm FET}$ and $C_{\rm cell}$ (assuming $C_{\rm cell} = 70\,{\rm fF}$ and operation at a few hundreds of MHz). Finally, given a voltage drop ratio of 1%, we estimate a retention time of 20 ms using the parameters extracted from the experiment which is much larger than the coherence time T_2^* of silicon-based electron spin qubits [10].

In this analysis, it is important to note that we keep $V_{\rm DL}$ constant which is approximately what will happen when addressing multiple quantum devices with similar operating voltages. Such operation is a particular feature of our proposal and differs from the 1T-1C DRAM read protocol where $V_{\rm DL}$ is typically set to half the maximum voltage stored in the capacitor. Such voltage level maximises the readout signal and the retention time of both the uncharged and charged memory state of the capacitor [42]. In our proposal, we operate exclusively at the charged state of Q_i. For sequential readout, as demonstrated further below, we select $V_{\rm WL}^{\rm L} = 0.5$ V ($R_{\rm FET} \approx 10^{13}\,\Omega$) to enhance the retention time in the *off* state while preserving good noise margins.

We now turn to demonstrate sequential dynamic readout of quantum devices in two memory cells. We show the pulsing scheme to dynamically read both memory cells in Fig. 4a. In the first half of the cycle, from 0 to 12 ms, we set T_1 and T_2 to the digital *on* and *off* states respectively. Simultaneously, we apply an analogue signal to the common data line $V_{\rm DL}$ (blue trace) that ramps up the gate voltage on the data line (now connected to Q_1). We read the signal dispersively using gate-based readout and detect peaks in the phase due to single-electron transitions between a QD and a reservoir in Q_1. In the second half of the cycle, from 12 to 24 ms, we invert the digital voltages on T_1 and T_2 such that we can now detect the transitions in Q_2 as we ramp down the analogue signal on the data line. The QD-to-reservoir transitions in the phase response are identical to those measured in a static experiment shown in Fig.1d-e. The RF modulation frequency and amplitude is kept constant throughout the measurement. There is a phase offset between the signal detected from Q_1 and Q_2 due to a small difference in reflection coefficient between cells (see Fig. 1c). We therefore show the change in phase $\Delta\phi$ in Fig. 4a (see also Supplementary Figure 2). We obtain a signal-to-noise ratio (SNR) of 10^5 with 100 ms integration time.

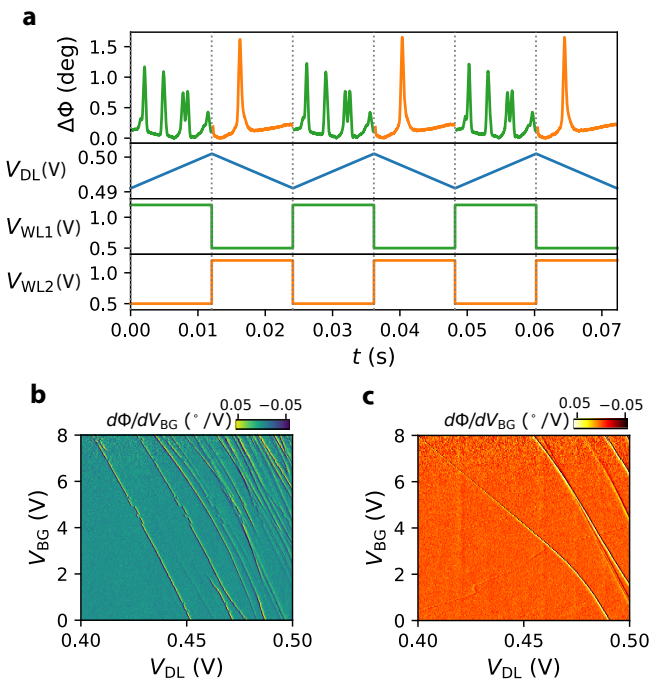

FIG. 4. **Dynamic readout. a**, Pulse scheme for sequential readout and phase response of Q_1 and Q_2. $V_{\rm DL}$ is ramped up and down while $V_{\rm WL1}$ and $V_{\rm WL2}$ are alternating between *high* and *low* states. Pulses are synchronised such that QD reservoir transitions from Q_1 are obtained when $V_{\rm DL}$ is ramped up while Q_2 is measured when $V_{\rm DL}$ is ramped down. **b-c**, Differential phase response obtained sequentially from both cells as a function of data line and back-gate voltages.

Using this interleaved pulsing scheme for sweeping $V_{\rm DL}$ combined with additional stepping of $V_{\rm BG}$ after each cycle, we obtain the charge stability map of both Q_1 and Q_2 sequentially as shown in Fig. 4b-c. The transitions observed in the measurement suggest formation of multiple QDs in both cells (see Supplementary Figure 1 for additional scans), i.e. corner dots [36]. We estimate a maximum power dissipation of $P = C_{\rm FET}f_{\rm op}\Delta V^2 = 25\,{\rm nW/cell}$ when operating at maximum readout bandwidth ($f_{\rm op} = 13$ MHz, $\Delta V = 0.7\,{\rm V}$, $C_{\rm FET} = 4$ fF). However, due to filtering of the lines delivering the control FET signals $V_{\rm WL1,2}$ and data line signal $V_{\rm DL}$, $f_{\rm op}$ was limited to 1 kHz in this demonstration (see Supplementary Figure 2).

INTEGRATED DESIGN AND SCALING UP THE ARCHITECTURE

An integrated design of the readout architecture requires a careful analysis of the relevant circuit parameters and their effect on chip footprint and readout SNR. To simulate performance of the architecture, we put for-

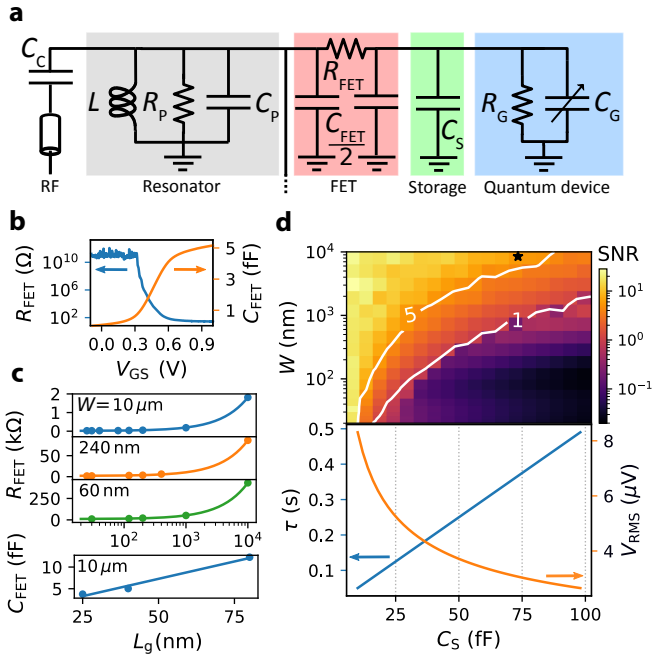

FIG. 5. **Integration.** **a**, Complete circuit model of a single cell composed of the resonator, control FET, storage capacitor and quantum device. The dotted wire indicates the connection to a subsequent cell. **b**, Exemplary resistance and capacitance measurement of a control FET of width $W = 10\,\mu$m and $L_g = 40$ nm at 4 K with turn on at $V_{GS} = 0.5$ V. **c**, Measurements at 4 K (circles) and fit to a model (solid line) of the *on* state capacitance and resistance of FETs with different width W as a function of gate length L_g. **d**, The top panel shows the calculated SNR based on the circuit model with the FET in the *on* state, $L = 400$ nH, $C_p = 480$ fF and R_p=800 kΩ as a function of C_S and W for $L_g = 20$ nm. The black star represents the configuration of the experiment. The bottom panel shows estimations of thermal noise (assuming a temperature of 50 mK) and circuit time constant with the FET in the *off* state.

ward an equivalent circuit of a single cell based on the discharge model in Fig. 3a which we expand to the RF domain (see Fig. 5a). The model consists of a readout resonator (inductance L, capacitance C_p and resistive losses R_p), the control FET (channel resistance R_{FET} and gate capacitance C_{FET}, split equally between source and drain), a charge storage capacitor C_S and the quantum device with state dependent gate capacitance C_G and resistance R_G, respectively [43]. To permit direct integration of classical and quantum devices, the classical control circuit should not exceed critical dimensions of the quantum circuit. In case of a dense array of silicon-based quantum dot qubits, the pitch should be smaller than 100 nm to allow exchange based two qubit gates [44]. Here we give clear guidelines of the circuit values that would enable such integration.

To estimate the dependence of the readout SNR on cell parameters, we first consider the signal to be measured, i.e. the change in quantum device capacitance when electrons tunnel. For quantum dots with a tunnel coupling $\Delta_c = 20\ \mu$eV and lever arm $\alpha = 0.5$, C_G changes by $\Delta C_G = 1$ fF [37] from its geometrical value of ≈ 10 aF, when tunnelling is allowed. Based on the dynamic operation results, we assume R_G is much greater than the impedance of the gate capacitance and can be treated as infinite. Turning to the control FET, we characterise multiple devices of different channel widths W and gate lengths L_g at 4 K to extract the channel resistance and gate capacitance. In Fig. 5b, we show an exemplary measurement of the dependence of these parameters with gate voltage (V_{GS}) for a transistor with $W = 10\ \mu$m and $L_g = 40$ nm and, in Fig. 5c, how the *on* state values depend on device dimensions. From these measurements we generate a model for R_{FET} and C_{FET} as a function of W and L_g (see Supplementary Equations 5&6) and perform circuit simulations assuming a well-matched high-Q RF resonator ($f_c = 310$ MHz and $Q \approx 400$) [35].

The SNR depends on multiple circuit components but here we study its dependence with the parameters that affect the physical dimensions of the cell most significantly: W and C_S. Figure 5d shows the simulated SNR for an integration time of 4 μs (much shorter than the coherence time of electron spins in ^{28}Si, $T_2^* \approx 100\ \mu$s), a noise temperature of 4 K and an optimised applied power at each data point. The SNR decreases as W decreases (*on* state R_{FET} increases) - this can be compensated by decreasing C_S, but only at the cost of reducing the time constant (τ) and increasing the RMS thermal noise voltage (see Fig. 5d). In balancing these various requirements to optimise for C_S, it is also important to consider the capacitor footprint. In DRAM, a storage capacitance of $C_S = 10 - 25$ fF is required to achieve a refresh time in the range of milliseconds. DRAM cells have been continuously scaled down while maintaining a total footprint of $6F^2$ by using trench or stacked capacitors with exotic high-k dielectrics and large capacitor aspect ratios where F is the minimum feature size currently reaching sub 10-nm [45]. We can therefore identify an example set of parameters ($W = 100$ nm, $C_S = 25$ fF) which can fit within an approximate 100 x 100 nm^2 footprint, commensurate with a QD pitch in a dense array, and still obtain SNR > 1 (see Supplementary Figure 6 and Supplementary Table 2). For these parameters thermal noise increases towards 5 μV – comparable to the precision and noise of common low noise voltage sources ($1 - 10\,\mu$V) – and the RC time constant decreases to 0.1 s, which is sufficient for a regular refresh of gate voltages. If longer retention time, better voltage stability (drift and noise) at the same SNR and readout bandwidth is desired, or even higher SNR and readout bandwidth, then the control circuitry requires a larger transistor or capacitor footprint; unless further advance in low *on* state resistance transistors or compact storage capacitors are made. Alternatively, the SNR can be improved by increasing the frequency of operation, the Q_L of the resonator, or using quantum-limited amplifi-

cation [35, 46, 47]. Moreover, requirements on critical dimensions could be relaxed depending on the architectural implementation, which could range from $< 100\,\mathrm{nm}$ for dense arrays using direct exchange to $< 400\,\mathrm{nm}$ when using mediated exchange via an intermediate state [48] or even $1-1000\,\mu\mathrm{m}$ when using sparse qubit arrays and long distance coupling via capacitive couplers, spin shuttles or superconducting resonators [30].

Our strategy for extending this demonstration to a large scale array builds on ideas that have appeared in the literature [29–31] by combining sequential gated readout with frequency multiplexing techniques [49] allowing addressing of an $N \times M$ array (see Supplementary Figure 4). There is a potential for the required inductors to be integrated and CMOS compatible using TiN. The footprint of such inductors can be reduced when operating at higher frequencies, using small critical dimensions and kinetic inductance (see Supplementary Information on control circuit footprint). Additionally, we envision to apply this strategy to a double QD split-gate architecture (see Supplementary Figure 5) where manipulation and readout signals are applied to different gates [50].

CONCLUSION

We have reported a CMOS dynamic random access architecture for radio-frequency readout of QD devices at millikelvin temperatures. We show sequential dispersive readout of individual quantum devices in a two-cell layout, which is an important step in being able to address larger arrays. We find opposing requirements between SNR, charge retention and circuit footprint when analysing scaling towards an integrated design. Our results provide guidelines to find a compromise between the desired measurement bandwidth, voltage drift, noise tolerances and critical dimensions, which can be different for a given qubit implementation. We find exemplary circuit values that can allow the desired level of integration for a particular implementation. Further work towards circuit optimisation could include cross-talk mitigation, adaptation of our circuit model to integrated circuit design, and creation of high quality superconducting inductors with reduced footprint.

METHODS

Fabrication details

All CMOS transistors used in this study were fabricated on SOI substrates with a 145-nm-thick buried oxide and 10-nm-thick silicon layer. The silicon layer is patterned to create the channel by means of optical lithography, followed by a resist trimming process. All transistors share the same gate stack consisting of 1.9 nm HfSiON capped by 5 nm TiN and 50 nm polycrystalline silicon leading to a total equivalent oxide thickness of 1.3 nm. The Si thickness under the HfSiON/TiN gate is 11 nm. After gate etching a SiN layer (10 nm) was deposited and etched to form a first spacer on the sidewalls of the gate. 18-nm-thick Si raised source and drain contacts were selectively grown before the source/drain extension implantation and activation annealing. A second spacer was formed followed by source/drain implantations, activation spike anneal and salicidation (NiPtSi). The wide channel control FETs T_i and nanowire quantum devices Q_i are connected via on-chip aluminium bond wires.

Measurement setup

Measurements were performed at base temperature of a dilution refrigerator (15 mK). Low frequency signals (V_{SD}, V_{DL}, $V_{\mathrm{WL1,2}}$) were delivered through filtered cryogenic loom while a radio-frequency signal for gate-based readout was delivered through an attenuated and filtered coaxial line which connects to a on-PCB bias tee combining the RF modulation with V_{DL}. The resonator is formed from a 82 nH inductor and the sample's parasitic capacitance to ground in parallel with the device. The inductor consists of a surface mount wire-wound ceramic core (EPCOS B82498B series) and the PCB is made from 0.8 mm thick RO4003C with immersion silver finish. The reflected RF signal is amplified at 4 K (LNF-LNC0.6_2A) and room temperature followed by quadrature demodulation (Polyphase Microwave AD0540B) from which the amplitude and phase of the reflected signal is obtained (homodyne detection).

DATA AVAILABILITY

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

S.S. and M.F.G.-Z. devised the experiment. S.S., A.R. and M.F.G.-Z. performed the experiments; S.B. fabricated the sample; V.N.C.-T and T.-Y.Y. performed measurements for low-temperature modelling; V.N.C.-T developed and performed simulations towards integration; S.S. did the analysis and prepared the manuscript with contributions from A.R., J.J.L.M. and M.F.G.-Z.

COMPETING INTERESTS

The authors declare no competing interests.

READOUT RESONANCE AND CELL PARAMETERS

We present the resonant frequency f_0, the frequency shift Δf, the total capacitance C_T and the loaded quality factor Q_L in Supplementary Table 1 extracted from Fig. 1b of the main text for each control FET configuration.

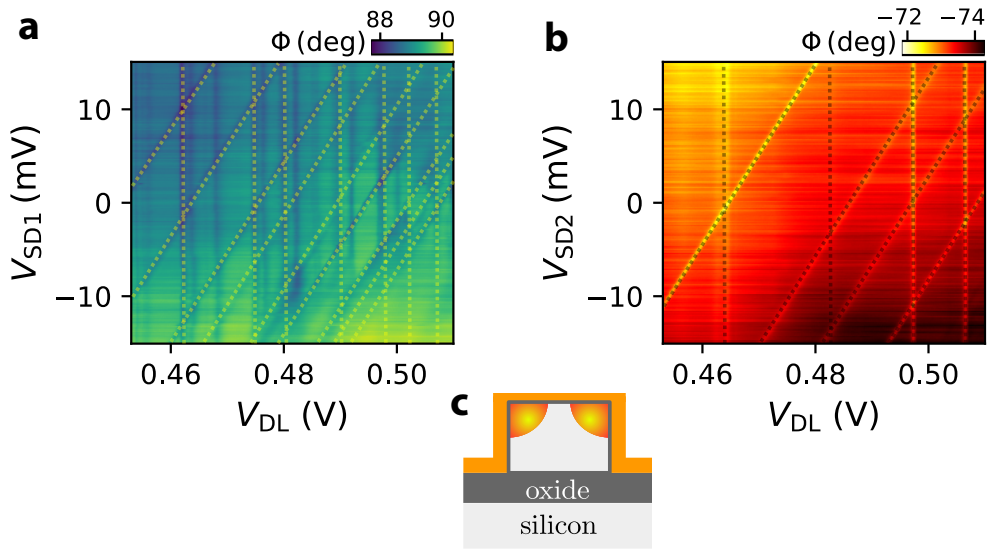
FET state: T_1-T_2	f_0 (MHz)	Δf (MHz)	Q_L	C_T (fF)	C_cell (fF)	C_FET (fF)	C_S (fF)
off-off	645.9	0	96	740	0	0	0
on-off	618.3	27.3	39	808	68	4	64
off-on	616.7	29.2	40	812	72	5	67
on-on	593.0	52.9	28	878			

Supplementary Table 1: Two-cell spectral parameters. f_0 is the centre frequency, Δf is the resonant frequency shift, Q_L the loaded quality factor and C_T the total circuit capacitance obtained using a nominal inductance of 82 nH. C_cell is the capacitance added by a single cell being selected via a control FET which is composed of the FET channel capacitance C_FET and storage capacitance C_S.

By comparing the total capacitance between different cases we can extract the cell capacitance C_cell which we model to be composed of the FET channel capacitance C_FET and the interconnection and storage capacitance C_S. We obtain C_FET from geometric estimations and measurements (shown in Fig. 5c of the main text) from which we extract C_S. We find that most of the additional capacitance causing the frequency shift can be attributed to interconnection between T_i and Q_i.

SEQUENTIAL MEASUREMENT OF COULOMB DIAMONDS

In addition to the sequential measurement as a function of top-gate and back-gate as shown in Fig. 4 of the main text we here present a sequential measurement of both cells as a function of top-gate and source-drain voltages. In Supplementary Figure 1 we observe Coulomb diamonds compatible with formation of multiple quantum dots in both quantum devices. In these devices, quantum dots form in the corners of the silicon nanowire as indicated in the side-view along the top-gate.

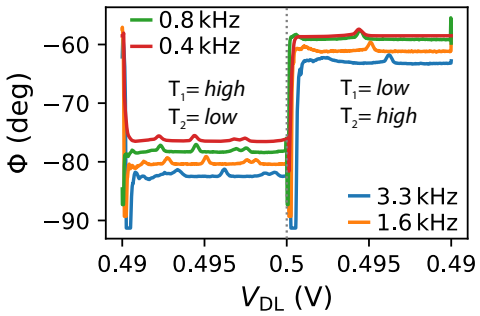


Supplementary Figure 1: Dynamic readout. a-b, Additional measurement as shown in Fig. 4 of the main text. Phase response obtained sequentially from both cells as a function of source-drain and top-gate voltages. Coulomb diamonds are observed and highlighted using dashed lines. **c**, Side view of the quantum device along the top-gate showing formation of corner quantum dots.

FILTERING LIMITATIONS AND POWER DISSIPATION

In this section we analyze the impact of low-pass filtering of lines delivering the control FET switching voltages $V_{\mathrm{WL}i}$ and data-line voltage V_{DL}. Supplementary Figure 2 shows a sequential measurement as shown in Fig. 4 of the main text where V_{DL} is ramped up and down while V_{WL1} and V_{WL2} are alternating between *on* and *off* states at the same frequency. Multiple traces represent measurement for increasing frequency and traces are offset for clarification. For measurements above 1 kHz we observe a significant impact of the filtering on the rise time of the pulses representing the frequency limit for sequential readout in this experiment. By using coaxial lines for delivering $V_{\mathrm{WL}i}$ and V_{DL} the operational frequency could be increased until the limiting factor becomes excessive device heating caused by fast switching.

We can estimate heating limitation using the dynamic power $P = C_{\mathrm{FET}} f_{\mathrm{op}} \Delta V^2$ when switching one control FET T_i, where $\Delta V = V_{\mathrm{WL}}^{\mathrm{H}} - V_{\mathrm{WL}}^{\mathrm{L}}$, C_{FET} is the overall capacitance subject to the voltage swing ΔV and f_{op} is the switching frequency. The maximum f_{op} is given by the readout bandwidth of the architecture and we estimate C_{FET} using geometric capacitance of



Supplementary Figure 2: Filter limit. Phase response obtained in a dynamic readout experiment as shown in Fig. 4 of the main text for increasing control transistor switching frequency. There is a significant rise time of the pulses above 1 kHz due to low-pass filtering of the lines. Traces are offset for clarity.

T_i. Given our selection of $\Delta V = 0.7$ V, the readout bandwidth 13 MHz and $C_{\mathrm{FET}} = 4$ fF in the experiment, we estimate 25 nW/cell which will allow operating 16,000 cells simultaneously when pulses are generated at mK. The power dissipation can be reduced by pushing the voltage levels closer to the *forbidden* region (e.g. $\Delta V = 0.4$ V), thus reducing the noise level margins, or using smaller control FET dimensions. If pulse generation would not be feasible at mK based on current technology or heating budget, pulses could be generated at a higher stage (e.g. 4 K) where higher cooling power is available, however this might increase the capacitance subject to the voltage swing.

DISCHARGE OF THE MEMORY CELL & FITTING PROCEDURE

In this section we explain the fitting procedure used to fit the decay of $V_{\mathrm{G}}(t)$ as a function of time as shown in Fig. 3c of the main text. We observe an initial fast decay from $V_{\mathrm{G}}(0) = 0.68$ V followed by a slow decay with a quasi static final gate voltage once the control FET gate voltage is switched from V_{WL}^{H} (1.2 V) to V_{WL}^{L}. We attribute the slow decay to discharge via the control FET (R_{FET}) and other leakage paths R_{G} (e.g. gate dielectric, see equivalent circuit in Fig. 3a of the main text). The fitting function consist of Eq. 1 of the main text parametrising the slow decay in addition to an initial fast decay

$$V_{\mathrm{G}}(t) = V_{\mathrm{final}}\left[1 + \frac{R_{\mathrm{FET}}}{R_{\mathrm{G}}}\exp\left(-\frac{t}{\tau}\right)\right] + V_{\mathrm{fast}}\exp\left(-\frac{t}{\tau_{\mathrm{fast}}}\right) \tag{1}$$

with $\tau = \frac{C_{\text{cell}} R_{\text{FET}} R_{\text{G}}}{R_{\text{FET}}+R_{\text{G}}}$ being the circuit's time constant and $V_{\text{final}} = \frac{V_{\text{DL}}}{(R_{\text{FET}}+R_{\text{G}})/R_{\text{G}}}$ the final quasi static voltage.

We assume a decay starting from the set-point of $V_{\text{G}}(0) = 0.68$ V and the results for V_{final} and τ are shown in Fig. 3d of the main text. We extract a time constant on the order of one milli-second for the fast decay and an amplitude of ≈ 0.1 V which we attribute to charge injection and clock-feedthrough. There is limited data available right after $t = 0$ since we need to match oscillations in the discharge to oscillations in the turn on characteristic, the time constant of the fast discharge τ_{fast} is only an estimate extracted from the fit and hence should be treated as an upper bound.

We estimate the effect of charge injection by calculating the amount of charge in the control FET channel which is escaping onto the quantum device gate when the charge in the FET is depleted: $\Delta V_{\text{CI}} = \frac{Q_{\text{channel}}}{2C_{\text{cell}}} = \frac{C_{\text{FET}}(V_{\text{WL}}^{\text{H}} - V_{\text{DL}} - V_{\text{th}})}{2C_{\text{cell}}} \approx 0.02\,\text{V}$ where C_{FET} is the gate capacitance of the FET and C_{cell} is the cell capacitance. Here, the factor of $1/2$ accounts for the assumption that the charge under the gate escapes equally to the source and drain which can be different in a real device. We calculate clock-feedthrough based on an estimation of the capacitance between gate and source C_{GS}. Due to unconventionally long gate spacers (25 nm), designed to create tunnel barriers to the source and drain access regions, we expect the contribution from direct overlap to be negligible. Fringing gate capacitance is likely to be the dominant parasitic contribution to clock-freedthrough. A fringing capacitance of 33% of the FET gate capacitance is observed for transistors of dimensions $W = 0.15\,\mu$m and $L_{\text{g}} = 60\,$nm [1]. For a transistor with $W = 10\,\mu$m and $L_{\text{g}} = 30\,$nm we therefore estimate $C_{\text{GS}} \approx C_{\text{FET}}/2$ which results in a voltage shift of $\Delta V_{\text{CF}} = \frac{C_{\text{GS}}}{C_{\text{GS}}+C_{\text{cell}}} \left(V_{\text{WL}}^{\text{H}} - V_{\text{WL}}^{\text{L}}\right) = 0.013\,\text{V}$. This yields an overall voltage shift of $\Delta V \approx 0.033\,\text{V}$. The amplitude of the fast decay observed in Fig. 3 is larger and we note that the amount of injected charge depends on the specific *on* and *off* state word line voltages. Further cross-talk in the lines, PCB as well as the device could have an additional contribution to the fast decay. To minimise the effect of such cross-talk on the analysis of the slow decay, the pulse amplitude in the measurement presented in Fig. 3 of the main text is kept constant and the offset is varied to produce different *low* levels while keeping the *high* level above threshold.

Finally, we note that the voltage shift due to charge injection and clock-feedthrough is reduced for smaller C_{FET} and larger C_{cell} and charge injection can be mitigated using a slow fall time of the clock or using one NMOS and one PMOS control FET in parallel where

the geometry of both can be optimised such that a negative voltage jump introduced when switching off the NMOS FET is cancelled by a positive voltage change due to switching of the PMOS FET. Usually a PMOS transistor of larger width is required due to the lower mobility. Alternatively, a dummy transistor in series with the control FET with approximately half the transistor width and opposite clock yields similar results. Furthermore, additional cross-talk can be reduced by using coaxial lines to deliver control FET signals and careful PCB and chip design.

SNR SIMULATIONS

In gate-based RF reflectometry, quantum dot devices are read-out by detecting small changes in the capacitance of the quantum device associated with the tunnelling of single electrons. This is achieved by embedding the device in a resonant circuit and monitoring changes in the complex impedance of the reflected signal when driven close to resonance. We perform simulations of the reflected signal to estimate readout performance when scaling the random access architecture.

The circuit model considered in these simulations can be found in Fig. 5a of the main text and the reflection coefficient is given by

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{2}$$

where Z_0 is the line impedance and Z is the circuit impedance. The absolute change in Γ to a given capacitive change ΔC_{G} in the state dependent capacitance C_{G} is then

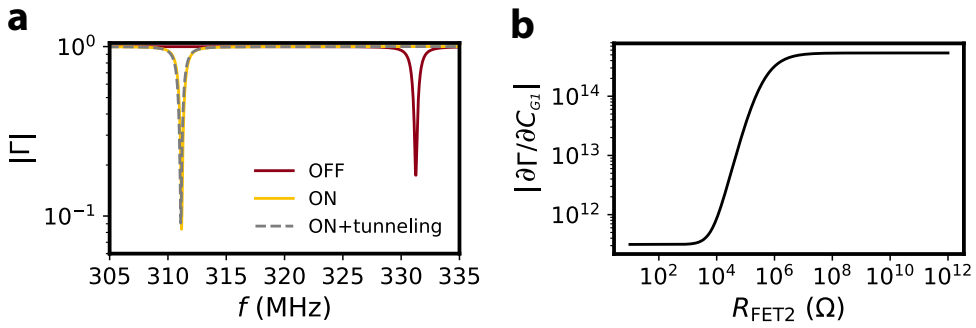
$$|\Delta\Gamma| = \left|\frac{\partial\Gamma}{\partial C_{\mathrm{G}}}\Delta C_{\mathrm{G}}\right| \propto Q_{\mathrm{load}}\frac{\Delta C_{\mathrm{G}}}{C_{\mathrm{T}}} \tag{3}$$

which will be proportional to the loaded quality factor and capacitive change compared to the overall circuit capacitance. The signal-to-noise ratio is

$$\mathrm{SNR} = |\Delta\Gamma|^2\frac{P_c}{P_N} \tag{4}$$

where P_c is the input drive power and P_N is the noise power.

In the experiment demonstrated in the main text, readout sensitivity was limited by the low quality factor. For the SNR simulations, we use recent improved experimental parameters



Supplementary Figure 3: Readout simulations. **a**, Demonstration of our simulation model with $C_{\mathrm{c}} = 90\,\mathrm{fF}$, $C_{\mathrm{p}} = 480\,\mathrm{fF}$, $C_{\mathrm{S}} = 70\,\mathrm{fF}$, $R_{\mathrm{p}} = 800\,\mathrm{k\Omega}$, $L = 405\,\mathrm{nH}$. Traces show cell not being addressed (red), addressed (yellow) and addressed when electrons tunnel in the device (dashed grey). A frequency shift similar to the experiment is observed. **b**, Effect of the *off* state resistance of a second cell R_{FET2} on the sensitivity of the reflection coefficient to changes in the quantum dot gate capacitance C_{G1} of cell 1.

where higher quality factors of $Q_{\mathrm{load}} = 400$–800 are achieved using superconducting spiral inductors [2]. Currently these inductors still reside off-chip but there is a potential for such inductors to be made CMOS compatible using TiN allowing on-chip integration. The footprint of such inductors can be reduced when operating at higher frequencies, using smaller critical dimensions or making use of kinetic inductance. We verify that the model reproduces the features observed in the experiment. In Supplementary Figure 3 we observe that as the control FET is turned on (R_{FET} small), the resonant frequency of our model shifts to lower frequency due to the additional cell capacitance. Small additional changes due to tunnelling in the quantum device lead to further shifts which we aim to detect.

To asses the effect of SNR as a function of the circuit parameters, we calculate the reflection coefficient and SNR as given above. To relate this to circuit dimensions, we performed measurements of transistors of different width W and gate length L_{g} (see Fig. 5c of the main text) and have developed the following model

$$R_{\mathrm{FET}} = a \cdot \frac{L_{\mathrm{g}}}{W} + b \cdot \frac{1}{W} \tag{5}$$

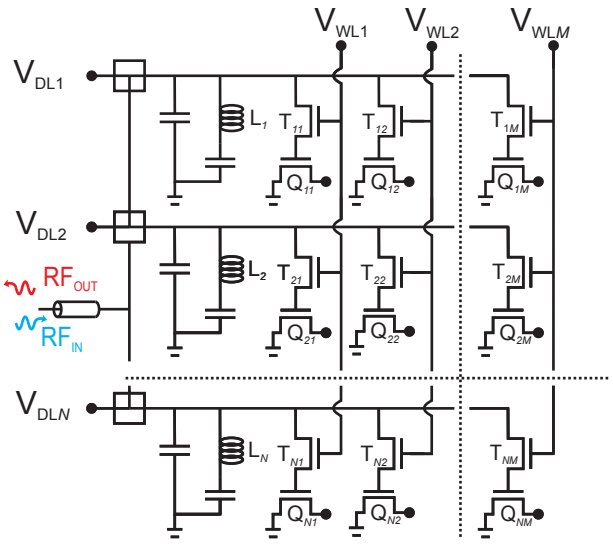
$$C_{\mathrm{FET}} = \frac{\varepsilon_r \varepsilon_0 (2H + W) L_{\mathrm{g}}}{1.87 \cdot d_{\mathrm{ox}}} \tag{6}$$

with $a = 2503 \pm 80\,\Omega$ and $b = 603 \pm 26\,\mathrm{k\Omega nm}$ and $H = 10\,\mathrm{nm}$ being the nanowire thickness.

The factor of 1.87 accounts for the dark space where the barycentre of the 2DEG is formed about 1.1 nm beneath the oxide-silicon interface.

To obtain the SNR, we choose an inter-charge-transition of a double quantum dot with tunnel coupling $\Delta_c = 20\,\mu$eV and gate coupling $\alpha = 0.5$ as an example. This gives a capacitive shift of $\Delta C_{\mathrm{G}} = \frac{(\alpha e)^2}{2\Delta_c} = 1\,$fF. The simulations in Fig. 5d of the main text show the dependence of the SNR on the most significant parameters for scaling, W and C_{S}, and include optimisation of the coupling capacitor C_{c} for each combination to achieve optimal matching between the resonator and the line. Additionally, the maximum input power below broadening is recalculated for each point due to a reduction of quality factor of the resonator and $R_{\mathrm{FET}}C_{\mathrm{S}}$-filter amplitude reduction for larger C_{S} and smaller W. The values range from $P_c = -124\,$dBm to $P_c = -92\,$dBm. We note that the SNR increases monotonically as L_{g} decreases due to a reduction in C_{FET} and we select $L_{\mathrm{g}} = 20\,$nm in Fig. 5d.

To estimate the effect of other cells on the readout of a selected cell, we simulate a circuit as shown in Fig. 5a but with an additional cell consisting of a second control FET, storage capacitor and quantum device connected to the same resonator as indicated by the dashed line in Fig. 5a. We evaluate the sensitivity of the reflection coefficient to changes of the quantum device capacitance of cell one, C_{G1}, as a function of the *off* state resistance of the control FET of cell two, R_{FET2}. As shown in Supplementary Figure 3b, we find that as long as $R_{\mathrm{FET2}} > 10\,\mathrm{M}\Omega$, the effect on the readout of the first cell becomes negligible. This is an important feature because we find that retention time can be enhanced when operating at a small FET *off* state resistance (large $V_{\mathrm{WL}}^{\mathrm{L}}$) which is large enough to block any readout of a deselected cell given that the data-line voltage is very similar for different cells. By comparing with the FET resistance measurement shown in Fig. 5b of the main text we can define an upper limit for $V_{\mathrm{WL}}^{\mathrm{L}}$ and we find that $R_{\mathrm{FET2}} > 10\,\mathrm{M}\Omega$ is compatible with operating closely below the forbidden region $V_{\mathrm{WL}}^{\mathrm{L}} < 0.7\,$V indicated in Fig. 2 of the main text. In the main text, we additionally estimate an *off* state resistance of $R_{\mathrm{FET}} = 10^{13}\,\Omega$ from the experimental discharge of a cell at $V_{\mathrm{WL}} = 0.5\,$V, which should not disturb readout of another cell.



Supplementary Figure 4: Large scale array. A $N \times M$ 2D array of single electron memory cells for sequential multi-qubit readout. Control transistors T_{ij} can be controlled by word line voltages $V_{\mathrm{WL}j}$. Qubits Q_{ij} can be controlled with data lines voltages $V_{\mathrm{DL}i}$. A single high-frequency line allows simultaneous readout via frequency-multiplexed RF reflectometry.

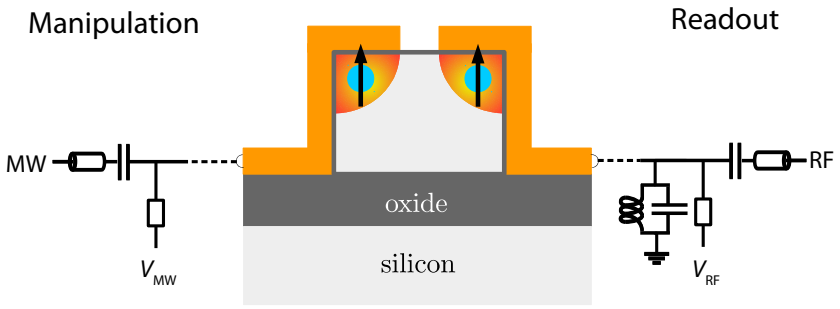
LARGE SCALE ARRAY

A large scale array can be constructed by employing sequential access combined with known frequency multiplexing techniques as proposed in literature [3, 4]. As shown in Supplementary Figure 4, such a two dimensional array is distributed in rows (i) and columns (j). A specific qubit in row i and column j, Q_{ij}, can be addressed by a word line $V_{\mathrm{WL}j}$, that controls the voltage on the gate of transistor T_{ij}, and by a data line voltage $V_{\mathrm{DL}i}$, that controls the gate potential on the qubit. Additionally, each row is connected to a different LC resonator for readout which is formed by the parasitic capacitance and inductor in parallel to each data-line. Each inductor is RF-grounded via a capacitor and distinct resonant frequencies f_i are achieved using different values for the inductance of each resonator L_i. Multiple resonators can be probed simultaneously using frequency multiplexing techniques [4] such that the whole array only requires a sole high-frequency line for readout which is connected to the data-lines via a bias-tee. The array can be operated dynamically in a random access manner. When a specific word line j' is activated qubits $\mathrm{Q}_{ij'}$ can be read simultaneously for all i or their gate voltages are refreshed using the specific data line voltages $V_{\mathrm{DL}i}$. Each qubit may be fabricated such that it is in close proximity to other qubits to perform two-qubit

operations [5, 6]. This possibility is indicated by the circular connection at the source of each quantum device. The array particularly suits one dimensional chains of interacting quantum devices such as they are distributed along the rows of the array [7–9]. The array can be extended in number of rows and columns limited by the spectral overlap of the data-line resonators and typical readout and retention time.

COMBINED READOUT AND CONTROL

The large scale architecture discussed in the previous note can be applied to different types of qubit implementations. The quantum devices presented in the manuscript, i.e. nanowire transistor devices with a single wrap-around gate, are a model system to benchmark the readout using dot-to-reservoir transitions. Such single-gate devices require control and readout pulses to be delivered via the same line. The resonator limits the rise time of control pulses. As long as the resonator bandwidth (here 13 MHz) is much larger than the inverse coherence time of the system (e.g. $1/T_2^* = 1/100\,\mu\text{s} = 10\,\text{kHz}$ for spin qubits in ^{28}Si) the readout gate can used for manipulation on timescales faster than the coherence time.



Supplementary Figure 5: Readout and control. Split-gate device based on a nanowire transistor as discussed in the main text. Splitting of the gate allows for individual control of the corner quantum dots and separation between manipulation and readout signals.

We envision a split-gate architecture as shown in Supplementary Figure 5 which is based on the same SOI nanowire transistor technology as the devices presented in the main text. However, the gate is split in the centre allowing individual control of each corner quantum dot. Such a double quantum dot system allows readout based on Pauli spin-blockade which is one of the most promising and scalable approaches as it does not require an electron

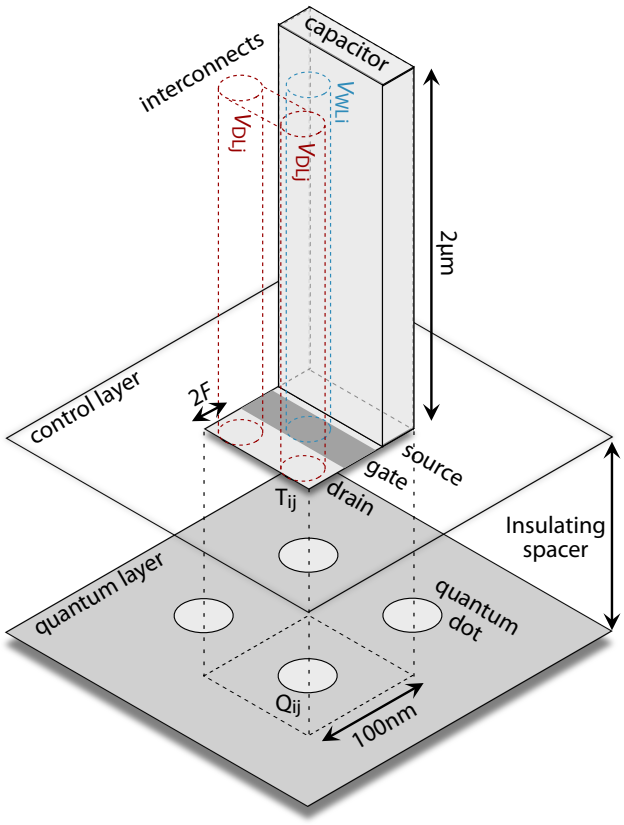
reservoir near the quantum dot [10]. Moreover, the two gates offer a way to separate signals for readout from manipulation signals which can have different bandwidth requirements. Thus, one gate serves as the manipulation gate while the other is used for RF readout via an LC resonator. The dotted lines indicate a possibility of separate random access circuits for each gate as presented above in case of the readout.

CONTROL CIRCUIT FOOTPRINT

In order to integrate quantum devices with classical control circuits, it is important to estimate the classical circuit footprint and compatibility with the critical quantum device pitch which may depend on the architectural implementation. As discussed in Section IV of the main text, we consider the example of a dense qubit array with a pitch of 100 nm and discuss the feasibility of fabricating the control circuit consisting of a control FET and storage capacitor within a footprint of $100 \times 100\,\mathrm{nm}^2$. In the main text we identify a combination of control transistor of width $W = 100\,\mathrm{nm}$ and length $L_g = 20\,\mathrm{nm}$ and storage capacitance $C_\mathrm{S} = 25\,\mathrm{fF}$ which yields a SNR > 1 with 4 μs integration time, thermal voltage noise $V_\mathrm{RMS} = 5\,\mu\mathrm{V}$ and RC time constant of 0.1 s. In Supplementary Figure 6 we estimate the footprint of such a combination of control transistor and capacitor and compare with the critical dimensions of the quantum devices.

We consider one layer for the quantum devices Q_{ij} and a second layer for the control FETs T_{ij}. The quantum layer shows four quantum dots with a pitch of 100 nm. For clarity, the control layer shows the circuit of a single cell only, consisting of the drain, gate and source electrode of the control FET, a storage capacitor represented by a cuboid of large aspect ratio and multiple interconnects.

Fabrication of the control circuit at the density shown in Supplementary Figure 6 seems feasible at the 10 nm or 14 nm technology node (for example) and using DRAM 1x nm technology. We account for a capacitor footprint of $\approx 12F^2$ (where F is the minimum feature size for a given technology) and an aspect ratio of up to 100 which should allow for fabrication of a 25 fF capacitor when comparing with the overall cell size (of $6F^2$ – which includes capacitor, transistor and bit-line) in current DRAM technology. To accommodate larger storage capacitance (e.g. to achieve longer retention with reduced SNR at same transistor width) or if additional dummy transistors for mitigation of charge injection are



Supplementary Figure 6: Circuit footprint. Schematic layout of the control circuit required for sequential readout with quantum device layer for comparison (100 nm pitch quantum device pitch).

desired (as discussed in the discharge analysis of the memory cell) a second control layer can be considered. For a quantum device pitch below 100 nm advances in low *on* state transistors and compact storage capacitors are required in order to maintain the same SNR and voltage stability. Further scaling towards smaller gate pitch might be necessary for a quantum device pitch approaching 50 nm.

Finally, we estimate the required footprint when integrating inductors on-chip. TiN, already present in recent gate-stacks in CMOS processes, is a good candidate for achieving high quality inductors at small footprint. When reducing dimensions, kinectic inductance can dominate over geometric inductance in superconducting films. In 30-nm-thick TiN films a kinetic inductance of 22.2 pH/sq is observed [13]. Based on this we estimate that 133 pH/sq could be achieved in a 5-nm film. A 5-nm-thick, 50-nm-wide and 19 μm-long wire then yields an inductance of 50 nH, compatible with high-frequency operation of gate-based RF

technology	interconnect/metal pitch	gate pitch	fin pitch	developments
14 nm	52 nm	70 nm	42 nm	air gaps
10 nm	36 nm	54 nm	34 nm	contact over active
technology	DRAM C_S	DRAM cell area	DRAM aspect ratio	developments
1x nm	8–12 fF[a]	$6F^2$	50–100[a]	towards $4F^2$ area

[a] Depending on manufacturer

Supplementary Table 2: Fabrication limits. Characteristic parameters for the 14 nm and 10 nm technology nodes and DRAM 1x nm technology [11, 12].

reflectometry readout as shown in the main text. While such an inductor still requires a substantial footprint, sequential access, as demonstrated in the main text, significantly reduces the number of inductors required to readout a large scale array (see large scale array discussion).

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