# Single-Stage and Multiplicative Distributed Amplifiers for 200GHz+ Amplification

Temitope Odedeyi[#1], Stavros Giannakopoulos[*2], Herbert Zirath[*3], Izzat Darwazeh[#4]
[#]Department of Electronic and Electrical Engineering, University College London, London UK
*Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology, Göteborg Sweden
{[1]temitope.odedeyi.13, [4]i.darwazeh}@ucl.ac.uk, {[2]stagia, [3]herbert.zirath}@chalmers.se

***Abstract*—In this paper, we review the merit of the single stage distributed amplifier (SSDA) and consider the potential of its derivative multiplicative amplifier topologies (the cascaded and the matrix SSDA) for ultra-wideband amplification. We highlight the significant bandwidth advantage that the SSDA topology offers and the higher gain potential of multiplicative DAs compared to the conventional multi-stage DA. Furthermore, we describe how available design trade-offs may be used to offset inherent noise performance limitations of this family of distributed amplifiers. We also report a new SSDA MMIC with $7.1\,\mathrm{dB}$ gain at $200\,\mathrm{GHz}$ bandwidth and a high frequency gain tuning range of $5\,\mathrm{dB}$ to $12\,\mathrm{dB}$, based on an Indium Phosphide DHBT process with $250\,\mathrm{nm}$ emitter width.**

***Index Terms*—Distributed amplification, Single stage distributed amplifier, InP, MMIC, ultra-wideband amplifier.**

## I. Introduction

As advancements in integrated circuit (IC) fabrication technology continue to deliver device processes with higher IC- and transistor bandwidth, there is need for circuit design topologies and techniques that optimise these new generation devices and enable them to deliver maximum benefits in performance [1], [2]. Applications such as broadband communications and high resolution imaging systems continue to drive demand for ultra-wideband integrated circuitry extending into the 0.3 - 3 THz frequency bands [2]. The concept of distributed amplification, which allows the absorption of bandwidth-limiting intrinsic capacitances into artificial transmission lines, has been employed in designing amplifiers with bandwidths approaching the transition-frequency-limit of the active device [3], [4]. The conventional distributed amplifier (DA) comprises of multiple gain cells with an additive gain mechanism, rather than the multiplicative gain achieved in cascaded amplifiers. More recently, the bandwith performance merit of the single stage distributed amplifier (SSDA) over the conventional multi-stage DA has been demonstrated [5]. The cascaded SSDA (C-SSDA) and matrix SSDA (M-SSDA) which both share a unique property in that they employ purely multiplicative gain - hence the term *multiplicative DAs* - have been introduced to overcome the gain limitation of the SSDA, while retaining the bandwidth advantage [5]–[7].

In this paper, we highlight the merits of the SSDA topology for the design of ultra-wideband amplifiers by considering its gain, bandwidth and noise performance. We also report a new ultra-wideband SSDA with $200\,\mathrm{GHz}$ bandwidth at $7.1\,\mathrm{dB}$ gain based on an InP DHBT process with $250\,\mathrm{nm}$ emitter width from TSC.

## II. Merit of the SSDA and Multiplicative DA for Ultra-wideband Amplification

Compared to the multistage DA, the SSDA topology offers a clear advantage in achieving ultra-wideband performance. This arises from the fact that the shorter lengths of transmission lines required in the SSDA result in minimal attenuative losses, making the topology particularly suitable in very high frequency circuits. This is even more so for HBT-based designs, which possess a forward biased PN junction between the base and the emitter, resulting in a complex characteristic impedance, which generally results in worse termination mismatch and higher input reflection with additional stages [5], [8]. Furthermore, the slower roll-off of the single stage low-pass filters that make up the input and output artificial transmission lines of the SSDA is easily compensated for, using the attenuation compensation and bandwidth extension techniques of [8], [9].

There are two major limitations with the SSDA: limited gain from the single gain cell and lower signal to noise ratio compared to the conventional multistage DA. The gain ($G_{DA}$) of the conventional multi-stage DA is given by [10]

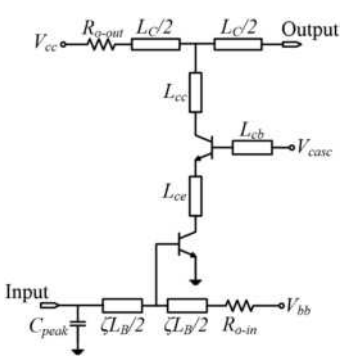
$$G_{DA} = \frac{1}{4} N^2 g_m^2 Z_{o-in} Z_{o-out}, \tag{1}$$

where $N$ is the number of stages (which is unity for the SSDA), $g_m$ is the transconductance of the active device, and $Z_{o-in}$ and $Z_{o-out}$ are the image impedances of the input and output transmission lines, respectively. The issue of limited gain has been addressed through multiplicative DA topologies - formed from cascading or arranging SSDAs in a matrix [5]–[8], [11]–[13], such that the gain of the multiplicative DA ($G_{mDA}$) is given by

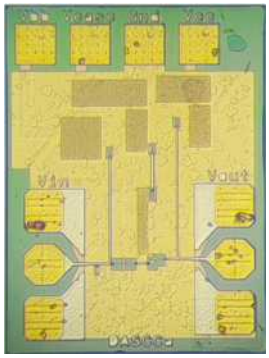
$$G_{mDA} = \frac{1}{4} g_m^2 Z_{o-int}^{2(m-1)} Z_{o-in} Z_{o-out}, \tag{2}$$

where $Z_{o-int}$ is the image impedance of the inter-stage transmission lines and *m* is the number of multiplicative stages [7]. These techniques make it possible to achieve significantly higher gain than is available from the conventional multi-stage DA, for the same number of active devices, while preserving the bandwidth advantage. The merit of the SSDA and its derivative multiplicative DA is highlighted by the fact that the amplifier that holds the current bandwidth record of any process technology and topology is the DHBT based C-SSDA cascode reported in [5], [13].

Regarding the noise performance limitation, the inherent flexibilities of the DA topology provide options for performance optimisation based on available trade-offs. Considering




(a) Schematic circuit of SSDA with scaled input line, shunt capacitance and adapted loss compensation.



(b) Microphotograph of SSDA. MMIC size: 460 µm x 620 µm.

Fig. 1: SSDA: Circuit diagram and MMIC microphotograph

the noise factor ($F_1$) of a MESFET-based SSDA which is derived as [14]

$$F_1 = 2 + \frac{4}{g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g}\omega^2 C_{gs}^2 R}{g_m} + \frac{4P}{g_m Z_{\pi g}}, \quad (3)$$

(where $g_m$ and $C_{gs}$ are the transconductance and input (gate-source) capacitance of the active device; and $Z_{\pi d}$ and $Z_{\pi g}$ are the $\pi$-image impedances of the input and output transmission lines of the DA), it is observed that the overall noise factor can be reduced by making $Z_{\pi g}$, larger. This would also increase the gain of the amplifier but the bandwidth would be reduced commensurately [14].

Further design trade-offs that allow for performance optimisation are available in the multiplicative DA. In [15], it is established that multiplicative DAs follow the noise scaling mechanism of cascaded systems, such that the overall noise factor of the amplifier is primarily established by the noise factor of the first gain stage. (The Friis' noise formula has been modified in [15], to describe the noise factor of multiplicative DAs.) A viable design approach is to to make the noise factor of the first stage of the multiplicative DA as low as possible at appreciable single stage gain. This may be achieved by designing the input transmission line at a higher image impedance and by adopting a transistor with a wider bandwidth potential i.e lower input capacitance (and corresponding lower gain) in the first stage. With this approach, the loss in bandwidth from using a higher image impedance input line is offset by the inherent wider bandwidth of the transistor, while from (2), the gain is kept at an appreciable level by increasing $Z_{o-in}$.

## III. Amplifier Design and Optimisation

We report a SSDA which is suitable as a gain unit in a multiplicative DA topology. The amplifier features a cascode gain cell with two identical InP DHBTs, each with an emitter area of $0.25 \times 6\mu m^2$. The cascode configuration is favoured for the high input-output isolation it offers, as well as the high output impedance which advantageously reduces the loading on the output transmission line of the DA [13], [16]. The design is based on an Indium Phosphide process with $f_T/f_{max}$ of 350 GHz / 600 GHz [17]. The device was biased at $I_B = 0.75\ mA$, $V_{CC} = 5.2\ V$ and $I_C = 14.8\ mA$. To improve bandwidth performance, the input transmission line is scaled down by a factor $\zeta \approx 0.5$ and peaked by a shunt capacitance $C_{peak} = \frac{1}{2}C_\pi$, where $C_\pi$ is the input (base-emitter junction) capacitance of the active device [8]. The loss compensation technique described in [8] was employed to achieve flat forward gain response. Fig. 1a shows the SSDA schematic featuring the applied modifications.

## IV. Results and Discussion

The fabricated MMIC occupies an area of 460 µm x 620 µm and can be seen in Fig. 1b. The verification of the amplifiers performance was done via small-signal on-probe measurements. Due to the wide bandwidth of the amplifier, two different measurement setups were required to characterize it.

The low frequency response of the amplifier was measured on probe in the band 100 MHz – 120 GHz with the VectorStar ME7838A series broadband VNA by Anritsu via 75 um 145 GHz Infinity probes. The input power was set to −20 dBm to avoid saturating the amplifier. The high frequency response in the band between 140 GHz – 220 GHz was measured with PNA-X N5247A by Keysight using VDI WR-5.1 frequency extenders and WR-5.1 waveguide probes. The input power was set and calibrated at −10 dBm to accommodate for the optimal operation of the frequency extenders. The limitations of the measurement equipment did not allow measurement in the 120 GHz – 140 GHz band. In both setups, the measurement reference plane was calibrated to the probe tips via certified calibration substrates.

Fig. 2 presents the results of the two measurements along with the simulated performance of the amplifier. There is good agreement between the simulated and the measured forward gain in terms of the bandwidth of 200 GHz. However, with average measured gain at 7.1 dB, there is an average shortfall in gain of ∼2.5 dB compared to the simulated response across the device bandwidth. The input and output reflection curves show good matching to the predicted results in the lower

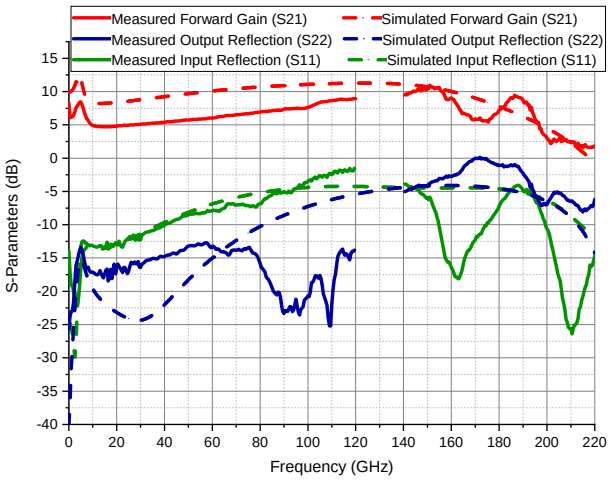



Fig. 2: Measured vs simulated S-parameters.

TABLE I: Comparison with state-of-the-art SSDAs and cascaded-SSDAs in literature.

| Technology | BW (GHz) | Gain (dB) | GBW (GHz) | Pdc (mW) | Area ($mm^2$) | DA Topology | Ref |
|---|---|---|---|---|---|---|---|
| 250 nm InP HBT | 192 | 7.5 | 455 | 40 | 0.24 | SSDA | [5] |
| 250 nm InP HBT | 235 | 16 | 1480 | 117 | 0.41 | 2-Cascaded-SSDA | [5] |
| 130 nm SiGe BiCMOS | 170 | 13 | 759 | 74 | 0.22 | 4-Cascaded-SSDA | [18] |
| 130 nm SiGe BiCMOS | 175 | 16 | 1102 | 360 | 0.38 | 2-Cascaded-SSDA (Balanced) | [11] |
| **250 nm InP HBT** | **200** | **7.1** | **455** | **75** | **0.28** | **SSDA** | **This Work** |

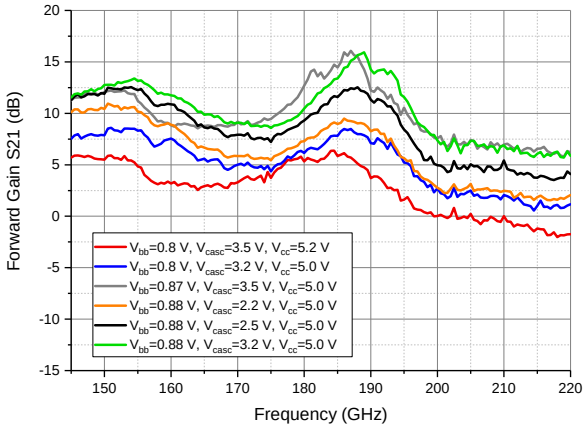



Fig. 3: High frequency S-Parameter response for SSDA under different bias conditions.

frequencies. In the higher frequency range, the measured results show some ripples on both input and output reflection curves around 150 GHz and 200 GHz, that were not predicted in pre-fabrication simulations. Following extensive post-measurement simulations, these ripples, which also manifest in the forward gain curve, were attributed to parasitics from the DC bias probes. Furthermore, a full E/M study of the substrate including the through-substrate-vias used, indicated that the substrate could sustain resonant modes at frequencies close to 160 GHz and 190 GHz. These resonances would account for the output reflection coefficient approaching 0 dB. It is expected that both effects would be alleviated by packaging the MMIC, as this would improve both the decoupling and the grounding of the amplifier.

Since the amplifier consists of a single cascode pair, it was straightforward to tune the gain of the amplifier, using the base and cascode biases ($V_{bb}$ and $V_{Casc}$, respectively) for various gain profiles. The measured results for different bias voltages are presented in Fig. 3, where a gain tuning range from 5 dB to 12 dB is demonstrated. Comparison of the amplifier with state-of-the-art SSDAs and multiplicative DAs in literature is presented in Table I. The amplifier of this work has the highest bandwidth to-date of reported single stage designs and is only outperformed by the 2-cascaded-SSDA in [5].

## V. Conclusion

The peculiarities of the SSDA topology make it possible to operate new generation transistor processes close to their bandwidth limit and would be instrumental in making Terahertz bandwidth amplification more practical. In this paper, we highlight the merits of the SSDA and its multiplicative derivatives in achieving ultra-wideband amplification, and we describe design approaches to gain, bandwidth and noise performance optimisation. We also present an SSDA amplifier with 200 GHz bandwidth and 7.1 dB gain that consumes 75 mW of power. To the authors' best knowledge, this is the highest bandwidth reported for any SSDA.

## References


[1] M. Urteaga, Z. Griffith, R. Pierson, P. Rowell, A. Young, J. Hacker, B. Brar, S. Kim, R. Maurer, and M. Rodwell, "THz InP bipolar transistors-circuit integration and applications," in *Compound Semiconductor IC Symposium (CSICS), 2017*. IEEE, 2017, pp. 1–4.

[2] S. Kang, D. Kim, M. Urteaga, and M. Seo, "State-of-the-art THz integrated circuits in InP HBT technologies," in *Radio-Frequency Integration Technology (RFIT), 2017 IEEE International Symposium on*. IEEE, 2017, pp. 25–27.

[3] E. L. Ginzton, W. R. Hewlett, J. H. Jasberg, and J. D. Noe, "Distributed amplification," *Proceedings of IRE*, vol. 36, pp. 956–969, 1948.

[4] T. T. Wong, *Fundamentals of distributed amplification*. Artech House, 1993.

[5] K. Eriksson, I. Darwazeh, and H. Zirath, "InP DHBT distributed amplifiers with up to 235-GHz bandwidth," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1334–1341, 2015.

[6] J. Y. Liang and C. S. Aitchison, "Gain performance of cascade of single stage distributed amplifiers [microwave circuits]," *Electronics Letters*, vol. 31, no. 15, pp. 1260–1261, Jul 1995.

[7] T. Odedeyi and I. Darwazeh, "Matrix single stage distributed amplifier design for ultra wideband application," in *24th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Batumi, Georgia, 2017*. IEEE, 2017.

[8] ——, "Bandwidth enhancement technique for bipolar single stage distributed amplifier design," in *2017 IEEE Asia Pacific Microwave Conference (APMC)*, 2017, pp. 833–836.

[9] S. Kimura, Y. Imai, Y. Umeda, and T. Enoki, "Loss-compensated distributed baseband amplifier IC's for optical transmission systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 10, pp. 1688–1693, Oct 1996.

[10] C. Poole and I. Darwazeh, *Microwave Active Circuit Analysis and Design*. Academic Press, 2015, pp. 468-470.

[11] P. V. Testa, C. Carta, U. Jörges, and F. Ellinger, "Analysis and design of a 30-to 220-GHz balanced cascaded single-stage distributed amplifier in 130-nm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1457–1467, 2018.

[12] G. Nikandish, R. B. Staszewski, and A. Zhu, "The (r)evolution of distributed amplifiers: From vacuum tubes to modern CMOS and GaN ICs," *IEEE Microwave Magazine*, vol. 19, no. 4, pp. 66–83, 2018.

[13] K. Eriksson, I. Darwazeh, and H. Zirath, "InP DHBT wideband amplifiers with up to 235 GHz bandwidth," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*. IEEE, 2014, pp. 1–4.

[14] C. S. Aitchison, "The intrinsic noise figure of the MESFET distributed amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 6, pp. 460–466, 1985.

[15] T. Odedeyi, C. Poole, and I. Darwazeh, "Noise analysis of multiplicative distributed amplifiers," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019, pp. 1–5.

[16] K. Kobayashi, D. Umemoto, T. Block, A. Oki, and D. Streit, "A wideband HEMT cascode low-noise amplifier with HBT bias regulation," *IEEE microwave and guided wave letters*, vol. 5, pp. 457–459, 1995.

[17] J. Hacker, M. Seo, A. Young, Z. Griffith, M. Urteaga, T. Reed, and M. Rodwell, "THz MMICs based on InP HBT technology," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*. IEEE, 2010, pp. 1126–1129.

[18] P. V. Testa, R. Paulo, C. Carta, and F. Ellinger, "250 GHz SiGe-BiCMOS cascaded single-stage distributed amplifier," in *Compound Semiconductor IC Symposium (CSICS), IEEE*. IEEE, 2015, pp. 1–4.