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Towards the integration of InP photonics with silicon electronics: design and technology challenges

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***Abstract*—Intimate integration of photonics with electronics is regarded as the key to further improvement in bandwidth, speed and energy efficiency of information transport systems. Here, a method based on wafer-scale polymer bonding is reviewed which is compatible with foundry-sourced high-performance InP photonics and BiCMOS electronics. We address challenges with respect to circuit architecture, co-simulation framework and interconnect technology and introduce our approach that can lead to broadband high-density interconnects between photonics and electronics. Recent proof-of-concept work utilizing DC-coupled driver connections to modulators, which significantly reduces the interconnect complexity, is summarized. Furthermore, co-simulation concepts based on equivalent circuit models are discussed with emphasis on the importance of impedance matching between driver and modulator. Finally, realizations of broadband interconnects and functional photonic building blocks after wafer bonding are highlighted to demonstrate the potential of this wafer-scale co-integration method.**

***Index Terms*—Photonic integrated circuits, wafer scale integration, BiCMOS integrated circuits, optical transceiver, electronic photonic integration**

I. Introduction

The motivation to integrate photonic functionality with electronic circuits has been long-lasting [1]. Electronic Integrated Circuits (EIC) followed Moore's Law scaling to reach today's state-of-the-art billion transistor chips, capable of Teraflops of data processing [2]. Photonic Integrated Circuits (PIC) are undergoing a similar progression, driven by the exponential increase in capacity demand of information transport systems, reaching thousands of components and terabit/s on chip [3], [4]. In both cases continued advances in the level of integration and the laws of scaling have been fundamental in meeting the communication and processing needs of today's applications.

However, with information systems pressing for higher performance and requiring further reduction of cost and power consumption, continued scaling of EIC and PIC separately from each other falls short to keep up with the demand. This can be attributed to the shortcomings of the current technology used to interconnect electronics and photonics, which failed to scale at the same pace and lacks the required bandwidth density in Tb/s per unit area. It poses a significant bottleneck to the performance of combined electronic-photonic systems, especially visible in data transport applications ranging from medium distance links to optical interconnects in data centers, on-board optics and chip-to-chip communications. It has been predicted for example that high-speed transceiver interface scaling will not be able to keep up with future increases in data generation and processing in ASICS, if current scaling rates are to continue [5]. To overcome this disparity, the photonic part of the transceiver has to be brought as close as possible to the electronics using co-integration approaches. Furthermore, coherent systems are now being used more frequently in short optical links, as well as in longer-haul systems, and these depend on complex, fast electronics to be closely interfaced with optical modulators and detectors, once again necessitating a higher degree of co-integration [6]. Likewise, the growth in channel count for Gigabit ethernet [7] and Tb/s optical interconnects [8] demands parallel scaling of connections between electronics and photonics for increased capacity, whereas the increase in symbol rate dictates close integration of the two in order to reduce electrical parasitics and enlarge serial bandwidth. A clear demand thus arises for scaling electronics and photonics as a co-integrated system incorporating high-density broadband interconnects and move towards convergence of the two.

Several technological approaches are being followed to realize this ambition. Monolithic concepts create photonic functionality on top of mature electronic processes with zero change e.g. in BiCMOS [9], CMOS [10] or InP [11]. This has led to transmitters and receivers reaching 64 GBaud operation in BiCMOS [12], [13], [14], albeit obtained with limited analog bandwidth (18 GHz for the modulator and 34 GHz for the receiver), and the realization of CMOS chiplets for chip-to-chip communications (13 GHz modulator, 5 GHz receiver) [10] [15]. Those examples show great promise with respect to integration density and scalability, but compromise on the optical circuit performance compared to dedicated photonic processes.

Dedicated silicon photonic foundry processes are well established and allow for higher overall transmit and receive

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performance [10] than their monolithic CMOS and BiCMOS counterparts, but laser integration remains to be a challenge for all silicon platforms and subject of active research. Generic InP based foundries in contrast can readily integrate active materials [16]–[18], rely on a stronger electro-optic (EO) Kerr and Pockels effect and thus achieve higher EO bandwidth-efficiency metrics [19]. Further enhancement of the EO effect can be accomplished with the quantum-confined Stark effect in quantum wells, but at the cost of higher temperature and wavelength dependence. Modulators and detectors with bandwidths exceeding 80 GHz have been demonstrated using the InP material system [20], [21], which, together with the capability for monolithic integration of various types of laser circuits [22], [23], makes InP PICs very attractive for co-integration with EICs. On the electronics side, generic foundry processes such as the 0.25 µm BiCMOS technology have been found to be well suited for high-speed transmitter and receiver front-ends [24]–[26]. A second approach to advance towards electronic-photonic convergence is therefore to rely on foundry-sourced high-performance EICs and PICs and co-integrate them using a scalable high-density interconnect process. The advantage is that well established electronic and photonic technology can be used essentially without change and thus without compromising the commercial foundry model or the performance of the combined system. The key challenge in this approach lies in establishing a scalable high-performance integration technology between electronics and photonics with high-speed interconnects.

Conventional co-packaging concepts connect highly integrated electronics with densely packed photonics using wire bonds that run along the edge of the circuits [3]. These introduce significant parasitics, causing signal degradations [27] and, more profoundly, only allow a limited number of connections due to the one-dimensional nature of the interface. Stud bump bonding used in flip-chip assemblies supports broadband connections and provides a two-dimensional interface [28], [29]. This has been applied on die level and used successfully to connect high-speed DACs and drivers to EAM arrays and to terminate MZMs with resistive load chips [20], [30]. However, wafer-level packaging is preferred in industry for scalability reasons, as it can enable lower production cost and higher yield [31], [32]. Die-to-wafer and wafer-to-wafer bonding are two promising approaches here. We pursued the latter for its potential to achieve higher throughput and the possibility to define interconnects between electronics and photonics lithographically at fine resolution, going beyond what current die-level processes can achieve in density and size.

Wafer bonding using polymers such as BCB as the adhesive layer has been suggested as a promising wafer-level technology to integrate electronics and photonics [33]. It is compatible with foundry sourced high-performance wafers, scalable in process and can be applied in a mature production environment [34]. Here we pursue this approach and discuss several challenges that need to be tackled on the route to electronic-photonic convergence.

Currently, the interconnect schemes between EIC and PIC are designed to operate with cumbersome and bulky biasing and supply circuitry, not suitable for high-density wafer-scale bonding. Innovations in circuit architecture and coupling schemes are needed that facilitate direct connection of driver electronics with fast optics. Furthermore, co-design and co-simulation becomes much more important in optimizing and predicting the combined system performance once EIC and PIC are closely integrated. New methodologies that incorporate electronic and photonic device models are needed. Finally, realizing broadband, high-density electrical interconnects through the polymer bonding layer is a key technology challenge to successful co-integration. In this paper, we present the recent work of the authors related to these design and technology aspects, extending the material presented in [35], and discuss how advances here can lead to wafer-scale co-integration of photonics with electronics. Section II discusses the interconnect schemes that are required for direct connection of EIC and PIC. Section III summarizes a joint electronic photonic simulation framework based on equivalent circuit representations and section IV outlines the progress in developing a high-density interconnect technology that supports broadband operation. Results of proof-of-concept building block operation will be presented and the conclusion is given finally in section V.

II. Interconnection Scheme Between Electronics and Photonics

A. *Interconnect Complexity*

Most modulator and detector devices require a DC bias to operate at their optimum. This is usually fed through a biasing circuit (AC coupling) which requires an external bias source and is inserted between the EIC and PIC as shown in Figure 1a for a driver-modulator configuration. When co-packaging devices, it can be easily realized in combination with wire bonds and surface mount components as depicted in Figure 1d. However, when moving towards two-dimensional wafer-scale interconnections with a high degree of integration, such a biasing circuit is not desired as the connection needs to be kept as short as possible to increase the achievable density and reduce parasitics. A direct connection between the driver output and modulator input is needed (DC coupling), as indicated in Figure 1b, c for the single-ended and differential case, respectively. Appropriate driver designs that support DC coupling reduce the coupling complexity and thus enable wafer-scale interconnections.

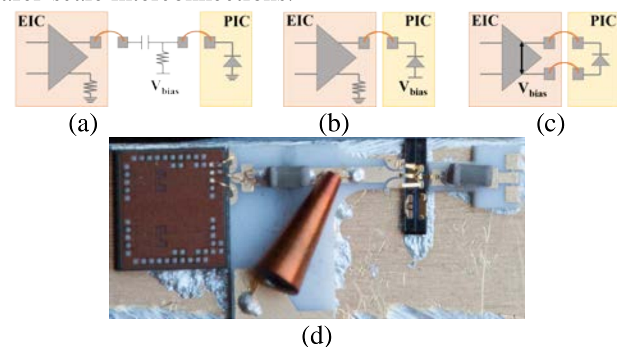

Figure 1: Connection between EIC and PIC using (a) biasing circuit and AC coupling, (b) single-ended DC coupling and (c) differential DC coupling. (d) Assembly of EIC and PIC using AC coupling.

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B. DC Coupling Proof-of-Concept

The single-ended DC coupling scheme has been used to connect drivers with electro-absorption modulators (EAM) [36] We have designed and fabricated a driver with DC coupling in a commercial 0.25 µm SiGe:C BiCMOS foundry technology, exhibiting 31.5 GHz bandwidth, 3V p-p output swing and open electrical eye diagrams at 56 Gb/s PAM-4 (VEC of 9.98 dB), leading to 6.5 pJ/bit power consumption [37]. The operation speed and energy per bit of the driver is limited by the transit frequency available on the commercial process but is sufficient for a proof-of-concept for DC coupling to photonics. To demonstrate the feasibility of a simplified interconnection with the modulator, we have paired it with EAM devices with 32 GHz of bandwidth [38] which were manufactured in a generic InP photonic foundry [39]. The DC coupling scheme was demonstrated with wire bond chip-to-chip interconnection to verify the operation of the scheme, as shown in Figure 2a. Note that the complexity of the connections between EIC and PIC in Figure 2a has reduced to a few direct bonds compared to Figure 1d. In principle, the termination loads on the right-hand side of the EAM can be integrated into the EIC when moving towards wafer-scale integration. The assembly has been characterized in transmission experiments with results and further details given in [40]. It exhibits open optical eye diagrams with an extinction ratio of 3.38 dB at 36 Gb/s NRZ, verifying the DC coupling operation [40]. The wire bonds are the limiting factor in this experiment, as both the driver and EAM had been characterized separately to work at higher modulation speeds.

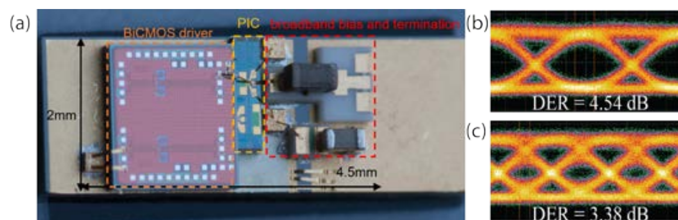

Figure 2 (a) Direct die-to-die connection for electro-absorption modulator-driver combination enabled through DC coupling with eye diagrams at (b) 20Gbit/s and (c) 36Gbit/s NRZ modulation. [40]

The single-ended DC coupling only makes use of half the available driver output swing voltage. In contrast, differential DC coupling can utilize the complete output swing with reduced common mode distortion and has been suggested in [41]. We have previously reported a novel driver design, shown in Figure 3, which is based on differential DC coupling that utilizes an asymmetric load configuration to provide up to -2V of bias for EAMs [24]. It can also operate in single-ended drive and allows for two EAMs to be connected with separate bias adjustments. It has been fabricated in the same commercial 0.25 µm SiGe:C BiCMOS foundry technology, exhibiting 51.5 GHz bandwidth, 2V p-p output swing and open electrical eye diagrams at 56 Gb/s PAM-4 (VEC of 10 dB), leading to 3.9 pJ/bit power consumption [24]. Most recently we have assembled the drivers with EAM modulators using the co-integration technology presented in section IV. The validation experiments are presently in progress.

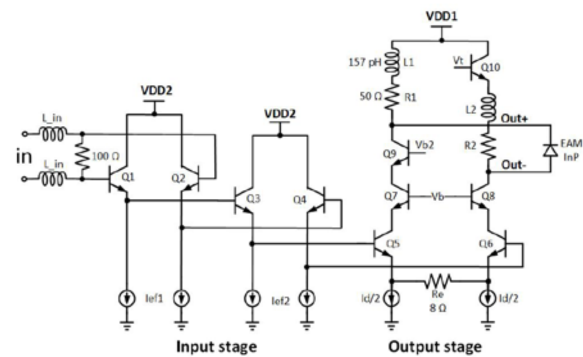

Figure 3: Driver with differential output and asymmetric load [24].

Similarly, for connecting to Mach-Zehnder modulators (MZM), DC coupling can reduce the complexity of the interconnection, as demonstrated in [42], [43]. Such a connection scheme is shown in Figure 4. Here, the data signal can be fed from the differential driver directly to the electrodes of the MZM and passed to a termination circuit at the output side. The modulator bias voltage is provided through the driver output with respect to the n-contact point of the photonic chip. This is possible if the MZM is made on semi-insulating substrate and operated in series push-pull [44], enabling short direct connections between the driver and modulator.

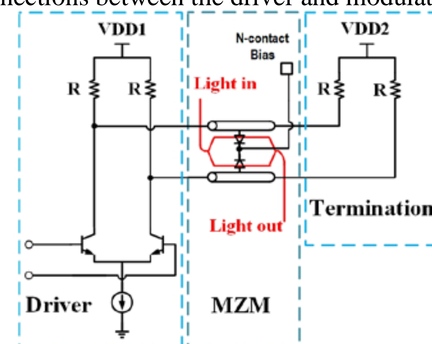

Figure 4: Circuit diagram of driver-MZM connection with termination.

We have designed a MZM driver based on a five-stage distributed amplifier topology that works with differential DC coupling and differential termination. It can supply 4 V p-p swing, exhibiting a bandwidth of 40 GHz, and was manufactured in the 0.25 µm SiGe:C BiCMOS technology [45]. To verify the DC-coupled operation, it has been combined with a DBR-laser-MZM transmitter that was fabricated in an experimental generic photonic foundry run [46]. The travelling-wave MZM, capable of 40 Gb/s NRZ operation with 35 GHz of bandwidth [47], is connected to the driver and to a resistor load chip which is fabricated in the same BiCMOS technology. The bias voltage is applied through the MZM n-contact. Wire bonds are used again to form an assembly of EIC and PIC to verify the working principle. We could observe open large-signal optical eye diagrams for the assembly at 30 Gb/s NRZ (extinction ratio of 5.63 dB), which validates the DC coupling scheme for driver-MZM assemblies. In the experiment, the modulator output is loaded with a 50 Ohm resistor, matching the MZM characteristic impedance. However, the driver output is intended for 100 Ohm differential output and its performance is degraded due to a mismatch to the MZM impedance. In

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principle, with the ability to co-design the EIC and PIC, any other value of impedance can be targeted and further performance improvement can be expected. Here, the focus lies on the DC-coupled interconnection scheme but we will see in section III that proper impedance matching between driver and modulator has a significant impact on the system performance.

C. Bond Wire Performance

The two assemblies using bond wires clearly illustrate that adopting a DC coupling scheme reduces the complexity of the interconnects between EIC and PIC by omitting otherwise cumbersome biasing circuitry. This is a prerequisite when moving towards wafer-scale co-integration processes. Furthermore, it becomes clear that the wire bonds are a limiting factor with respect to speed. Transitioning from high inductance wire bonds towards stud bump bonding and ultimately to wafer-scale interconnects will increase the bandwidth and density of connections that can be pushed through the interface.

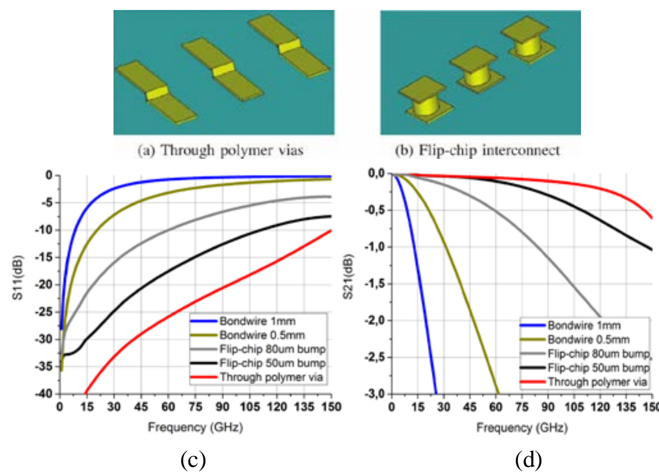

Figure 5: 3D model of (a) 40 µm wide and 7 µm high TPV and (b) 50 µm diameter stud bump connections. Simulated (c) S11 and (d) S21 for bond wire, stud bump and TPV connections. [48]

We have modeled bond wires, stud bump and through polymer via (TPV) interconnects in Advanced Design System (ADS) [49] using the standard bond wire model [50] and CST Studio Suite [51] with custom geometries. Figure 5a,b depict the shape of 40 µm wide, 7 µm high TPVs and stud bumps with 40 µm height and either 50 µm or 80 µm diameter in a coplanar GSG configuration. We performed simulations in [48] to compare their respective bandwidths with that of standard wire bonds, 0.5 and 1 mm in length, 25 µm in diameter, and the results are shown in Figure 5c,d. It can be seen that moving from wire bonds to stud bumps significantly improves the bandwidth, which is attributed to the omission of wire inductance and a reduction in interconnect resistance. Although well-designed short ribbon bonds can be of high bandwidth and alleviate some of the wire bond drawbacks, they do not provide the needed level of interconnect density. Further improvement in bandwidth can be achieved when moving to TPVs, with only 0.5 dB transmission loss at 150 GHz. This is due to their smaller dimensions and less parasitic pad capacitances compared to the stud bump case.

This section has presented ways to simplify the interconnect circuitry between EIC and PIC, particularly for high-speed transmitters, and demonstrated these techniques using die-to-die assemblies. The schemes we have presented become essential for wafer-scale co-integration using TPV interconnects, which have been shown in simulation to perform much better than conventional wire and stud bump bonding.

III. Co-Simulation and Design Framework

Another challenge when moving towards co-integrated electronic and photonic systems is to predict the performance of the combined system accurately. This can be achieved when the simulation approaches and design flows for the EIC and for the PIC are consolidated. Recent work has focused on integrating compact models of photonic devices into standard CMOS simulation environments e.g. using VerilogA [52], [53] or with commercial links between software providers such as Cadence and Lumerical establishing common electronic photonic design automation (EPDA) [54]. It works well for passive optics that can be described with S-parameters but becomes more challenging when modelling active components such as lasers or modulators in combination with driver electronics [55]. Especially for high-speed applications, it is important to correctly capture and account for the RF chain between the driver, interconnects and modulator.

We summarize our work on developing an equivalent circuit based electro-optic model for a MZM device that can be easily implemented in electronic tools to be co-simulated with driver models. This is illustrated in an example where the modulator is connected with an electrical filter circuit.

A. Electrical Model of Modulators

A successful model of the MZM for co-simulation purposes needs on the one hand to be simple to implement in electronic circuit simulation environments such as ADS or Cadence Spectre, whilst on the other hand also capture the physical mechanisms that govern the modulator operation such as transmission line effects, voltage induced refractive index change and the optical interferometer transfer function.

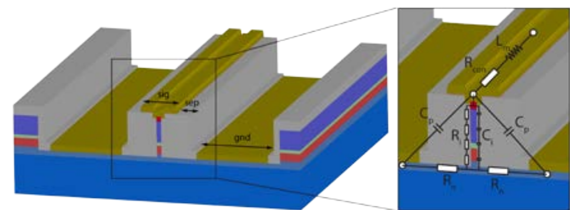

Figure 6: Equivalent circuit model for traveling-wave MZM modulator.

We are using a combination of an equivalent circuit model with analytical first-principle calculations to represent electrical signal propagation along the optical phase modulator, capturing the interplay between the transmission line and the optical wave. Figure 6 illustrates the cross-section of a coplanar MZM electrode and how the equivalent circuit is mapped to the electrode geometry. Each element is calculated from first principles through analytical expressions that depend on the design geometries. It is further resolved spatially by constructing a distributed equivalent circuit along the

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propagation direction to incorporate the effect of traveling-wave behavior and electrical signal to optical group velocity mismatch. The voltage dependent refractive index change along the modulator electrode is calculated by incorporating the Pockels, Kerr and plasma dispersion effects in the optical waveguide. The model is implemented within the ADS tool [49] and allows for structural optimization which directly results in changes in the output of a system simulation and has been verified against experimental small and large-signal measurements of manufactured InP traveling-wave MZMs [56]. This allowed the current limitations to modulator speed to be analyzed and has yielded 100 GHz class optimized modulator designs [57]. Figure 7 shows a good match of the calculated electro-optic frequency response from our model with the measured data for a modulator device used for calibration purposes. Here, the fast reduction and plateau of the EO response is due to an impedance mismatch of the electrode (~25 Ω) to the measurement environment (50 Ω). The model successfully accounts for mismatch effects which will be discussed in the next section and agrees with the experimental data.

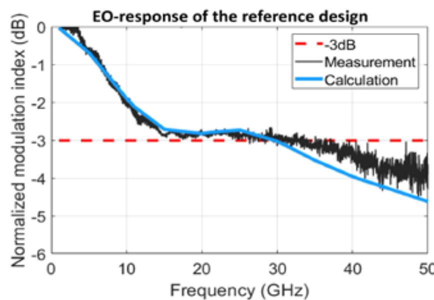

Figure 7: Calculated EO frequency response compared with measured data of 1 mm long traveling-wave coplanar MZM for model calibration [56].

To illustrate that the model can easily be extended to interface with electronic circuits, we connect the modulator to an electrical filter as shown in the inset of Figure 8. In this case, its purpose is to pre-emphasize the analog signals entering the modulator electrode and achieve a flatter overall frequency response, which can be seen in Figure 8. Similarly, this approach can be extended to incorporate a complete driver circuit and used for co-simulation of EIC and PIC performance.

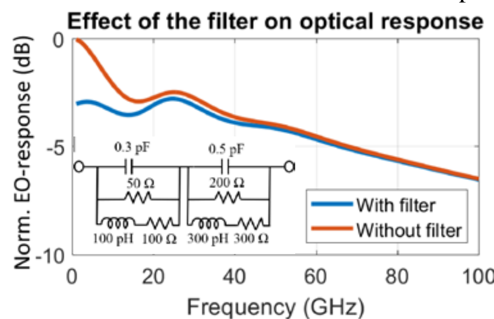

Figure 8: Combined simulation of pre-emphasis filter with modulator model indicating a flattening of frequency response.

B. Choice of Impedances

Co-integrating drivers and modulators on wafer-scale eliminates lengthy cabling and connections between them. Thus, the need to match to the standard RF system impedance of 50 Ohm is no longer present and the value of driver output and modulator load impedances can instead be chosen freely to optimize for low power consumption or high-speed operation.

Instead of using 50 Ohm load resistors in the output driver stage, resistors with 40 Ohm can be implemented in combination with inductors of 166 pH, with the latter responsible for an inductive peaking effect in the frequency response [37]. This peaking can compensate for EAM losses and achieve a higher bandwidth in the driver-EAM system overall. Furthermore, it results in higher voltage gain in the driver and higher output swing as shown in Figure 9.

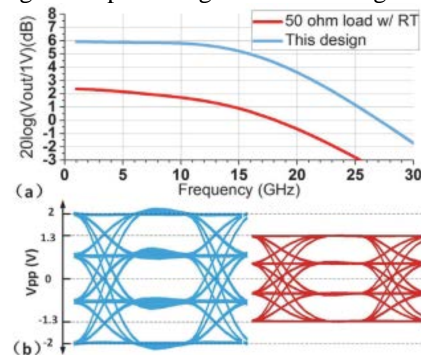

Figure 9: Simulated driver performance with different loading configurations: (a) voltage gain vs frequency and (b) eye diagram at 20 GBaud PAM-4.[37]

Similarly, the loading condition at the end of the modulator device is an important parameter that can be optimized. If the driver modulator interface is already impedance matched, the modulator loading can also deviate from 50 Ohm and take a value that maximizes the bandwidth. Utilizing the equivalent circuit model, we have analyzed this on MZM electrodes, for which the electro-optic modulation index has been calculated for different load resistor values [56], illustrated in Figure 10. In this case, the characteristic impedance of the modulator has the value of 23 Ohm, causing a better broadband match if the load is between 20 and 25 Ohm. It can be seen that the bandwidth increases significantly over the 50 Ohm loading case from 35 GHz to 60 GHz.

Both examples illustrate the importance of a joint approach to EIC and PIC simulation and show how an equivalent circuit model can help analyze the role of impedance matching on the total driver-modulator performance.

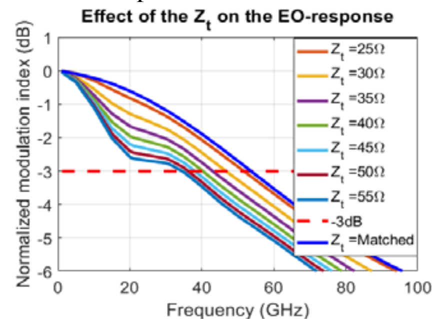

Figure 10: Simulated modulation index vs frequency for varying loading conditions [56]. Z_t is the termination load value.

IV. Co-Integration Technology

Next to the interconnect circuit schemes and the co-simulation framework, the development of wafer-scale interconnection technology is central in achieving electronic-photonic co-integration and increasing density. The wafer bonding process

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is one part of it, but also the realization of broadband metal connections in the form of through-polymer vias is essential for connecting contact pads between the electronic layer and photonic layer.

A. *Wafer Bonding Process*

Several wafer bonding techniques exist and have been studied in the literature [58]. We pursue adhesive wafer bonding here, as it has been successfully applied to bond InP devices on silicon wafers for heterogeneous integration schemes [59], using BCB as a bonding polymer. It allows for moderately low bonding temperatures and low levels of outgassing, being used widely in 3D packaging of electronic ICs [60], [61].

Within the WIPE [62] project, the BCB bonding process has been developed to work with fully populated electronic and photonic wafers, accommodating total vertical topology variations up to 9 µm. The bonding scheme is illustrated in Figure 11a, with further details reported in [63]. The BCB is spin-coated onto both wafers and then soft-baked. The actual bonding is performed at a temperature of 240°C, which is limited by the used BiCMOS technology. Temperature budget tests have been performed to define the boundary conditions. For 15~hours at 240°C no degradation has been detected, while 1~hour at 280°C resulted in measurable performance reduction. The photonic wafer and electronic wafer are bonded facing each other to enable the shortest possible electrical connections. The BCB is cured for 10~hours to guarantee full cross linking according to [64], [65].

The alignment is performed using the backside alignment technique [34]. Markers on the backside of the InP wafer are transferred by optical contact lithography. The theoretical wafer-to-wafer alignment accuracy is 2 µm. We have tested wafer bonds with varying BCB thicknesses and observed reproducible accuracy <4 µm. This is sufficiently small to realize broadband high-density interconnects between the EIC and PIC. The InP and silicon wafer have a different linear thermal expansion coefficients (CTEs) which will result in a shift during bonding. This position dependent effect can be pre-calculated and compensated for during the design phase of the InP wafer. It has further no influence on the overall alignment. Finally, the substrate of the InP wafer is removed in a wet etch step until only the functional photonic layers remain. Figure 11 (b), (c) show a bonded sample of a 3” InP photonic wafer on top of a silicon electronic BiCMOS wafer and the contact pads after the TPV process.

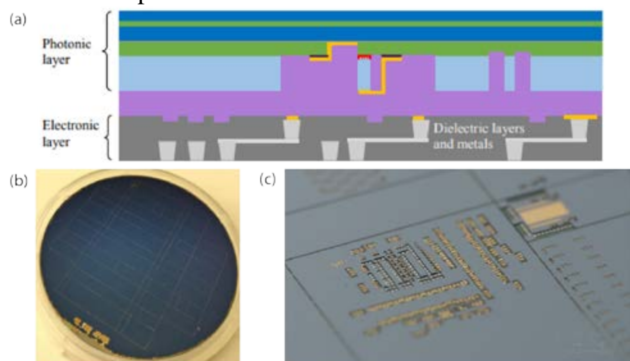

Figure 11: (a) Illustration of PIC bonded to EIC [63]. (b) Microphotograph of bonded photonic wafer on electronic wafer. (c) Microphotograph of EIC and PIC after TPV creation.

B. *Through Polymer Via Interconnects*

After a successful bond, the interconnections need to be established. The developed TPV process has been reported in [66]. To create vias, the photonic layers and the BCB bonding layer at the positions of the InP and BiCMOS contact pads are completely removed in an etching step, so that they are exposed. To define sloped side walls in the BCB-layer, on which the metal interconnects can be created, a photoresist AZ9260-layer [67] is used in combination with reactive ion etching. For the via metallization, a seed layer of Ti/Au is applied, followed by an electro-plating process. The schematic of the via process and SEM images of realized TPVs can be seen in Figure 12 and Figure 13.

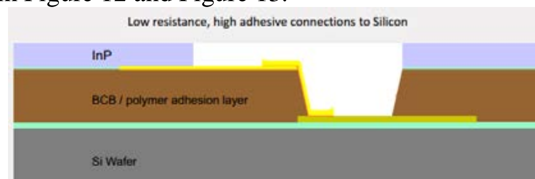

Figure 12: Illustration of through polymer vias created between EIC and PIC.

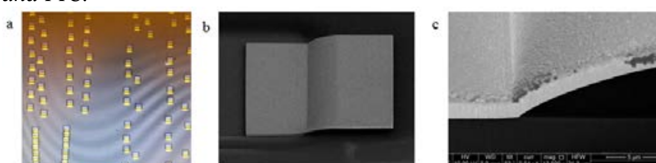

Figure 13 Through polymer vias with a) completed process module showing top-to-bottom-surface electrode connection b) one via with dimensions 116×116 µm² and c) detailed view of the via.[66]

These TPVs have been characterized in both DC and RF measurements, in order to assess their suitability for broadband interconnects in high-speed applications. For the DC measurement, we have established TPVs through 7 µm thick BCB. Figure 14 shows the resistance obtained in a four-probe measurement on tracks of different lengths that either contain a via transition or not [66]. It can be seen that the resistance values follow the predicted length dependence. No significant difference is caused due to a via transition compared to tracks without vias. Since the thickness of the TPV metal varies as a result of the used plating process, upper and lower resistance estimates have been calculated and plotted. The minimum TPV size depends on the thickness of the bonding layer and can be reduced to be similar in dimension. Given a good wafer planarity, it can be reduced to the order of ~10 µm, making them suitable for high-density connections. Further tests shown in Figure 15 reveal that the measured resistance before and after a temperature cycling procedure does not change significantly.

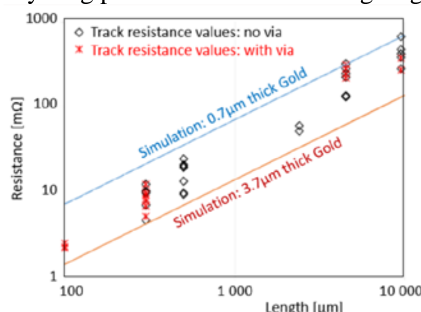

Figure 14: Resistance measured on metal tracks with and without TPVs at different track lengths.[66]

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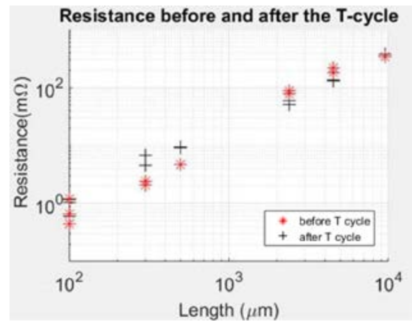

Figure 15: Measured DC resistance of TPVs before and after temperature cycling (-40˚C to 85˚C, 15 min dwell time, 400 cycles).

For the RF characterization, we have formed TPVs through 24 µm thick BCB, connecting coplanar waveguide tracks on an InP sample with tracks on a BiCMOS wafer [68]. A thicker bonding layer is utilized here to cover the increased wafer topology. S-Parameter values measured from the EIC to the PIC are shown in Figure 16. It is worth noting that transmission lines on both sides are not de-embedded in this case and their influence is included in the measured results. The S21 of the coplanar tracks including three TPV transitions of 75 µm width and 50 µm separation lies above -3dB within the full measurement range until 67 GHz. The reflection values are kept below -10 dB until 50 GHz, confirming that TPVs can act as broadband RF interconnects between EIC and PICs. Note that the measurement includes the effect of the transmission line losses on both the EIC and PIC side and higher bandwidth for the pure TPV structures can be expected after de-embedding of the transmission lines. Further improvement can be gained by shrinking the dimensions of the TPV structures.

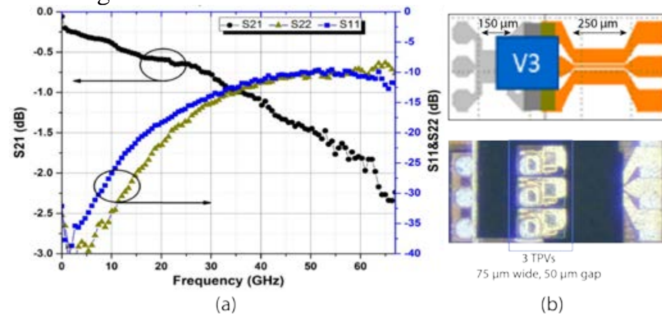

Figure 16 (a) S-Parameter measurement of coplanar track from EIC to PIC that contains TPVs (75 µm wide, 50 µm gap). (b) Schematic and microphotograph of test structure.

C. Photonic building blocks

To validate the TPV technology in combination with the adhesive polymer bonding approach for functional device building blocks, we have performed bonding experiments with foundry-sourced wafers [68]. An electronic wafer is fabricated in the NXP SiGe 0.25µm BiCMOS technology and contains transmitter and receiver components. Section II has presented connection schemes that were implemented in the EIC designs. The photonic wafer originates from the HHI generic InP foundry platform [16], [17], [69], which has been used to produce PICs for a wide range of applications ranging from optical transceivers [70] to circuits for optical signal processing [71]. We designed Tx and Rx building blocks on the photonic wafer in form of DFB lasers with EAMs and PIN photodiodes with spot-size converters (SSC), respectively. The photonic and electronic wafers have been bonded and dies cut out from the full wafers. We report the performance of the photonic building blocks after bonding and the TPV process. The key component for the receiver is the pin photodiode. Its 3dB OE bandwidth after wafer bonding has been measured to reach 28 GHz as shown in Figure 17. The exact device could not be measured before bonding to avoid surface damage but typical bandwidth values are around 35 GHz. We assume that the degradation is linked to reflections from the SSC but more investigation is needed to explain the reduced bandwidth.

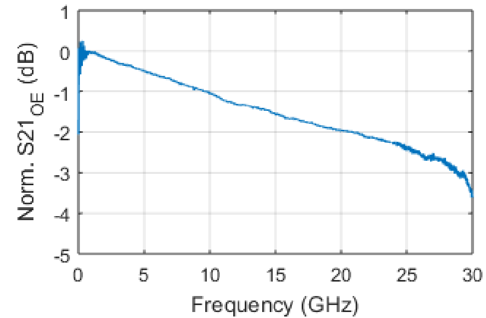

Figure 17: OE frequency response measurement of PIN photodetector building block after wafer bonding.

On the transmitter side, thermal dissipation becomes a challenge. The lasers are operated uncooled and initial DFB laser measurements with 4 µs current pulses at 100 mA with a 1 kHz duty cycle lead to laser operation at -4 dBm output power collected in fibre. It can also be pumped up to cw current of 35 mA and achieves -13 dBm optical power in fiber. Advanced heat extraction schemes from both the EIC and PIC are topics of ongoing research. Losses between the optical waveguide and the fibre are estimated at 6 dB in these preliminary measurements. The performance of the co-integrated transmitter and receiver circuits still needs to be characterized.

V. Conclusion

A wafer-scale approach for co-integration of photonics with electronics is presented in this paper, which promises to overcome the interconnect bottleneck of current wire or stud bump bonding techniques and establish broadband, high-density connectivity between PIC and EIC. Several challenges with respect to the interconnection scheme, the co-simulation framework and the technological realization are addressed and recent work on these aspects is reviewed. DC coupled driver-modulator connections reduce the interconnect complexity and are essential for wafer-scale co-integration. A circuit-based modelling framework is discussed that enables co-simulation of PIC and EIC so that impedance and equalization can be optimised. The proposed co-integration technology is based on polymer wafer bonding and subsequent TPV creation, which allows the combination of high-performance foundry photonics with foundry electronics. We have demonstrated its feasibility by creating 67 GHz TPV interconnects and verifying the operation of bonded photonic laser and detector building blocks. In light of on-going improvements in foundry photonics [16], [18] and the emergence of nanophotonic platforms [72] combined with faster electronic capabilities, we regard the proposed wafer-scale co-integration approach as an important step towards electronic photonic convergence.

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