Towards an Improved Model for 65-nm CMOS at Cryogenic Temperatures

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***Abstract*—Cryogenic CMOS is a crucial subcomponent of quantum-technological applications, particularly as control electronics for quantum computers. Simulation is an important first step in designing any CMOS circuit. However, the standard BSIM4.5 model is only applicable for temperatures between 230 K and 420 K. In this work, N-type MOSFETs with different dimensions in a 65-nm CMOS technology were characterized at room temperature and liquid helium temperature (4.2 K). These measurements were compared with corresponding simulations from the BSIM4.5 model. A model of drain current in the triode region was constructed, where key parameters, such as threshold voltage and effective mobility, were modified. By adjusting these temperature-dependent parameters, the modified model predicted the triode region currents with an error reduced to 7.6%. Thus, the modified model can be utilized to simulate transistor behavior in the triode region at cryogenic temperatures.**

Keywords—Cryo-CMOS, 65-nm CMOS technology, MOSFETs characterization, modeling, BSIM4

I. Introduction

With the potential to improve the computational power far beyond anything possible by transistor scaling, quantum computers promise to address many challenges currently intractable in existing computers [1]. They include the optimization of industrial chemical processes [2], and advanced mathematical analysis [3]. Quantum computers generally have two main components: a quantum processor, containing many coupled qubits, and a classical controller, which aims to manipulate and read out the states of these qubits [4]. The most promising qubit structures, such as trapped ions [5] and electron spins in quantum dots [6], are commonly operated at a cryogenic temperature, as low as tens of mK. Currently, control systems are generally placed at room temperature (RT), 300 K approximately, where the electrical connections to and from the cryogenic processors limit the number of qubits by thermal loads in the connecting cables, and latency in error-correcting loops [7].

One proposed alternative is to put the classical control system in close proximity to deep-cryogenic temperatures, where CMOS technology has proved to be a strong potential candidate [7], [8]. Because of the limited cooling power available on modern closed-cycle cryostats, only ultra-low power CMOS electronics can operate at a temperature environment adjacent to the quantum processors (about 20 mK), while more power-intensive components could in principle be operated at a higher-temperature stage in the cryostat, e.g. liquid helium temperature (LHT) 4.2 K [7]–[9]. Physical and electrical properties of various CMOS technologies under ultra-low temperatures have been investigated [10]–[20]. To design CMOS circuits for cryogenic applications, industry-standard transistor models compatible with ultra-low temperatures are essential. Thus, it is a priority to extend CMOS modeling to cryogenic temperatures.

This work aims to improve the low-temperature simulation accuracy by adjusting key parameters in a simplified model of triode-region current at LHT for a 65-nm CMOS technology. Section II introduces the relevant parts of the BSIM model. Section III presents simulations and measurements of 65-nm N-type MOSFETs at cryogenic temperatures, showing how the adjusted simplified model predicts the MOSFET behavior accurately at LHT. Section IV concludes the paper and discusses potential future work.

II. BSIM4.5 Model

A. General Modeling

BSIM (Berkeley short-channel IGFET model) is a series of accurate MOSFET models for electronic circuit simulations [21]. BSIM4 is a widely used version of the model, applicable to MOSFETs in sub-100 nm process nodes [22]. It comprises several sub-models that consider the basic physics behind the devices. It parametrizes the behavior of MOSFETs by considering parameters such as threshold voltage, unified mobility, and gate tunneling. Considered as a physics-based model, BSIM attaches fabrication procedure correlations or physical significance to most of its parameters while the others are introduced for the purpose of more accurate fitting and better modeling [23]. In BSIM4.5, the values of basic parameters for calculations are divided into groups. It is the designed transistor size that determines which group is used.

For current-voltage *(I-V)* characteristics there is a single-equation channel current model:

$$I_{ds} = \frac{I_{triode}\,NF}{1 + R_{ds}\,I_{triode}/V_{dseff}}\left[1 + \frac{1}{C_{clm}}\ln\left(\frac{V_{Asat} + V_{ACLM}}{V_{Asat}}\right)\right] \cdot \left[1 + \left(V_{ds} - V_{dseff}\right)/V_{ADIBL}\right] \cdot \left[1 + \left(V_{ds} - V_{dseff}\right)/V_{ADITS}\right] \cdot \left[1 + \left(V_{ds} - V_{dseff}\right)/V_{ASCBE}\right] \quad (1)$$

where I_{triode} is the current in the linear (triode) region, *NF* is the number of device fingers, V_{ds} is the drain-to-source voltage, V_{dseff} is an effective drain-to-source voltage, R_{ds} is the lightly doped drain (LDD) source/drain resistance, V_{Asat}, V_{ACLM}, V_{ADIBL}, V_{ASCBE}, V_{ADITS} are Early voltages due to current saturation, channel length modulation (CLM), drain-induced barrier lowering (DIBL), substrate current induced body effect (SCBE) and drain-induced threshold shift (DITS), respectively. This whole-range drain current equation (1) covers both linear and saturation regions. The current in the triode region, I_{triode} is defined as:

$$I_{triode} = \frac{W_{eff}}{L_{eff}}\mu_{eff}\,Q_{ch0}\,V_{ds}\,\frac{1 - V_{ds}/(2V_b)}{1 + V_{ds}/\left(E_{sat}\,L_{eff}\right)} \quad (2)$$

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TABLE I
DEVICES AND TEMPERATURE-DEPENDENT PARAMETERS

Parameters	**NMOS Devices (Nominal voltage = 1.2 V)**											
Transistor No.	***NMOS1***				***NMOS2***				***NMOS3***			
Dimensions *W*/*L* [nm]	500/120				1000/60				300/240			
Model type	Triode-region model		Foundry BSIM4.5 model		Triode-region model		Foundry BSIM4.5 model		Triode-region model		Foundry BSIM4.5 model	
Temperature	RT	LHT	RT	LHT	RT	LHT	RT	LHT	RT	LHT	RT	LHT
μ_{eff} [m^2/(Vs)]	**0.02276**	**0.02319**	**0.02309**	**3.51575**	**0.02484**	**0.02319**	**0.02107**	**4.4739**	**0.02198**	**0.02319**	**0.02447**	**2.2048**
Q_{ch0} [C/(m^2)]	**0.00098**	**0.00147**	**0.00112**	**0.00007**	**0.00104**	**0.00147**	**0.00134**	**0.00011**	**0.00171**	**0.00147**	**0.00189**	**0.00001**
V_b [V]	**0.13740**	**0.16165**	**0.14239**	**0.00072**	**0.11914**	**0.16165**	**0.26746**	**0.00095**	**0.17047**	**0.16165**	**0.12980**	**0.00065**
E_{sat} [kV/m]	**51.288**	**7813.07**	**55.790**	**66.943**	**80.297**	**7813.07**	**78.779**	**9443.98**	**9990.59**	**7813.1**	**9899.12**	**12696.4**

where Q_{ch0} is the charge density for subthreshold and inversion regions, μ_{eff} is the effective mobility, W_{eff} and L_{eff} are the effective dimensions, E_{sat} is a critical electric field in the channel at which the carrier velocity saturates and V_b is an intermediate quantity defining the bulk charge effect. It should be noted that Q_{ch0}, μ_{eff}, E_{sat}, V_b are functions of gate-to-source voltage (V_{gs}) [22]. This paper is limited to modeling I_{triode} down to LHT.

B. Temperature Dependence and Limitations

In the BSIM model, all the parameter extractions are implemented at a nominal temperature *TNOM* (=298 K for technology in this work). In consideration of parameters sensitive to operating temperature, BSIM4.5 treats the energy band gap and intrinsic carrier concentration of silicon as functions of device temperature. It also contains an intrinsic temperature dependence model to extend the flexibility of threshold voltage, mobility, saturation velocity and LDD resistance etc. For instance, the threshold voltage V_{th} varies with temperature *T* as described by:

$$V_{th}(\mathrm{T}) = V_{th,TNOM} + \left(kt1 + \frac{kt1l}{L_{eff}} + kt2\, V_{bseff}\right)\left(\frac{T}{TNOM} - 1\right) \quad (3)$$

where $V_{th,TNOM}$ is the threshold at *TNOM*, $kt1$ and $kt1l$ are the temperature effect and its channel-length dependence respectively, $kt2$ is a body-bias coefficient and V_{bseff} is the effective body-source bias.

Apart from the more advanced temperature model, BSIM4 has shown advances in many aspects when simulating MOSFET behavior, such as improving the accuracy accounting for effects of nonuniform vertical and lateral doping, covering the quantization effect of inversion charge layer etc. Nonetheless, it is valid only for a temperature range from 230 K to 420 K [24], which means that for most parameter values, even some key equations are not accurate under cryogenic conditions.

III. ADJUSTED MODEL FOR LHT

In this work, NMOS transistors with different dimensions were fabricated in a 65-nm CMOS technology. Dimensions of three example devices are listed in Table I. Each dimension has a unique W/L ratio. Thus, NMOS1-3 employs different groups of parameters in BSIM4.5. These devices were tested at both RT and LHT. The measurements were carried out in a TTPX probe station [25], in which the whole enclosed system surrounding the sample chips was cooled in liquid helium for cryogenic measurements. By separately sweeping the DC voltages supplied at drain and gate, with a zero bulk bias, the drain current is characterized as a function of V_{ds} and also of V_{gs}. For each W/L dimension in Table I, three devices were tested, giving consistent results. It should be noted that this paper only presents one group of the results. And during low temperature testing, the temperature of the chips was maintained at 4.5 K.

A. Breakdown of BSIM Simulations at LHT

Fig. 1 shows how the simulated *I-V* curves from BSIM4.5 model fail to accurately model transistor behavior at LHT. The default BSIM model predicts a very small triode region, and much higher saturation currents than those measured. In general the BSIM model predicts the saturation region current to be much larger than measured values (up to +24% in this case). Modifications to the foundry model are required, which may involve further parameter extractions for low temperatures, additional temperature dependence of key variables or appending new parameters.

B. Cryogenic Characteristics and Underlying Physics

To determine how to adjust the model, the underlying physics in the MOSFETs must be considered. As temperature decreases, carrier concentration and energy band gap in the semiconductor become the first to be affected [19], [26]. This means subsequent influence on the quantization of inversion layer, the scattering mechanisms, the impact ionization effect and the parasitic resistances.

An accurate threshold voltage model is crucial to predict the electrical behavior of MOSFETs. BSIM4 [22] utilizes a long-channel threshold with uniform doping and considers offsets resulting from nonuniform vertical and lateral doping, short- and narrow-channel effect, and DIBL. To provide a practical derivation of the threshold voltages they are

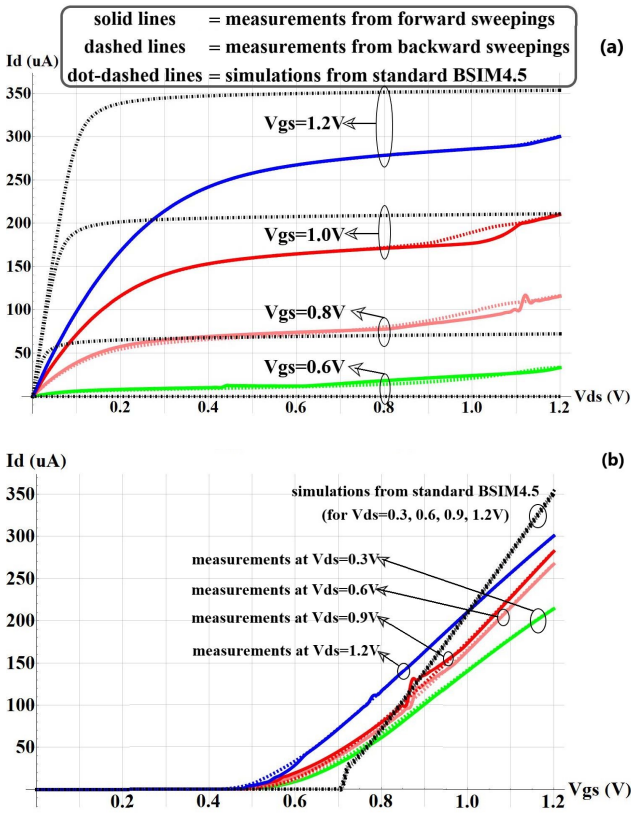

Fig. 1. Breakdown of simulations from BSIM4.5 model at LHT for characteristics of (a) I_d-V_{ds} and (b) I_d-V_{gs} for NMOS1.

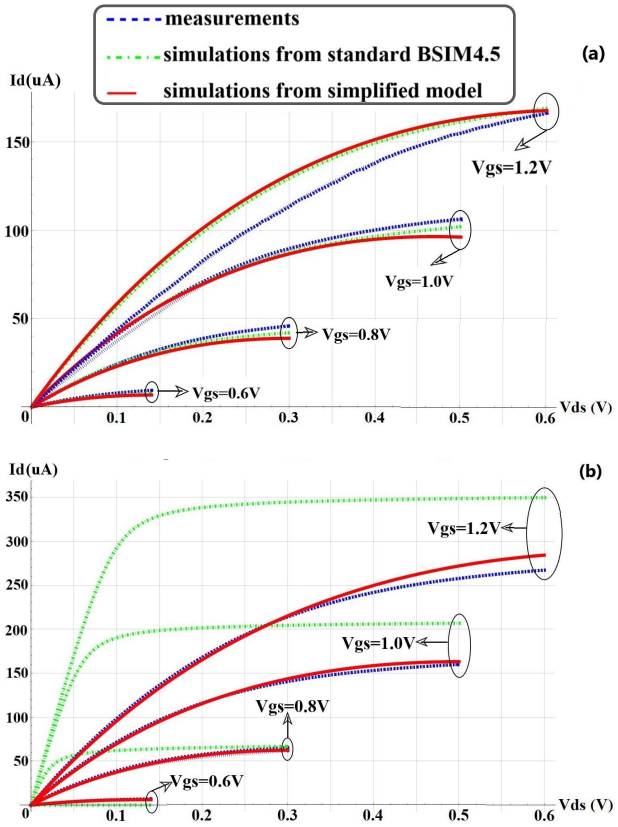

Fig. 2. Comparison between measurement and models at (a) RT and (b) LHT for NMOS1.

calculated by an engineering methodology recommended in the BSIM model [27]. The variation in gradient of an I_d-V_{gs} curve is computed to find the gate supply at which the corresponding transconductance is maximum. The tangent at this point cuts $I_{ds} = 0$ at a value of V_{gs0}, and finally the threshold is given by $V_{th} = V_{gs0} - 0.5V_{ds}$. In practice, the threshold obtained by this method is slightly smaller than that from BSIM model. This is because the applied V_{ds} is higher than the value in the theoretical V_{th} definition. Barrier lowering due to drain voltage is more evident in a MOSFET with a shorter channel.

When an NMOS device is cooled, there exist fewer free electrons to be attracted by a given gate supply as a result of declining impurity ionization. Therefore, a larger V_{gs} is desirable to form the channel under the gate and make the transistor 'turn on' [23]. In the LHT measurements, V_{th} at V_{ds}=0.3 V increased by 0.110 V, 0.143 V and 0.126 V in NMOS1, NMOS2, and NMOS3 respectively, while the built-in T-dependent model of (3) predicts an increment ranging from 0.233 V to 0.267 V. Fig. 1(b) shows an obvious disagreement about the thresholds between the simulations from standard model and the measurements at LHT.

As temperature goes down, the slopes of currents in linear region are noticeably increasing. One of the direct temperature dependent factors is the mobility of carriers inside the inversion layer, which are determined by three mechanisms: phonon scattering due to lattice vibrations in semiconductor material, Coulomb scattering related to ionized impurity atoms and surface roughness scattering caused by disorders at the interface [26]. Which mechanism dominates is dependent on conditions such as doping levels, operating temperature and imperfections in fabrication. At cryogenic temperatures, because of the evident lower ionization rate and reduction in lattice vibrations, free carriers in the inversion layer should be more free to transport in the channel, which provides improved mobility [23], [24].

There are two main nonidealities for LHT behavior: kink and hysteresis. Fig. 1(a) shows these phenomena in the saturation region. The magnitude of current in the device channel depends on the density of majority carriers there, which can be affected by two factors, ionization and externally applied electric field. Under LHT, both the source/drain region and substrate 'freeze out', i.e. they are in an extremely low ionization level [19][29][30]. With an increasing V_{ds} in an NMOS device, more and more electrons gather in the channel region due to the gradually stronger field, forming a suppression to the freeze-out effect. It appears as if the device turns on for a second time, and source-drain parasitic resistance is reduced by such cryogenic environment, but then back to normal when V_{ds} is high enough [31]. On the other hand, the whole depletion region does not share a common potential. The impact ionization substrate current, generated in the space charge region around the drain, would partly flow to the source through the substrate and result in an increase of internal substrate potential in the depletion region. If so, this would cause a lower threshold at a sufficiently positive V_{ds} [32], bringing about a sudden rise in I_{ds}. Another obvious nonideal phenomenon is the deviation in currents when the voltage is swept in an inverse direction (hysteresis). At each fixed V_{gs}, V_{ds} was swept forward and backward in a range of 0-1.2 V at a steady rate of 0.01 V/s. However, both kink and

hysteresis make little difference in triode region, and thus currents there are easier to model more accurately.

C. Modeling and Analysis

A simplified triode-region current model was constructed with the aid of Mathematica, based on the triode region sub-model from BSIM4.5. The main equation in the model here is (2). It refers to BSIM4.5 sub-models relevant to DC drain current behavior, including the effective channel dimension model, threshold voltage model, channel charge density model, asymmetric source/drain resistance model and mobility model, while the capacitance-voltage properties are excluded.

This model makes it convenient to directly change parameter values, and adjust the simulations to fit measured data. In addition to V_{ds}, as shown in (2), there are six parameters. The effective dimensions W_{eff} and L_{eff} rely on the offsets due to mask or etch effects and doping profile. Since these parameters are determined by fabrication, it is reasonable to assume they are unaffected by temperature. The optimum values of the other four parameters were each determined by procedurally fitting the simulation current to the measured current and adjusting the parameters appropriately.

In order to prove the feasibility of the simplified model, it was first tested at room temperature. Since the standard BSIM4.5 model is accurate at room temperature, these 'standard' simulation results can act as a reference or an evaluation criterion on how accurate the simplified model is. Since the simplified model is based on a subcomponent of the full BSIM model, the predicted currents from the two should agree in the triode region provided they have the same parameters. Fig. 2(a) shows how the simplified model matches the BSIM model closely at room temperature in the triode region. The deviations are primarily affected in two respects. Firstly, there are excluded sub-models which also have an impact on device *I-V* behavior, such as the tunneling current sub-model [22]. Secondly the border between linear and saturation regions is variable (dependent on V_{gs}), disturbing the fitting results.

By adjusting values of the parameters μ_{eff}, Q_{ch0}, V_b and E_{sat}, the simplified model achieves better matching to LHT measurements at different V_{gs} values, as shown in Fig. 2(b). This model predicted the triode region currents with a greatly improved performance (up to 7.6% error for all three different transistor dimensions). Table. I shows the calculated RT and LHT results of μ_{eff}, Q_{ch0}, V_b and E_{sat} at V_{gs}=0.6 V from the simplified triode-region current model and the foundry BSIM4.5 model. According to the simplified model, the effective mobility at LHT does not increase so dramatically as predicted by the standard BSIM4.5 model. To associate the μ_{eff} changes with most fundamental parameters' variations, one of the easiest ways is via the low field mobility parameter *u0*. In the mobility sub-model of BSIM4.5, μ_{eff} is directly proportional to *u0*. Thus, the changes of μ_{eff} can be regarded as a result of temperature dependence of *u0*. Furthermore, based on the definition of $E_{sat} = 2\,vsat/\mu_{eff}$, where $vsat$ is a basic parameter, the saturation velocity relates E_{sat} to μ_{eff}. Hence, by simply adjusting two basic parameters in the model, *u0* and $vsat$, one can make μ_{eff} and E_{sat} applicable to LHT simulations for triode-region current. Q_{ch0} and V_b have intricate expressions in the model, and this complicates finding an appropriate fundamental parameter to change for each of them. Further investigation is required in the future to find out which basic parameters are most responsible for simulation error at LHT. It is also worth noting that this work focuses on determining best-fit numerical results to adjust the triode region model to be more accurate at LHT. Future work will cover a wider MOSFET dimension range, characterize P-type transistors as well, and involve investigating trends in these adjusted parameters to relate them more closely to the cryogenic physical behaviors in a more generalized CMOS model.

IV. Conclusion

In comparison with RT behaviors, the LHT *I-V* characteristics of N-type MOSFETs in 65-nm technology have shown increased transconductances, higher thresholds, enhanced mobilities and nonidealities including kinks and hysteresis. The parameter values of the triode-region current model, which is simplified from BSIM4.5 model, have been modified by fitting the adjusted model to measured LHT triode-region currents. The simplified model predicts drain currents more accurately in the triode region at LHT with an error of up to 7.6%. This adjusted model is a first step to making a fully characterized model for cryogenic CMOS design and simulation. The focus here is on finding best-fit numerical results to make the triode region model more accurate at LHT. Investigations into temperature-dependent trends of these adjusted parameters will be a future step to tie the model more closely to the cryogenic physical behavior.

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