

# A CMOS Analog Front-End for Implantable Pulmonary Artery Pressure Monitoring System

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**Abstract**—This paper presents an energy-efficient analog front-end circuit to monitor the pulmonary artery pressure (PAP) with piezoresistive pressure sensors. A low-power capacitively-coupled instrumentation amplifier (CCIA) is developed in order to boost the amplitude of the bridge sensor to the input range of the analog-to-digital converter (ADC). The  $1/f$  noise and input-referred offset of the amplifier are eliminated by the chopping technique. Simulation results show that this CCIA with chopping technique achieves an input-referred noise density of  $38.7 \text{ nV}/\sqrt{\text{Hz}}$  and an input-referred offset voltage of  $4 \text{ }\mu\text{V}$  with a current consumption of  $4.28 \text{ }\mu\text{A}$  at  $1.8 \text{ V}$  voltage supply. This gives a noise-efficiency factor (NEF) of 3.1. Dual supply voltages are used to decrease the power consumption of the bridge sensor. The pressure range is selected to be between 0 and  $125 \text{ mmHg}$  and the bandwidth of the interface is set from DC to  $400 \text{ Hz}$  with an RC low pass filter (LPF). This low-noise, low-offset analog front-end circuit achieves an accuracy of  $0.125 \text{ mmHg}$ .

**Index Terms**—heart failure (HF), pulmonary artery pressure (PAP), Wheatstone bridge sensor, capacitively-coupled instrumentation amplifier (CCIA), chopping technique.

## I. INTRODUCTION

Heart failure (HF) disease occurs when the heart muscles cannot pump enough blood as well as body needs. HF is one of the most important issues faced by mankind in the 21<sup>st</sup> century as it affects around 26 million people worldwide, and it is a leading cause of morbidity and mortality [1], [2]. Furthermore, the pulmonary hypertension (PH) is also a serious cardiac disease which has a strong relation with HF [3]. It is important to continuously monitor the heart activity, especially the pulmonary artery (PA) pressure, in order to adapt the treatments based on how the patients reacted to the prescribed drugs. PH is defined when a mean PA pressure (PAP) exceeds  $25 \text{ mmHg}$  [3], and the close tracking of the PAP is crucial to diagnose PH and HF. [2]. The state-of-the-art device in the arena of implantable hemodynamic monitoring is the PAP monitoring system called as CardioMEMs HF System [4]. It is based on a passive capacitive pressure sensor, which can be placed into a branch of the pulmonary artery to record the variations in blood pressure [2], [4].

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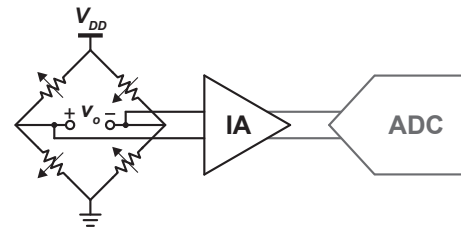


Fig. 1. Bridge readout system.

The PAP can also be monitored by an implantable active system based on a pressure sensor and its readout integrated circuit (IC). With a low-noise and low-offset readout IC (ROIC), the PAP can be monitored with high-accuracy. Fig. 1 represents a conventional pressure sensor readout consisting of an instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). The wireless powering and communication with deeply implanted system can be established by ultrasound. Thus, a high voltage (HV) CMOS technology is chosen to have a compact solution for both power management and sensor interface part.

In order to measure the PAP, a piezoresistive pressure sensor based on Wheatstone bridge is selected. Thanks to its simplicity, reliability, low manufacturing cost, size and accuracy, piezoresistive sensors represents the most widely used conditioning circuit to monitor pressure, humidity and temperature [5]–[8].

This paper presents an energy-efficient capacitively-coupled IA (CCIA) to boost the amplitude of the bridge output to the input range of the ADC for continuous monitoring of the PAP. In order to have an accurate and energy-efficient pressure sensing system, the IA must have low power consumption, low input-referred noise, low-offset, high common-mode rejection ratio (CMRR) and high input impedance. The capacitively-coupled chopper amplifier offers the best conditions in terms of both energy efficiency and accuracy [9]. Simulation results show that this ROIC based on CCIA with chopping technique and designed in a  $0.18 \text{ }\mu\text{m}$  HV CMOS process achieves an input-referred noise density of  $38.7 \text{ nV}/\sqrt{\text{Hz}}$ , an input-referred offset voltage of  $4 \text{ }\mu\text{V}$  and a noise-efficiency factor (NEF) of 3.1 with a current consumption of  $4.28 \text{ }\mu\text{A}$  at  $1.8 \text{ V}$  supply.

## II. SYSTEM DESIGN OF THE READOUT CIRCUIT

Patients are considered at risk for heart failure hospitalization if their pressures are above the range of 15 to 35 mmHg for systolic, 8 to 20 mmHg for diastolic and 10 to 25 mmHg for mean PAP [2]. In order to cover these extreme pressure limits, such as systolic PAP of pediatric patients, the pressure range is selected to be 0 to 125 mmHg with an accuracy of 0.125 mmHg. A low-noise, low-offset and low power CCIA with chopper technique is developed to amplify the differential output signal of the piezoresistive sensors to the input range of the ADC. The bandwidth of the system is set from DC to 400 Hz with an RC low pass filter (LPF).

### A. Pressure Sensor

A piezoresistive pressure sensor is chosen due to its simplicity, reliability and high accuracy. On the other hand, piezoresistive sensors have the drawbacks of zero-pressure offset voltage and thermal drift [5], [8]. Since the pressure sensor in this application intends to measure the blood pressure in PA, it will work under stable temperature conditions. The temperature drift is negligible and does not affect the system. The main challenging part of the Wheatstone bridge is handling the zero-pressure offset caused by mismatch of piezoresistive elements during fabrication. In order to avoid saturation of amplification stages due to offset voltage, the input range of the amplifier covers both worst-case zero-pressure offset plus the differential signal to monitor the pressure.

A commercial piezoresistive pressure sensor with a pressure range of 250 mmHg is selected, and its half pressure range up to 125 mmHg is monitored effectively. At 5V biasing voltage, the sensor has a typical voltage span of 44 mV in 0 to 125 mmHg pressure range and a worst-case zero-pressure offset of -22 mV. The value of bridge resistors is 5 k $\Omega$ .

### B. CCIA based on Dual Supply Voltages

In order to have an accurate and energy-efficient sensing system, the readout circuit must have low power consumption, low-offset, low input-referred noise, high common-mode rejection ratio (CMRR) and high input impedance [6], [8].

The instrumentation amplifier determines the energy efficiency of the system, since the main noise contribution comes from its input stage. The classic 3-Opamp IA and the current-feedback IA (CFIA) have two noise critical input stages, while capacitively-coupled instrumentation amplifiers have only one. As a result, CCIA's are generally more energy-efficient than 3-Opamp and CFIA's [9]. In addition, their input capacitors block the common-mode (CM) input voltages of the Wheatstone bridge and allow using different supply voltages for the resistive bridge and the readout circuit [8].

The ROIC is powered by 1.8V power supply voltage. For the piezoresistive sensor, there is a trade-off between the bridge sensitivity and the power dissipation. In general, the bridge sensor is powered from a supply voltage higher than the readout circuit to improve the bridge sensitivity [8]. Since this application will be implanted in the human body, the main target of the system is low power consumption. In

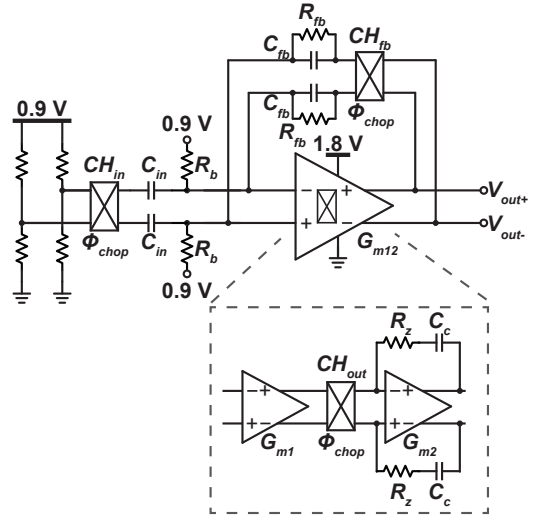


Fig. 2. Dual supply sensing system using CCIA.

case the resistive bridge is powered by 1.8 V, its current consumption becomes 360  $\mu$ A with 5 k $\Omega$  bridge resistors and it consumes 648  $\mu$ W power. However, this power consumption is high for biomedical implants. Thus, the supply voltage of the piezoresistive sensor is reduced by a factor of two which leads to an improvement by a factor of four in power consumption (162  $\mu$ W). In addition, it decreases the voltage span of the sensor, but the sensitivity of the system can be enhanced by a low-noise and low-offset amplification stage. The CM level of the bridge is 0.45 V while the CM level of the CCIA is 0.9 V. At 0.9 V biasing voltage, the maximum voltage span of the sensor is  $\pm$ 5 mV while its worst-case zero-pressure offset is  $\pm$ 8 mV. Thus, the input range of the CCIA is selected to be  $\pm$ 13 mV and the gain is chosen to be 52 in order to amplify the sensor output signal to the level of the input of the ADC with an input range of  $\pm$ 676 mV.

Fig. 2 represents the system, which consists of a bridge pressure sensor and a CCIA with chopping switches. The CCIA consists of a two-stage Miller-compensated opamp ( $G_{m1}$  and  $G_{m2}$ ), three chopper switches ( $CH_{in}$ ,  $CH_{out}$  and  $CH_{fb}$ ), a capacitive feedback to set the gain ( $C_{in}$ ,  $C_{fb}$ ) and high-value pseudo-resistors ( $R_b$ ,  $R_{fb}$ ) to set input CM level.

### C. Chopping Technique

The chopping technique is a modulation method that can be employed to suppress the  $1/f$  noise and input-referred DC offset voltage of the opamp. The input chopper switches convert DC and low frequency input signals to AC signals that are then capacitively-coupled to the input of 1<sup>st</sup> stage amplifier,  $G_{m1}$ . Since the offset and  $1/f$  noise of  $G_{m1}$  is up-modulated away from DC by the switches at its output, a microvolt offset and very low  $1/f$  noise can be achieved [10].

The chopper frequency,  $f_{chop}$ , is selected to be higher than  $1/f$  noise corner in order to remove  $1/f$  noise completely. Due to mismatched charge injection and clock feedthrough at the input chopper switches, residual offset occurs, which is

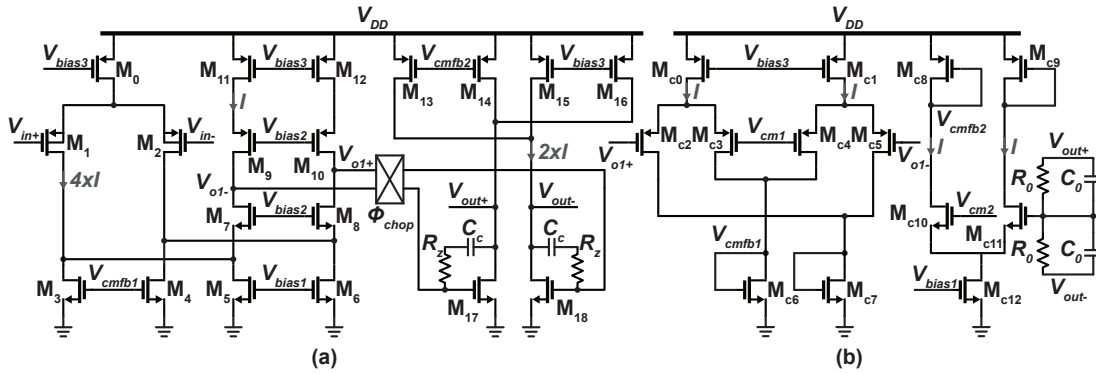


Fig. 3. Schematics of (a) the Miller compensated two-stage amplifier with demodulating chopper, (b) CMFB circuits for the first and second stages.

proportional to  $f_{chop}$  [10]. Thus, there is a trade-off between noise and residual offset. To decrease the charge injection and clock feedthrough, minimum size switches can be used, however in ultra-low-noise applications, the noise of on-resistance of chopper switches may not be negligible. Thus, the width of the switches can be increased to decrease the on-resistance. In our application, the noise of the switches is negligible, and minimum size switches are used.

The major drawback of this technique is that up-modulated offset and  $1/f$  noise appears as output ripple that must be eliminated. The amplitude of the ripple is estimated by [11]

$$V_{ripple} = \frac{V_{offset} \times G_{m1}}{2 \times f_{chop} \times C_c}. \quad (1)$$

Another disadvantage is that the input impedance of the opamp decreases with increased  $f_{chop}$  [11]. The chopper frequency should be chosen carefully, since it affects input-referred noise, output ripple, residual offset and input impedance. In this application, the chopper frequency is selected to be 40 kHz in order to be higher than  $1/f$  noise corner and also high enough to suppress the output ripple by a 1<sup>st</sup> order LPF with a cut-off frequency of 400 Hz.

### III. TRANSISTOR LEVEL IMPLEMENTATION

#### A. Two-Stage Opamp of the CCIA

The gain of the CCIA is set to 52 by capacitors  $C_{fb}$  and  $C_{in}$  to amplify the sensor output signal to the level of the input range of the ADC. In order to have a gain error less than 0.1% and to achieve a high linearity, a two-stage Miller RC compensated amplifier with a DC gain of 103 dB is designed (Fig. 3a). The first stage consists of a chopped folded-cascode amplifier with a PMOS input pair biased in weak inversion to achieve high gain. Since the noise of the system is dominated by the input pair, large PMOS transistors are employed (500  $\mu\text{m}/0.5 \mu\text{m}$ ).

The demodulating chopper switches are placed between the output of 1<sup>st</sup> stage and input of 2<sup>nd</sup> stage to suppress the  $1/f$  noise and the input-referred offset of the folded-cascode amplifier. The  $1/f$  noise and offset of the following stages are minimized by the high gain of the 1<sup>st</sup> stage amplifier. The second stage is a common source (CS) amplifier that has a

high output swing. The currents that circulate in the folded branches are scaled by a factor of four, and the currents that flow in the common source branches are scaled by a factor of two to enhance the NEF. The contribution of the active load devices to the input-referred noise is minimized.

In order to ensure stability in any mismatch and process condition, RC compensation is used. The Miller compensation capacitors  $C_c$  are selected to be 30 pF to ensure stability and also to suppress the ripple (Eq. 1). The  $G_{m1}$  is 22.5  $\mu\text{S}$  and the unity-gain frequency of the CCIA is 120 kHz.

#### B. Common-Mode Feedback (CMFB) Circuits

Two separate CMFB circuits are developed to adjust the output CM voltages of the two stages and are shown in Fig. 3b. Since the first stage does not need high output swing and has very high output resistance, the CMFB topology based on two differential pair is selected. This topology does not limit the amplifier output resistance, however limits the differential amplifier output swing. The CM reference voltage of the first stage ( $V_{cm1}$ ) is set to 0.8 V to bias the input pair of the second stage ( $M_{17}, M_{18}$ ) at this value in order to achieve high output swing in the second stage.

On the other hand, the CMFB topology based on a resistive divider and an amplifier is chosen for the second stage because a large voltage output swing is required at the output. Although the resistive divider limits the output resistance, and thus the gain of the second stage, it is not a significant problem since the majority of the gain comes from the first stage. The CM reference voltage of the second stage ( $V_{cm2}$ ) is set to 0.9 V to have the maximum possible output swing.

#### C. Low Pass Filter (LPF)

A passive first order RC LPF is selected to remove the chopper ripple. In order to achieve a cut-off frequency at 400 Hz, high-value resistors and capacitors are used. Furthermore, the chopper frequency is selected to be high enough to suppress the output ripple sufficiently by a 1<sup>st</sup> order RC LPF.

As a future work, an AC-coupled ripple reduction loop (RRL) [6], [11] will be designed to suppress the chopper ripple. The system with RRL offers more design flexibility and  $C_c$  and  $f_{chop}$  can be reduced to save chip area, to decrease the residual offset and to increase the input impedance.

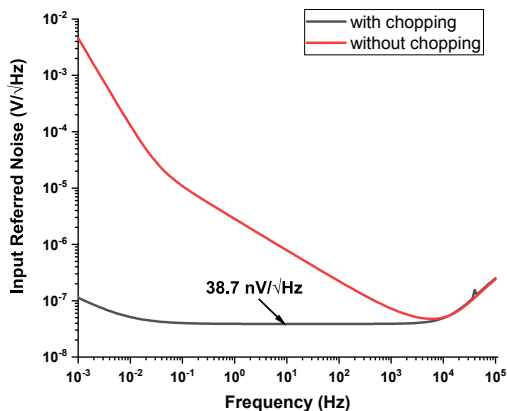


Fig. 4. Simulation results of input-referred noise density.

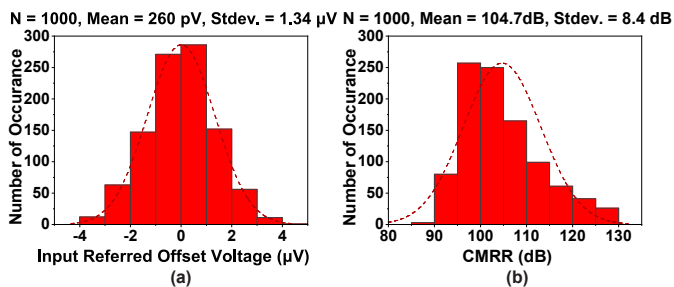


Fig. 5. Simulation results of (a) input-referred offset voltage and (b) CMRR.

#### IV. SIMULATION RESULTS

The CCIA with chopper switches is designed in a 0.18  $\mu\text{m}$  HV CMOS technology. The input range is selected to be  $\pm 13$  mV in order to cover both the differential output ( $\pm 5$  mV) and also the worst-case offset ( $\pm 8$  mV) of the bridge sensor. The gain of the amplifier is set to 52, and the output swing of the amplifier is limited to  $\pm 676$  mV. The performance parameters of the ROIC has been simulated in Cadence. Fig 4 shows that an input-referred noise density of 38.7 nV/ $\sqrt{\text{Hz}}$  is achieved with a 5 mHz 1/f noise corner in 400 Hz bandwidth at  $f_{\text{chop}} = 40$  kHz. In order to simulate the input-referred offset and CMRR, Monte Carlo simulations were run for 1000 samples. An input-referred offset of 4  $\mu\text{V}$  is achieved in  $3\sigma$  worst-case corner (Fig. 5a). The mean value of the CMRR is 104.7 dB with a  $\sigma$  of 8.4 dB (Fig. 5b).

This analog front-end circuit consumes 4.28  $\mu\text{A}$  at a 1.8 V voltage supply. The simulated input-referred noise density and the low current consumption give an NEF, defined as

$$NEF = v_{n,in} \sqrt{\frac{2I_{tot}}{\pi U_T 4kT}} \quad (2)$$

equal to 3.1.

The performance parameters of this work are summarized in Table I and compared to the state-of-the-art results published for bridge sensors. The selected works [5], [6], [8] report the measurement results for both IA and ADC parts together. This work shows simulation results only for the IA.

TABLE I  
COMPARISON WITH STATE-OF-THE-ART ROICs

	This Work	[5]	[6]	[8]
<b>Architecture</b>	CCIA	IA + SAR	CFIA + DT $\Delta\Sigma\text{M}$	CCIA + CT $\Delta\Sigma\text{M}$
<b>Technology (<math>\mu\text{m}</math>)</b>	0.18	0.35	0.7	0.18
<b>Supply Voltage (V)</b>	1.8	3.3	5	1.8
<b>Current Consumption (<math>\mu\text{A}</math>)</b>	4.28	61	270	1200
<b>Offset (<math>\mu\text{V}</math>)</b>	4	-	0.05	7
<b>Input Noise Density (nV/<math>\sqrt{\text{Hz}}</math>)</b>	38.7	191	16.2	3.7
<b>NEF</b>	3.1	58	10.4	5.0

#### V. CONCLUSION

This paper presents a readout IC to monitor the PAP with piezoresistive pressure sensors. An energy-efficient CCIA is developed to amplify the sensor signal to the level of the input range of the ADC. Chopping technique is employed to remove the 1/f noise and input-referred offset. Dual supply voltages are used to decrease the power consumption of the sensor. Simulation results show that the proposed ROIC draws 4.28  $\mu\text{A}$  from a 1.8 V power supply, and achieves an input-referred noise density of 38.7 nV/ $\sqrt{\text{Hz}}$ , an input-referred offset of 4  $\mu\text{V}$  and an NEF of 3.1. This ROIC is suitable to measure the PAP in a pressure range of 0 to 125 mmHg with an accuracy of 0.125 mmHg in 400 Hz bandwidth.

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