An Implantable Versatile Electrode-Driving ASIC for Chronic Epidural Stimulation in Rats

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***Abstract*—This paper presents the design and testing of an electrode driving application specific integrated circuit (ASIC) intended for epidural spinal cord electrical stimulation in rats. The ASIC can deliver up to 1 mA fully programmable monophasic or biphasic stimulus current pulses, to 13 electrodes selected in any possible configuration. It also supports interleaved stimulation. Communication is achieved via only 3 wires. The current source and the control of the stimulation timing were kept off-chip to reduce the heat dissipation close to the spinal cord. The ASIC was designed in a 0.18-μm high voltage CMOS process. Its output voltage compliance can be up to 25 V. It features a small core area (<0.36 mm^2) and consumes a maximum of 114 μW during a full stimulation cycle. The layout of the ASIC was developed to be suitable for integration on the epidural electrode array, and two different versions were fabricated and electrically tested. Results from both versions were almost indistinguishable. The performance of the system was verified for different loads and stimulation parameters. Its suitability to drive a passive epidural 12-electrode array in saline has also been demonstrated.**

***Index Terms*—Application specific integrated circuit (ASIC), electrode array, electrode driver, epidural stimulation, implantable electronics, low power, rats.**

I. Introduction

In spinal cord injured (SCI) individuals, the neural pathway between the brain and the extremities is damaged, to some extent paralyzing the lower extremities. Recent advances in the field of neuroscience have suggested that epidural spinal cord stimulation (ESCS) can facilitate recovery of bladder function, standing and perhaps locomotion in SCI humans ([1], [2]). Some rat studies have supported this concept [3], but further testing is required to increase our understanding and optimize the stimulation parameters. Testing protocols are currently limited by the available technology.

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More specifically, the number of electrodes one can use seriously limits the paradigms that could be investigated. For this reason, electrode arrays, as opposed to the conventional pairs of electrodes, can be used to investigate the effect of ESCS at different sites. The development of epidural electrode arrays for chronic testing in rats is a challenging task due to their small size [4]. The difficulties increase radically when a larger number of electrodes need to be independently controlled. It has been well documented in the literature [5] that a large number of connections is highly undesirable because it either makes the implantation procedure more challenging, or, if the device is successfully placed in the body, it could imperil perfusion, result in infections, tissue damage [6], or simply cause the device to fail [7].

We are involved in a European research project (NEUWalk), which focuses on the development of neuroprosthetic concepts for restoration of motor functions in individuals with severe spinal cord injury. To demonstrate the approach we are combining ESCS with pharmacology to promote the recovery of full weight bearing walking in paralyzed SCI rats [8]. Epidural implants for rats including up to 8 electrodes have been successfully developed and chronically implanted. To test a new paradigm, at least 12 electrodes are required but this has not been possible so far, mainly due to the increased number of connections. Our approach is to develop application specific integrated circuits (ASICs) to be placed on the array, acting as electrode drivers, reducing the number of connections, while providing the necessary versatility for the testing.

Placing electronic drivers close to the electrodes is not a new concept ([9]–[13]). Although this list is not exhaustive, it includes some indicative systems, giving an overview of what has been reported so far. In the majority of these systems, an external hub is connected to the driver chip via a number of wires, usually between 7 and 5. These are used to send data, control information, synchronization pulses, and power to the chip at the same time. The amplitude of the stimulus current is conventionally generated on chip by integrated current digital-to-analog converters (DACs) (with the exception of [12], where the stimulus generator chip is stacked on the output stage chip), while the timing of the stimulation can be controlled either on chip, using dedicated timers [10] or integrated clocks, or be assigned off chip ([9], [12]). Also, random-access memory (RAM) has been used to store the chosen stimulation patterns locally, to minimize the information sent by telemetry when a larger number of electrodes is to be addressed [10]. In these systems, the electrodes can either be selected in any configuration, usually using a dedicated DAC for each electrode, or in predefined configurations, such as tripoles [13]. They are normally

powered using voltages of 10 V or higher, to allow for stimulation in cases where the load impedances are large, or high currents are required. In [12], charge pumps are used in the output stage to generate the required ± 9 V. The final size of the chips is between 4.8 mm^2 to 27.3 mm^2, and the power consumption is in the range of 450 μW up to 30 mW, depending on the number of channels and the functionality.

There is also a variety of implantable stimulating systems for use in rats ([14]–[24]), but almost all of them are designed for implantation in parts of the body where size is not of such concern, and they are also mostly intended for acute experiments. To the best of the authors' knowledge there are only three other currently reported systems aiming to stimulate the rat's spinal cord. In [19] and [22] the number of electrodes used is limited to two. More recently, an epidural electrode array was reported in [24]. This features 27 electrodes which are driven bipolarly by an external control box connected via 12 wires to 10 implanted multiplexing chips implemented by discrete off-the-shelf components on a 10.3 mm $\times$ 33.2 mm printed circuit board.

We have developed an electrode driver, capable of driving 13 electrodes (12 on an epidural electrode array and 1 implanted subcutaneously), through one channel (i.e., one independent current source), in any possible configuration, while communicating via only 3 wires. One or more electrodes can be selected as cathodes or as anodes for each stimulus pulse, allowing full flexibility. The timing of the stimulation is controlled off-chip, so that no power-consuming on-chip clock is required. In addition, to keep the power dissipation low in the epidural region, we have chosen to separate the current source from the driving circuitry, keeping the generation of the amplitude of the stimulus current also external to this ASIC. It is part of a fully implantable stimulating system we are currently developing to be used in freely moving animals in the future (graphically illustrated in Fig. 1). In this system, the active electrode array is placed epidurally and communicates with a subcutaneous hub via 3 wires. The subcutaneous hub comprises a microcontroller (μC), a current source, a dc-dc converter and a battery. It can be reprogrammed and recharged via a connector fixed on the head of the rat.

In this paper, we describe the complete design details of the electrode driving ASIC and present its experimental evaluation with measurements that verify its performance (the simulated performance of some blocks has been previously presented in [25]). We also discuss here some details of the first (non-implantable) version of the hub. The rest of this paper is organized as follows. Section II sets the specifications of the system. Section III presents the system design from the point of view of both its layout and its operation. Circuit details are discussed in Section IV and design details of the first version of the hub in Section V. Section VI presents measured results, and Section VII concludes the paper with a discussion and a comparison.

II. System Specifications

A. Area and Power Considerations

Apart from the flexibility in electrode configurations and the limited number of inputs, the electrode driver needs to fulfill several other requirements. The fact that it is to be integrated

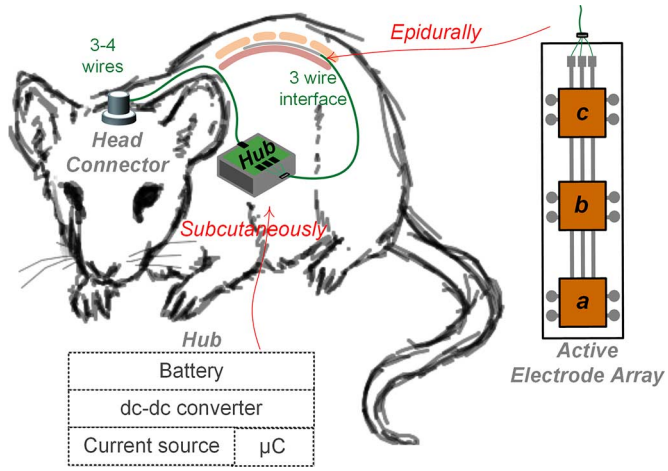

Fig. 1. Fully implantable stimulating system under development. This paper discusses the design and testing of the ASICs to be embedded on the active electrode array, as well as some details of the performance of the first non-implantable version of the hub. Grey circles and orange rectangles a, b, and c represent electrodes and ASICs, respectively (see Section III-A). Only the electrodes on the array are illustrated here, the subcutaneous electrode is not shown.

on the electrode array imposes tight area and power constraints. The epidural space of the rat spinal cord is only 3 mm wide and 300 μm deep [26]. Larger implants are not suitable for epidural implantation.

When electronics are placed in the body, heat dissipation must be taken into account during the design phase. According to studies that have been performed on animals, a maximum of 40 mW/cm^2 (or 400 μW/mm^2) chronic heat flux can be tolerated for implantable devices, as this has been shown to lead to less than 1°C temperature increase of the surrounding tissue [27]. Chronic temperature increases larger than this have been shown to have a harmful effect on the health of the tissue ([28], [29], and [30]). The values mentioned above refer to *in vivo* studies in lung and muscle tissue of calves [30], and are also supported by results derived by a computational model of the human head [28]. They are expected to be slightly different for different implantation sites and perfusion rates. The total heat flux tolerated by the tissue will depend on the final size of the integrated circuit and the layout of the whole implant. Keeping in mind the maximum allowable power dissipation per area, our approach was to minimize the power consumption using low power design techniques.

Based on the above, our design choices aimed at achieving a good trade-off between the often conflicting goals of small area and low power consumption without compromising performance and functionality.

B. Stimulus Waveform Requirements and Interleaved Stimulation

The system was designed to deliver rectangular monophasic or biphasic constant current pulses ([31], [32]), up to 1 mA (in this application a resolution step of 10 μA is sufficient [33]), to high impedance loads (there is a 25 V available voltage compliance), at repetition rates of up to 100 pulses per second (pps). This is a single channel system and all the stimulus waveform parameters (amplitude, duration, delay) can be independently

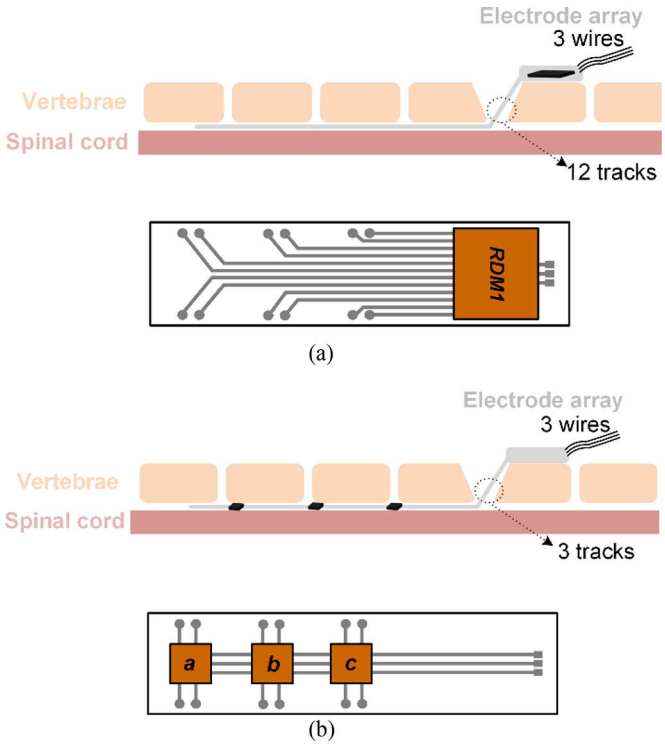

Fig. 2. The proposed layout of the implant in respect to the implantation site (top) and a sketch of the top view of the layout of the active array (bottom) for (a) version RDM1 and (b) version RDM2. In the top drawings, the electrode array is represented by the grey structure entering the spinal canal through the laminectomy. The electrodes are located in the implant's main body, in contact with the spinal cord. In the bottom drawings, sketches of the top views are included to enhance the clarity by better illustrating the differences between the two versions. Grey circles and orange rectangles represent electrodes and ASICs, respectively.

selected for each phase. In the scenario where pulses of different characteristics need to be delivered to different electrodes, as it is often desired in ESCS, this system is capable of interleaved (sequential) stimulation; the time between two successive pulses allows other pulses with independently controlled characteristics to the same or different groups of electrodes. Since all pulses are generated from the same current source the stimulation period is either the same for all patterns, or a multiple of the smallest.

III. System Design

A. System Layout

When implantable electronics are designed the final layout is often dictated by the implantation site and must also comply with the restrictions posed by the implantation procedure. To evaluate the suitability of this implant for chronic implantation we developed two different versions of this ASIC, called RDM1 and RDM2, respectively.

In the first version, RDM1, the whole driver is integrated into one ASIC which controls all 13 electrodes. This is placed at the end of the array outside the spinal canal [Fig. 2(a)], while the epidural part passes through the laminectomy into the epidural space created by the neurosurgeon. This ensures that the ASIC can be securely fixed on the bone in a protected place and can also have a larger total area. In this case, 12 long tracks run along

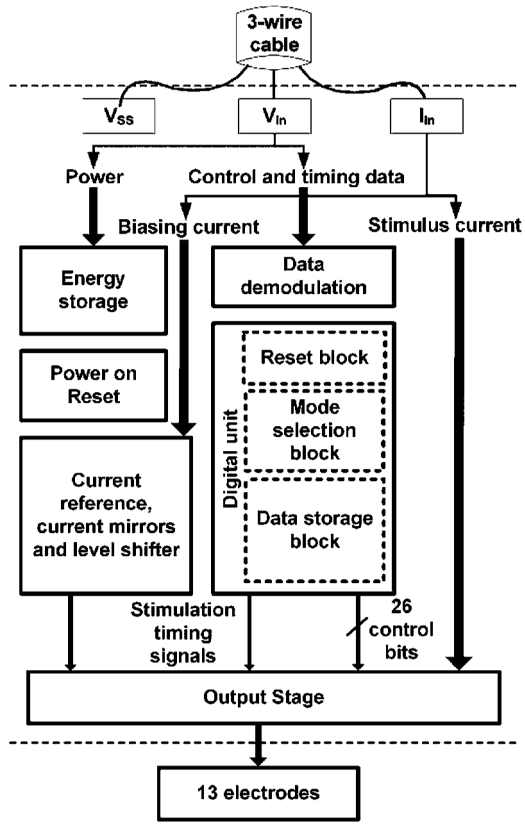

Fig. 3. Functional block diagram of the electrode driving ASIC (RDM1).

the array, but the number of wires needed for communication with the subcutaneous hub is only 3, thus reducing the risk of failure or infection.

Towards a more delicate solution, we have developed a second version, RDM2, where three submodules, RDM2a, RDM2b and RDM2c [ASICs a, b and c, in Figs. 1 and 2(b)], work together as one driver. Three smaller ASICs were designed, each driving 4, 4 and 5 electrodes, respectively. These are placed on the main area of the electrode array, in the epidural space near their respective electrodes [Fig. 2(b)]. This version has many advantages over the first. The number of long tracks that run along the array is reduced from 12 to 3, making the implant narrower. The design of the electrode array becomes more versatile as the width of each interconnecting track can be increased to reduce the chance of failure [7]. In addition, the power dissipation is more uniformly distributed. However, it requires much smaller and thinner ASICs to fit into the 3 mm wide and 300 μm deep rat epidural space, and adds to the complexity of the implantation procedure.

B. ASIC Operation

In both versions of the ASIC discussed above, the operation and circuit design is essentially the same, differing only in the number of electrodes. Therefore, the rest of this section applies to both RDM1 and RDM2.

The block diagram of the electrode driving ASIC is shown in Fig. 3. Two input wires (V_{in} and the negative supply rail V_{SS}, set here to 0 V) are used to deliver the power, control data for the selected electrodes and timing information for the stimulation.

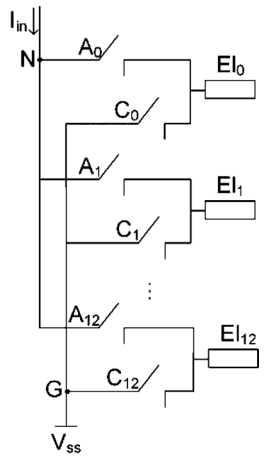

Fig. 4. Output stage topology. A_{0-12} and C_{0-12} indicate the anodic and cathodic switches, respectively and El_{0-12} the electrodes.

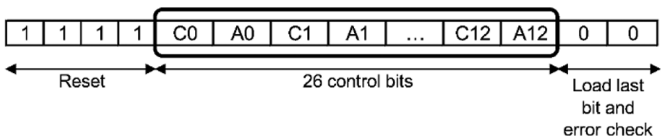

Fig. 5. Structure of control word expected at the input. 4 '1' bits prepare the data demodulation block for the reception of the control data. The next 26 bits indicate the state of the switches and 2 '0' bits provide the clocking information to load last bit and trigger error checks.

The externally generated stimulus current I_{in} is delivered by the third wire.

To achieve arbitrary selection of any of the electrodes on the array, each is connected to two high voltage (HV) switches in the output stage block, one anodic and one cathodic (Fig. 4). Thus, by setting its respective switches on or off, each electrode can be used either as an anode, cathode or not used at all for a specific pattern, allowing the formation of multi-electrode configurations. This topology very conveniently allows the reversing of the direction of the current for the second stimulus phase without using an extra current sink.

The necessary data for the control of these switches are sent to the ASIC as a 32-bit digital word via input V_{in} in the form of a train of pulse width modulated voltage pulses. The form of the expected word at the input is shown in Fig. 5.

Fig. 6 shows waveforms during the system's transient operation. Initially, V_{in} is raised to 5 V to charge an on-chip storage capacitor in the energy storage block. The rest of the system is powered by the charge on this capacitor. The increasing voltage across it (V_{DD}) indicates that the system has been turned on, causing the power-on-reset (PoR) block to reset the logic.

V_{in} is continuously monitored throughout the operation. A negative step to V_{ss} indicates that a bit is being sent. To respect our low power requirement we decided not to implement any clock on this system. Therefore, the data demodulation block and the digital unit operate in an asynchronous manner, only processing data as they arrive at the input. This allows us to externally define the rate at which the data are sent. In this design, rates of up to 0.5 MHz can be used to ensure complete recharging of the capacitor after the reception of each bit.

A monostable in the data demodulation block, triggered by the falling edge of V_{in}, produces a pulse of a predefined width. The inverted output of the monostable is used as an extracted clock (clk). Its falling edge provides some clocking information to manage the operation of the digital unit, while its rising edge is used to sample the input and demodulate the received data.

After the '1111' sequence (allocated for resetting) is detected, 26 control bits are stored serially inside the data storage block. These are followed by two zero bits (dummy bits used to operate the logic) that indicate the end of the control word and trigger error checks. These safety checks ensure that no electrodes have both their switches on simultaneously and that there is at least one anode and one cathode for each stimulation pattern. If an error is detected, all switches are kept off and no stimulation occurs.

After the whole 32-bit word has been sent, the system is ready to start the delivery of the stimulus current. When V_{in} is next pulled 'low', the output stage is updated and the current I_{in} is directed to the electrodes. The absence of a clock means that there is no accurate timing control on this ASIC. Therefore, the timing of the stimulation is externally defined by pairs of zero bits sent at the beginning and end of each stimulus phase. In this way, the accuracy of the pulse duration is not compromised.

After the end of the first phase, during the interphase delay, all the switches are kept off, leaving the electrodes floating [31]. At the onset of the second phase, the state of the stored bits defining the current stimulation pattern is reversed for the delivery of the reverse pulse to the participating electrodes. Electrodes that did not participate in the first phase are kept disconnected from the system the whole time. After the end of the second phase, all electrodes are connected to the reference potential (0 V), so that any remaining charge is passively removed [32]. The system is now ready to receive the new control word for the next pattern asynchronously, whenever this is available at the input.

Throughout this flow, the mode selection block keeps track of the operating mode (data reception and demodulation, first stimulus phase, interphase delay, second stimulus phase) and manages the output stage, by its 2-bit output signal (U_0 and U_1).

IV. Circuit Design

A. Energy Storage Block

In order to deliver both power and data through 2 wires (V_{in} and V_{SS}) the storage capacitor needs to be able to store the necessary charge long enough to power the system while V_{in} is kept low (for a maximum of 1.5 μs, when sending '1' bits). Simulations taking into account the maximum instantaneous and average charges drawn from a 5 V supply during the transient operation of the system suggested that a 271 pF capacitor would be sufficient. The gate capacitance of a 5 V PMOS was used, which occupies a 0.1 mm^2 die area. Higher voltage transistors could not be used due to their limited capacitance per unit area. A Schottky diode connected between V_{in} and the capacitor to prevent reverse current causes a voltage drop of about 0.3 V (smaller than conventional diodes). The simulated maximum voltage across the capacitor is 4.7 V, and during the operation of the system it can be as low as 4.3 V.

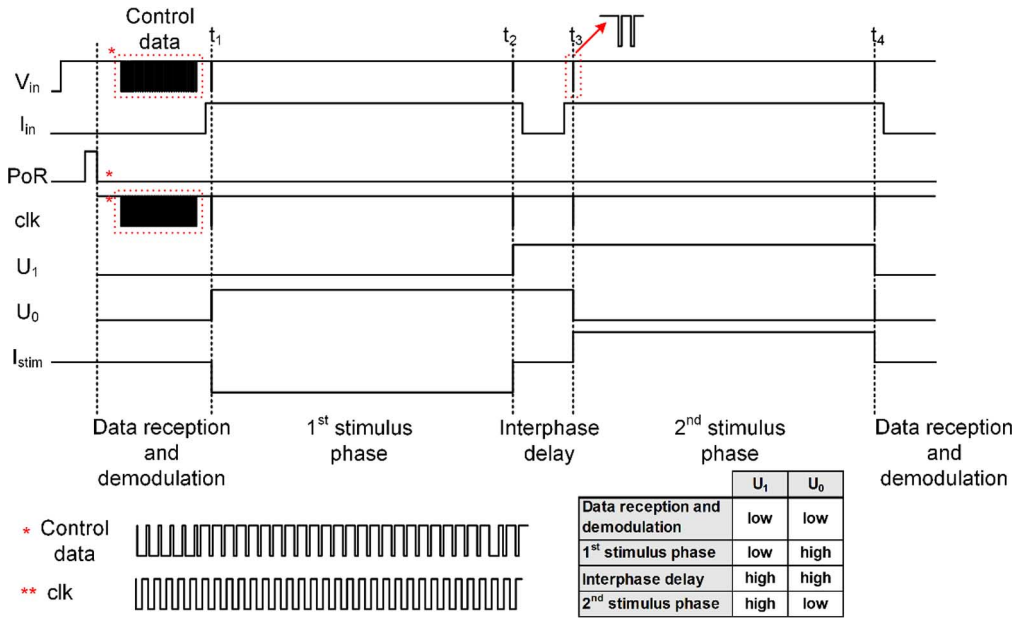

Fig. 6. Signal flow from the time when the system is powered on and for a full biphasic cycle. $\mathrm{I_{in}}$ is switched on and off briefly before and after the delivery of each phase, but the exact timing is not important. Clocking information is only available during data transmission. Signals $\mathrm{U_1}$ and $\mathrm{U_0}$ are produced by the mode selection block, and indicate the current operating mode according to the bottom right table. The control data in this example define $\mathrm{C0} = \text{`1'}$, $\mathrm{A0} = \text{`0'}$, $\mathrm{C12} = \text{`0'}$ and $\mathrm{A12} = \text{`1'}$ and disable electrodes 1–11 (see Fig. 5).

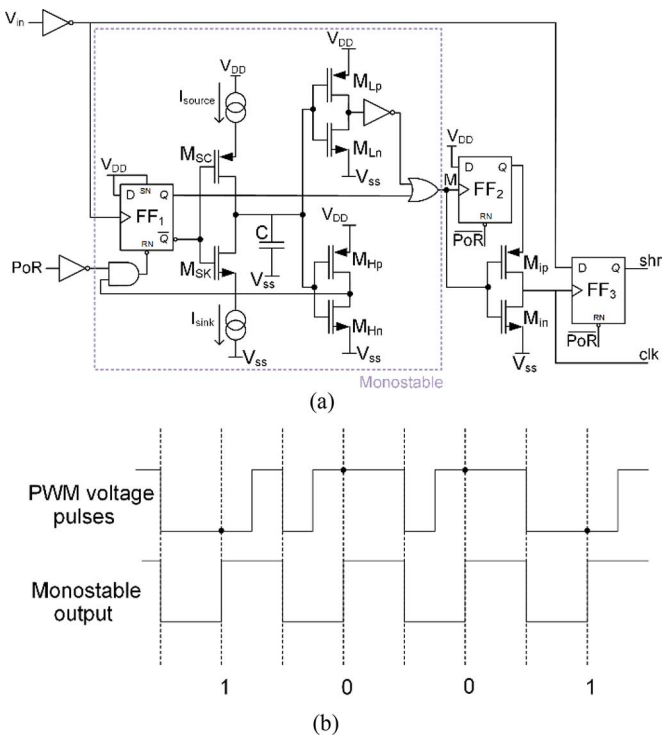

Fig. 7. (a) Circuit schematic of the data demodulation block. (b) Timing diagram of the demodulation scheme.

B. Data Demodulation Block

In the data demodulation block [Fig. 7(a)], the monostable constantly monitors $\mathrm{V_{in}}$. In this monostable topology [34], a current source $(\mathrm{I_{source}})$ and a current sink $(\mathrm{I_{sink}})$ are used to charge and discharge a capacitor (C). They are implemented by current mirrors that copy and scale the current produced by an on-chip current reference. The increase and decrease of the voltage across C causes two analog inverters to toggle their outputs at different switching points, one high ($\mathrm{V_H}$, for $\mathrm{M_{Hp}}$, $\mathrm{M_{Hn}}$) and one low ($\mathrm{V_L}$, for $\mathrm{M_{Hp}}$, $\mathrm{M_{Hn}}$), so defining the duration of the produced pulse. At the end of this pulse, $\mathrm{V_{in}}$ is sampled by flip-flop $\mathrm{FF_3}$, the input data are demodulated and the output of this block (shr) is transferred to the data storage block. The signal clk is used as a clock for the digital unit. The monostable was designed to produce an 800 ns pulse, to distinguish between short (250 ns) and long (1.5 μs) pulses, that indicate a digital '0' or a digital '1', respectively, according to the demodulation scheme shown in Fig. 7(b).

C. Digital Unit

The digital unit was designed in Verilog. It comprises three dynamic logic blocks that complement each other. Fig. 8 shows how substructures in the digital unit communicate with each other. The reset block uses counters to monitor consecutive '1's received at the input and detect the reset sequence. The reset signal it produces is different from the PoR signal, and it only resets the digital unit, not the whole ASIC.

The data storage block is directly connected to the output of the data demodulation block. It includes two 26-bit registers; one serial-input parallel-output register, $\mathrm{Reg_1}$, to store the demodulated data, and one parallel-input parallel-output register, $\mathrm{Reg_2}$, to control the output stage. A counter is used to manage the loading of the demodulated bits into $\mathrm{Reg_1}$. This counter addresses the flip-flops using the Gray code to minimize the number of transitions. The simulated average power consumption of the block was reduced by 33% when Gray code was used as opposed to serial loading.

The data loaded on $\mathrm{Reg_2}$, as well as the time when these will be loaded are managed by the mode selection block. This block

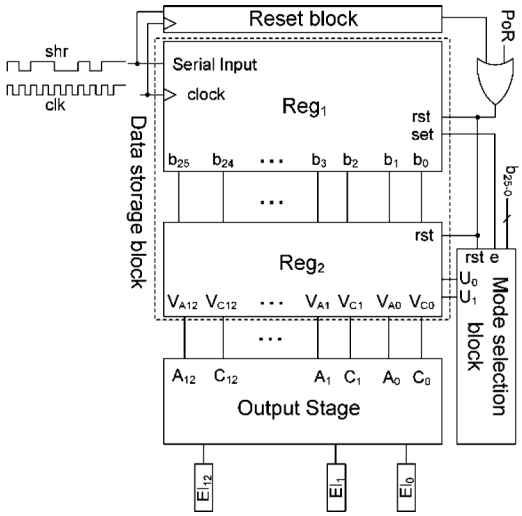

Fig. 8. Connections between the substructures of the digital unit and the output stage.

uses counters to monitor the input pulses, counting 26 clock cycles after the reset sequence. Once all 26 bits have been loaded, the loading stops until the register is reset by the reset block. Some extra logic is also included in this block to set Reg_1 to all zeros (through output e) in case an error is detected in the control word, preventing undesirable stimulation. The combined value of its output bits (U_0 and U_1, Fig. 6), that indicate the operating mode of the system, is used for communication with Reg_2.

D. Output Stage and Current Reference Block

The circuit schematic of the output stage block is shown in Fig. 9. This analog block includes details of the implementation of the switches in Fig. 4, as well as their control circuit. For the cathodic switches, 30 V NDMOS transistors were chosen $(\mathrm{M_{C0\text{-}12}})$. These are controlled by voltages produced by the digital unit $(\mathrm{V_{C0\text{-}12}})$, connected directly at their gate terminal. DMOSs were selected as simulations showed that an increased speed could be achieved with significantly smaller devices, compared to conventional HV transistors. For the respective 30 V PDMOS transistors $(\mathrm{M_{A0\text{-}12}})$ used as anodic switches, a voltage controlled topology would be too complex due to the wide variations of the voltage at node N (in the range of approximately 2.3 V up to 25 V, depending on the load at the output and the stimulus current). For this reason, 5 μA current mirrors acting as current sinks are used to establish the necessary voltage drop across resistors $(\mathrm{R_{b0\text{-}12}})$ to turn the anodic switches on [35]. $\mathrm{R_{b0\text{-}12}}$ were implemented using a high-ohmic non-salicided resistor, each occupying an area of 178 $\mu\mathrm{m}^2$.

A current reference $(\mathrm{M}_1 - \mathrm{M}_8)$ generates the only bias current $\mathrm{I_{ref}}$ (500 nA) on this chip, while a set of current mirrors is used to copy $\mathrm{I_{ref}}$ $(\mathrm{C_{M1\_0-12}})$ and scale it up to 5 μA $(\mathrm{C_{M2\_0-12}})$. Current $\mathrm{I_b}$ is set by an NMOS cascode current mirror implemented using HV devices $(\mathrm{C_{M3\_0-12}})$ to interface the 5 V transistors with the HV line. We chose to scale up the current using $\mathrm{C_{M2}}$, which is made of low voltage PMOS transistors, rather than $\mathrm{C_{M3}}$. This choice requires 10 times more current drawn from the on-chip capacitor, but leads to a considerably smaller area. Voltages $\mathrm{V_{A0\text{-}12}}$ (outputs of the digital unit) define whether the respective anodic switch is on or off, by turning on and off the whole current mirror structure for the specific electrode.

The correct operation of $\mathrm{C_{M3}}$ requires that the voltage at node N is at least 2.3 V. To ensure that, we had to shift the voltage at node C to above 0 V. We used the two diode connected transistors, $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$, to shift it to 2.3 V during stimulation, consuming negligible extra power, but at the expense of a reduced output voltage swing.

V. Subcutaneous Hub

To test this ASIC the 'subcutaneous hub' was implemented as a non-implantable platform having a structure as shown in Fig. 10. This first version of the hub was connected to a USB port, providing both a 5 V power supply and bidirectional data transfer between the host PC and hub. The hub can communicate operational parameters such as supply voltage status back to the host, which will be useful for monitoring the battery voltage after implantation. The host can communicate the stimulation parameters to the MSP430FR5739 microcontroller, which interprets the data and generates the appropriate bit sequence $\mathrm{V_{in}}$, as well as the programmed current.

A programmable voltage is generated by the AD7524, an 8-bit multiplying DAC which is operated in voltage mode. The 2.5 V reference voltage ('Ref' in Fig. 10) is connected to one of the DAC's output terminals and the other output is grounded. The divided voltage of the internal R2R ladder network can then be accessed from a third terminal. This arrangement is preferred in this single-supply setup, as the output does not need to be inverted.

The DAC's output voltage is then converted into a current by an improved Howland current source (Fig. 11). Its operational amplifier has to be supplied by up to 28 V from a unipolar supply and its common-mode input must include the 0 V rail. The high voltage supply is generated by an LMR64010 boost converter, which features output voltages up to 40 V and an efficiency of about 75% with the chosen input and output settings. Since the current drawn is less than 1 mA, the efficiency drops. As a result of the short duty cycle, the dissipated power of the converter would not cause a significant increase in the temperature inside the implant.

Note that the source does not continuously supply a current, but only at times when the ASIC connects the source between the chosen electrodes in either stimulation phase. The opamps of the Howland current source have to recover from saturation as fast as possible after the source has been switched to the selected electrode pair. These criteria are fulfilled by the chosen OPA2140, which features a short overload recovery of 600 ns, and a fast large-signal settling time of 1.6 μs.

VI. Experimental Results

The prototype chips were fabricated in XFAB XP018, a 0.18 μm high-voltage CMOS technology. A microphotograph of the fabricated RDM1 ASIC is shown in Fig. 12.

We kept the area occupied by the core of the ASICs less than 0.36 mm^2 to be compatible with both versions. The total area of each version was adapted to the specific requirements of the integration procedure of the ASIC on the electrode array. Large custom designed ESD pads were used in both

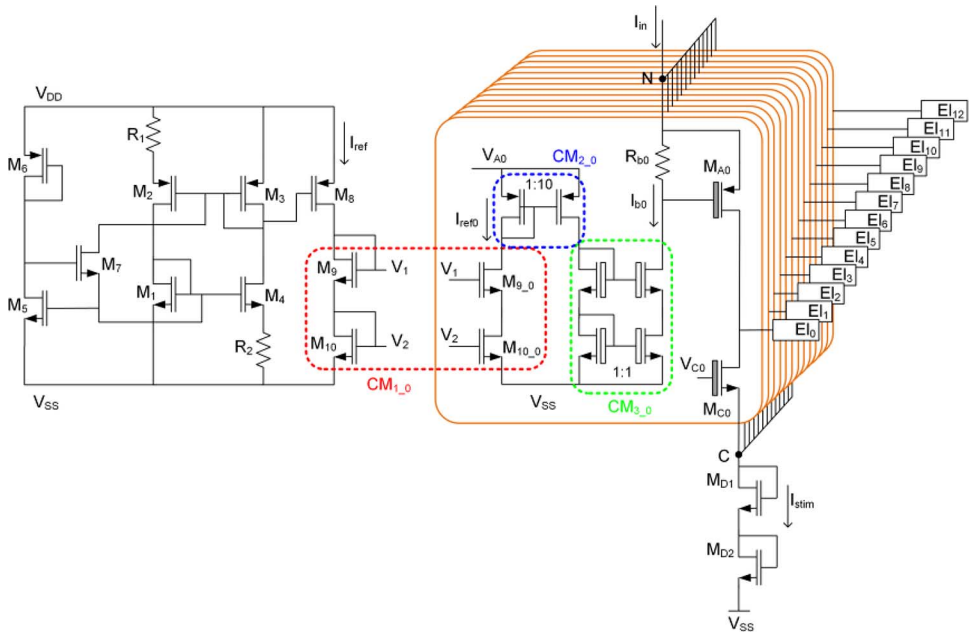

Fig. 9. Circuit details of the output stage block and its control. An on-chip current reference (M_1–M_8) generates the reference current I_{ref} which is then copied and scaled up (CM_1–CM_3) to create the biasing current I_b for each anodic switch. Voltages V_A and V_C are the respective outputs of the digital unit that define the role of the specific electrode. Diode connected transistors M_{D1} and M_{D2} are used as a level shifter. The current at the input is the sum of all the individual biasing currents ($I_{b0\text{-}12}$) plus the total stimulus current I_{stim}.

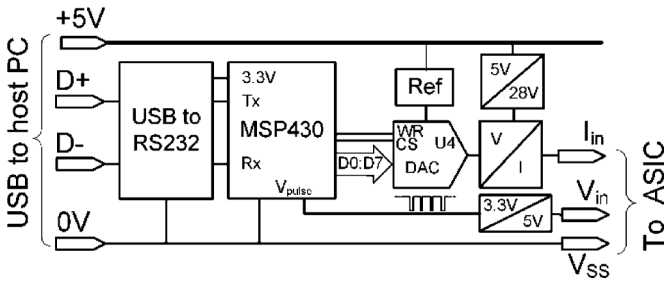

Fig. 10. Block diagram of the hub. A graphical user interface provides an environment for the user to insert the stimulation parameters. These are transferred from the host PC to the hub, through a USB, which, in turn, controls the operation of the ASIC via its 3 outputs.

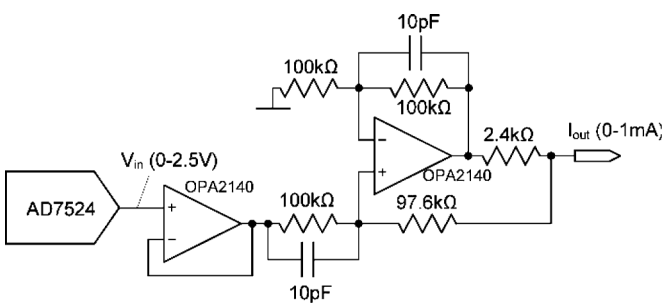

Fig. 11. Improved Howland current source schematic.

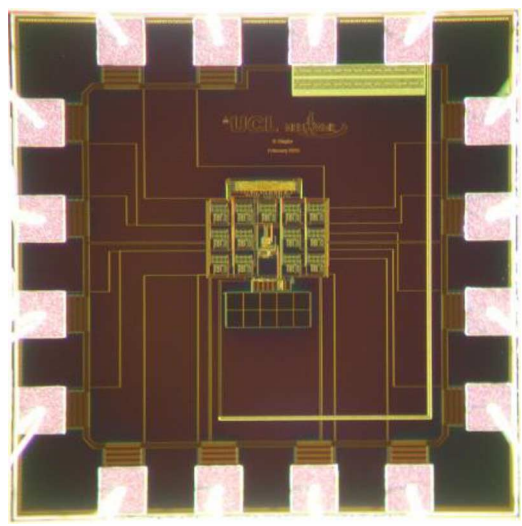

Fig. 12. Microphotograph of RDM1.

cases to facilitate assembly. Thus, RDM1 features a total area of 2.944 mm × 2.944 mm, while each of the submodules of RDM2 is 1.753 mm^2 (see Section VII). Table I shows the silicon area breakdown.

Table II shows the average power dissipated by the system, and eventually converted into unwanted heat dissipation, during different operating modes. In these calculations, we exclude the power used for the stimulation. Only the 500 nA current reference is constantly on, and a number of current mirrors also draw currents of up to 5 μA each from the 5 V supply when on. The data demodulation block, together with the digital unit operate with a very small duty cycle during the delivery of a biphasic stimulus pulse and they mainly consume power when transitions occur. According to our simulations, in a full biphasic stimulation cycle, with two 250 μs long pulses and a 100 μs interphase delay, the mean power consumption of the system is not more than 114 μW in the worst case.

A printed circuit board platform was used for the testing of both versions of the system. Thirty ASICs were tested in total, 15 RDM1 and 15 RDM2, all of which were fully functional.

TABLE I
AREA BREAKDOWN

Subcircuit	Area (μm^2)
Energy storage block	58464
PoR	4828
HV switches (and their control)[a]	12485
Digital unit	44000
Data demodulation block	10863
Current reference	667
Current mirrors and level shifter	5528.5

[a] For each electrode

TABLE II
AVERAGE DISSIPATED POWER

Operating Mode	Average Dissipated Power[a] (µW)	
Stand-by	13.5	
Data reception and demodulation	42.5	
Stimulation	min[b]	61.8
	max[c]	336.8
mean[d] (worst case)	114	

[a]Stimulus current not taken into account, [b]1 anode, [c]12 anodes, [d]Simulated throughout the full biphasic stimulation cycle

A current source (6221, Keithley) was used to accurately produce the input current (I_{in}). An arbitrary waveform generator (TGA12104 100 MHz, TTi), was programmed to produce the selected voltage waveform for the input of the system V_{in} (including the pulse width modulated control data as well as the timing of the stimulation). Transient results were plotted on a mixed-signal oscilloscope (MSO-X 2024A 200 MHz, Agilent Technologies). Both versions of the system were tested with different loads, various current amplitudes and against several stimulation parameters and all chips had a very similar response.

A. Performance for Various Loads/Current Amplitudes

First, to evaluate the ability of the ASIC to accurately drive different loads, purely resistive loads (between 2 kΩ and 25 kΩ) were connected between the output pads.

Fig. 13 shows the current waveform that flows between the cathode and the anode of the system during a biphasic pulse for various current amplitudes (100 μA, 500 μA and 1 mA) when an 18 kΩ load is connected between them. For this test a single pair of electrodes alternately perform as anode and cathode in a full biphasic cycle. The results suggest that the desired current is accurately delivered in both phases. Similar results were observed for different loads as low as 2 kΩ and for all 30 tested chips. Small deviations from the expected current are observed

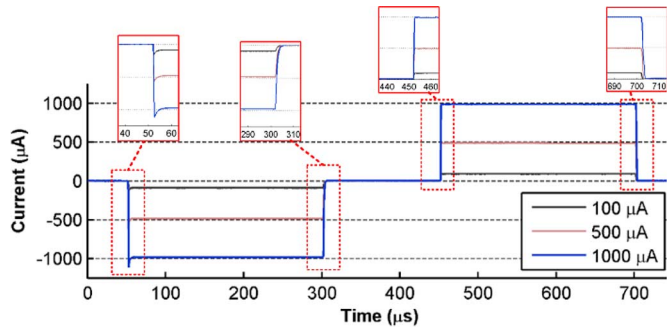

Fig. 13. Recorded current waveforms through a resistive load (18 kΩ) for different injected current amplitudes. The results validate that the correct current amplitude flows through the load each time and that pulses are symmetrical. Similar results were observed for different loads.

in the individual anodic (cathodic) currents in a multi-anode (cathode) stimulus pattern, due to the different impedances of the HV switches among different outputs. For a nominal current of 500 μA, we measured a mean amplitude of 500.28 μA, with a standard deviation of 4.69 μA. These values were derived from 195 measurements among same-chip, as well as different chips.

A maximum rising time of 1.4 μs was measured when high currents were delivered to high loads, which compares relatively well to the simulated value of 0.9 μs. Measured falling times were typically 10 times lower.

Magnified views of the rising and falling edges of the pulses are illustrated in Fig. 13. The imperfect rectangular shape of the pulses, caused by the stray capacitances when switching the current at the beginning and end of each stimulus phase, results in a negligible charge error between the two phases. In fact, the maximum remaining charge across any pair of electrodes after a full biphasic cycle was measured to be -0.223 pC (or $<0.0001\%$) (average of 64 cycles, the sign here indicates that slightly more charge is injected during the first phase of the pulse). This is when the maximum current (1 mA) is delivered to the load, for 250 μs, where the nominal injected charge in each phase is 250 nC.

B. Interleaved Stimulation

Fig. 14 illustrates the transient operation of the system during interleaved stimulation. Control data and timing information for four different stimulus patterns are successively sent at the input V_{in}, each at a 50 pps. For these patterns, different current amplitudes, pulse widths and interphase delays were set and the correct operation was validated for all settings. All outputs were connected via 18 kΩ resistors to a common node. The recorded current waveforms through outputs 0, 1 and 2 are plotted. For pattern a, 2 outputs (1 and 2) formed the cathode group and 4 others (0, 3, 5 and 7) formed the anode group. Thus, the amplitude of the current that flows through each of the anode resistors is half that which flows through the cathode resistors. This is in contrast to pattern b, where a 3-resistor cathode and a 3-resistor anode are used. In pattern c, the control word that was sent to the ASIC did not define any electrode as a cathode, thus, the error prevention mechanism of the digital unit detects this and no stimulation occurs for this pattern. In pattern d, output 0 does

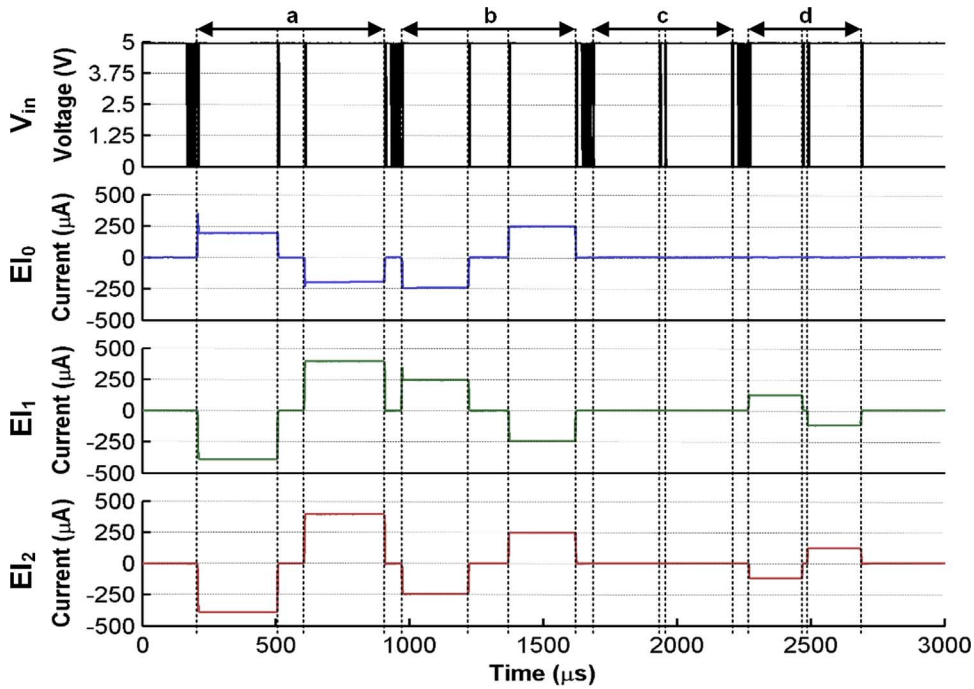

Fig. 14. Transient operation of the system during interleaved stimulation; four patterns (a), (b), (c) and (d) are successively sent, indicated by time intervals in the figure. Recorded waveforms of the voltage applied at the input of the system, and the current through El_0, El_1, and El_2, are illustrated. The specific settings used for each pattern are explained in Table III.

TABLE III
SETTINGS FOR THE DIFFERENT PATTERNS USED IN FIG. 14

Pattern	Cathodes	Anodes	Pulse duration (μs)	Interphase delay (μs)	Current amplitude (μA)				Load[b] (kΩ)		
					Input[a]		Expected cathodic	Expected anodic	Each electrode	Total cathodic	Total anodic
					1st phase	2nd phase					
(a)	El_1, El_2	El_0, El_3, El_5, El_7	300	100	820	810	400	200	18	9	4.5
(b)	El_0, El_2, El_4	El_1, El_3, El_5	250	150	765	765	250	250	18	6	6
(c)	no cathode[c]	El_0, El_2, El_4	250	20	780	780	0	0	18	non applic.[c]	non applic.[c]
(d)	El_2, El_4, El_5, El_9, El_{10}, El_{12}	El_1, El_3, El_6, El_7, El_8,El_{11}	200	20	780	780	125	125	18	3	3

[a]The input current amplitude is calculated from the desired amplitude of the cathodic pulse plus the current needed to bias the anodic switches. The values in this table are calculated so that balanced biphasic pulses are delivered though the selected group of electrodes.
[b]18 kΩ resistors were connected to each output pad instead of electrodes for this test. The expected total anodic and cathodic load seen at the output varies for each pattern according to the number of anodes and cathodes, respectively.
[c]This pattern is to illustrate that no stimulation occurs when an error is detected in the control bits sequence.

not participate in the stimulation, therefore there is zero current flowing through it. More details of the settings used for all patterns are shown in Table III. The terms 'expected cathodic' and 'expected anodic' current correspond to the stimulus current amplitude that is expected to flow out or into each individual cathode and anode, respectively. In this context, the input current is the current required at the input of the ASIC to ensure the desired stimulus amplitude at the output. This is the sum of the total expected cathodic current amplitude and the current needed to bias the anodic switches, in each phase.

C. Other Results

To evaluate the operation of the sub-blocks of this system, some test structures were added to a test chip fabricated together with RDM1 and RDM2. From this chip, we were able to measure the voltage across the storage capacitor used to power up

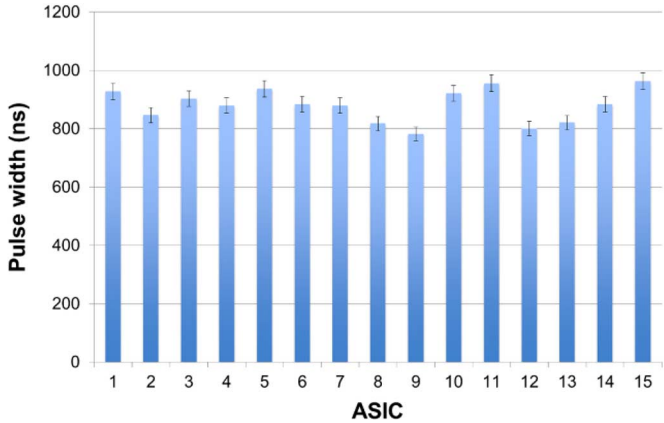

Fig. 15. Average measured monostable pulse width from each of the 15 tested chips. The error bars indicate the minimum and maximum pulse widths measured from each chip.

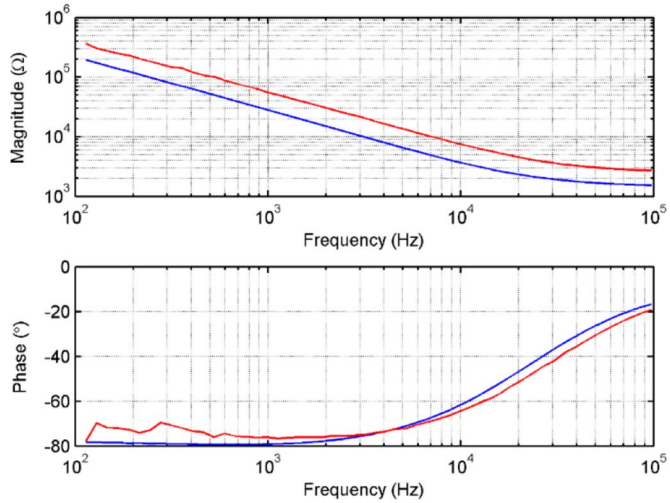

Fig. 16. Typical impedance magnitude and phase traces recorded when the electrodes on the array were used in monopolar (blue) and bipolar (red) configurations.

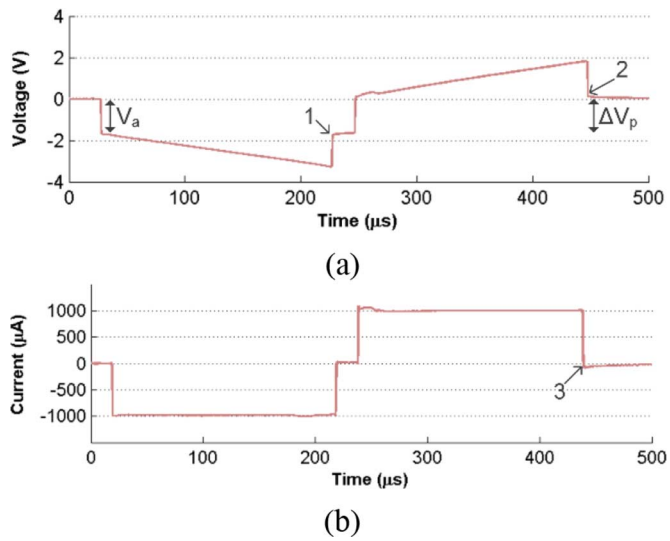

Fig. 17. Recorded voltage (a) and current (b) waveform between the anode and the cathode of the system when 1 mA is delivered to the load. For this test, one electrode on the array was used as the cathode in a monopolar configuration.

the ASICs. According to our measurements, this voltage varies between 4.17 V and 4.62 V, which agrees well with the simulated results. We were also able to measure the width of the pulse produced by the monostable block. Results from 15 chips, graphically illustrated in Fig. 15, show that the average duration for all chips is 880.5 ns (as opposed to the targeted 800 ns), with a standard deviation of 56.5 ns. This difference is of no importance in this implementation, as the monostable is used to distinguish between 250 ns and 1.5 μs pulses.

D. Testing With Electrode Arrays

To verify the correct operation of the system with a realistic load, the chips were tested with an electrode array in normal (or physiological) saline (0.9% or 9 g/1000 ml solution of Na^+Cl^-). Normal saline has a conductivity of $\sim$15 mS/cm which, in the frequency range of 0–10 kHz, matches the conductivity of the human cerebrospinal fluid [36]. The electrode array that was used for this test was a custom made epidural 12-electrode array specifically developed for this application by the Institut für Mikrotechnik Mainz (IMM), Mainz, Germany. It is made from polyimide and thin film gold tracks. Stainless steel wires connect the electrode array to the interface in our setup.

Impedance measurements using an impedance analyzer (6500B, Wayne Kerr Electronics) were taken prior to the experiment to verify that all electrodes were functional. The array was immersed in unbuffered saline in a beaker together with a return electrode for monopolar tests. The return electrode was the 1 cm exposed end of an insulated stainless steel wire. Typical recorded impedance traces for monopolar and bipolar configurations are plotted in Fig. 16. Measured standard deviations from all electrodes in 2 arrays (at 1 kHz) were in the order of 0.8 kΩ and 0.65 kΩ for the monopolar and the bipolar case, respectively.

Fig. 17 demonstrates the capability of this ASIC to drive a realistic load by showing the recorded voltage [Fig. 17(a)] and the respective current [Fig. 17(b)] waveform between the cathode and the anode of the system when the maximum current (1 mA) is delivered to the load. In this test we used only one of the electrodes on the 12-electrode array as the cathode in a monopolar configuration, to test the system with a higher impedance load. When more electrodes are used, they appear in parallel, reducing the total load impedance. For the waveform of Fig. 17(b), a 1 kΩ resistor was connected in series with the electrodes and the voltage across it was recorded and translated into current. In point 3 all electrodes are shorted to the reference potential and any small charge mismatch between the two phases is passively discharged (see discussion). The almost linear change of the recorded voltage during the two stimulus phases in Fig. 17(a) suggests a very strong capacitive nature for these electrodes, supported by the close to $-90°$ phase in the low frequency part of the impedance spectroscopy phase trace in Fig. 16. A 1.7 kΩ resistive contribution of the electrolyte is anticipated, as suggested by the high frequency part of the magnitude trace in Fig. 16. This would correspond to a 1.7 V voltage drop at the onset of the stimulus pulse, which agrees well with the plotted values for V_a in Fig. 17(a). The voltage difference

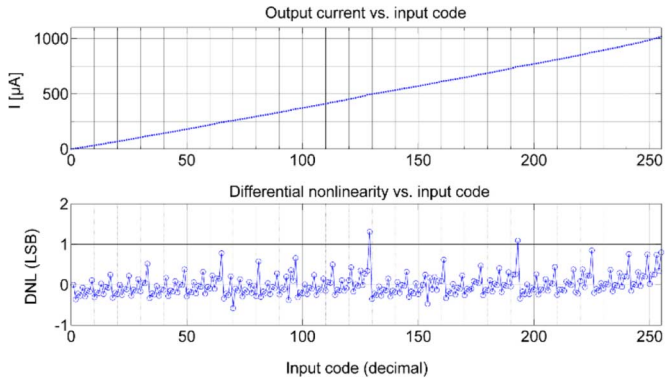

Fig. 18. Performance of the programmable V/I conversion chain in the hub.

between point 1 and 2, in Fig. 17(a), corresponds to the maximum polarization voltage across the electrode-electrolyte interface. When voltage transients are recorded using a 3-point setup (where a large-area return electrode is used and potentials are referenced to a non-current-carrying reference electrode) [37], both potentials at points 1 and 2 are expected to be between the established minimum and maximum potentials (for the specific material) beyond which electrolysis is likely to occur. This potential difference is the water window and for gold is suggested to be around 1.8 V [38]. Direct comparison between the extreme potentials would not be valid, as there was no reference electrode in our setup. We could nevertheless, relate the potential difference ΔV_p of Fig. 17(a), which is approximately 1.7 V, to the reported water window, and assume that this waveform would not translate to unsafe stimulation. In the discussion above we need to consider the contribution of the return electrode in our setup; although this was larger in area compared to the working electrode, it appears in series and contributes to the recorded trace. Fig. 17, together with Fig. 16, suggest that electrodes with even higher impedance magnitudes could be accommodated by this system, as only a total voltage headroom of 5.8 V is practically required in this case (out of the available 25 V compliance) to deliver the maximum current to the load.

E. Testing With the Subcutaneous Hub

The performance of the whole programmable V/I (voltage-to-current) conversion chain in the hub is shown in Fig. 18, where the DC output currents were measured using a 10 kΩ load and a precision ammeter (6485 picoammeter, Keithley) for all possible input codes. The response is linear, the two missing codes for differential nonlinearity (DNL) larger than 1 can be tolerated for this application. This first, non-implantable, version of the hub was successfully used to deliver the information to the ASIC supplied through a graphical user interface (GUI).

VII. Discussion and Conclusion

The decision to keep the generation of the stimulus current external to this ASIC was to satisfy our low power and area requirements and has two advantages. Any extra circuitry needed for the implementation of the programmable current source and any additional voltage required by the current generator to satisfy variations in loads is within the hub where the area and power specifications are not so tight. In a future implementation of the hub, feedback could be introduced to inform the system about the expected load impedance and generate only the necessary drive voltage, avoiding unnecessary power consumption.

The layout of this ASIC was developed to be compatible with two different electrode array designs. Since manual bonding is necessary, large custom designed pads (up to 300 μm $\times$ 300 μm) were incorporated. The off-chip tracks will be insulated by polydimethyl siloxane (PDMS), which must adhere to the passivation layer on the chip to provide sufficient protection [39]. We felt that a gap of 300 μm is reasonable (but this has to be tested). These dimensions finally dictated the size of the ASICs. The core occupies only 4% of the total die area for RDM1 and less than 20% in each version of RDM2. In future versions, the size of the ASICs could be scaled down, by using an automatic bonder that would allow for smaller pads.

When the number of anodes differs from the number of cathodes, the required total bias current I_b (Fig. 9) for each phase is provided by adjusting the injection current. Differences in the individual currents $I_{b0\text{-}12}$ from the expected 5 μA value though, could mean that a different amount of charge could be injected between the two phases. Unfortunately, due to the layout of the chips, we did not have access to these currents, therefore it has not been possible to measure their amplitudes. Nevertheless, our Monte Carlo post-layout simulations (taking into account both process and mismatch variations with parameters provided by the foundry) have shown that the mean value of I_b is 4.95 μA with a standard deviation of 0.41 μA [25]. In addition, simulated results when V_{DD} is varied from 4 V to 5 V (the measured V_{DD} agrees well with these limits) showed that the nominal amplitude of I_b is in the range of 4.85 μA–4.95 μA. Based on the above, we do not expect I_b to be less than 4 μA in any case. That suggests a maximum error of 1 μA for each anode. In the extreme case, when 12 electrodes are used as anodes, this could add up to a maximum of 12 μA, all of which need to be injected through the single cathode. In this case, as far as charge balancing across the cathode is concerned, there will be a difference of 11 μA between the first and second phase of the pulse flowing through the cathode. For pulses of 250 μs, that would lead to a 2.75 nC residual charge at the end of each cycle. The practical current amplitude values for this 12-electrode extreme scenario fall in the range of 400 μA–1 mA. This translates to a 100–250 nC total charge in each phase, corresponding to a 2.75%–1.1% mismatch error, which is within the limits of other designs, when only active discharge is employed ([40], [41]). Even if smaller currents were to be used though, the present system is still able to passively further minimize most of the remaining charge by shorting all electrodes to the reference potential after each cycle [see Fig. 17(b), point 3]. The degree to which this shorting is effective, apart from the initial imbalance, depends on the electrode discharge time constant and the time available for discharge, which is ample in this case since this is a low frequency application (maximum 100 pps).

Regarding the driving capabilities of these chips, despite the results of Fig. 17, the situation could be very different in a chronic state. Connective tissue is expected to grow around the electrode array after implantation and the conductivity around the electrodes is will decrease [42]. *In vivo* testing is needed to

TABLE IV
COMPARISON TABLE

		[9]	[10]	[11]	[12][3]	[13]	[This work]
Technology		3-µm	2-µm	1.5-µm	0.8-µm	0.6-µm	0.18-µm
Number of inputs		5	8	not specified	not specified	5	3
Number of electrodes		16	8	8	4	12	13
Number of channels[1]		16	1	1	1	4	1
Electrodes configuration		any	monopolar	monopolar	monopolar and bipolar	tripolar	any
Pulse duration		any, externally defined	4 - 512 µs, 4 µs resolution	up to 1 ms	any, externally defined	2 - 1069 µs, exponential	any, externally defined
Current amplitude		± 254 µA, 2 µA resolution	up to ±126 µA, 2 µA resolution	up to 120µA or 600 µA, 6-bit resolution	1.6 -167.2 µA	1, 4, or 8 mA	up to 1 mA, externally defined (+ up to 60 µA for biasing)
Power supply		±5 V	±3 V	±6.5 V	3.3 V	18 V	5 V
Voltage compliance		10 V	6 V	13 V	13.6 V	18 V	adaptable, up to 25 V
Expected load		not specified (tested with 6.8 kΩ)	not specified (tested with 10 kΩ)	up to 10 kΩ	up to 100 kΩ	up to 2 kΩ	up to 25 kΩ
Die area	**core**	11 mm²	2.9 mm²	approx[4]. 2.5 - 3 mm²	appox[4]. 5.3 mm²	6.4 mm²	< 0.36 mm²
	total		4.8 mm²	4.84 mm²	8.38 mm²	27.3 mm²	[5]8.67 mm² / 1.753 mm²
Power consumption	**stand-by**	80 µW				30 µW	13.5 µW
	average[2]	not specified	450 µW	500 µW	51.37 mW	30.11 mW	114 µW

[1]Independent current sources, [2]Stimulus current not included in calculations, [3]Output stage chip, [4]Not specified in the publication, estimate from the microphotograph, [5]Values refer to RDM1 and each module of RDM2, respectively.

verify that stimulation can be induced in the chronic state. Nevertheless, we expect these load variations to be accommodated as this ASIC allows for a maximum of 25 V output voltage compliance, to account for the increased load impedance.

To conclude, Table IV summarizes some of the most important characteristics of this work in comparison to previously reported designs. The ASIC presented here features the smallest core size and power consumption and the lowest number of driving input wires.

ACKNOWLEDGMENT

The authors are especially grateful to Dr. A. Vanhoestenberghe for her contributions to understanding all the relative anatomical aspects and finalizing the active implant layout, which in turn led to finalizing the structure of this system. They would also like to thank the Institut für Mikrotechnik Mainz, Germany, for kindly providing the passive electrode arrays used for the electrical testing. Last, but not least, acknowledgments are due to all people participating in the NEUWalk project, particularly P. Munsienko and N. Wenger for their guidance; the scientific discussions contributed significantly to this work.

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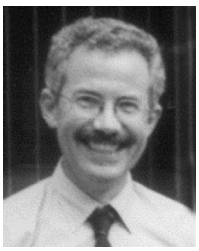

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