Advances in Scalable Implantable Systems for Neurostimulation Using Networked ASICs

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***Abstract*—Neurostimulation is a known method for restoring lost functions to neurologically impaired patients. This paper describes recent advances in scalable implantable stimulation systems using networked application specific integrated circuits (ASICs). It discusses how they can meet the ever-growing demand for high-density neural interfacing and long-term reliability. A detailed design example of an implantable (inductively linked) scalable stimulation system for restoring lower limb functions in paraplegics after spinal cord injury is presented. It comprises a central hub implanted at the costal margin and multiple *Active Books* which provide the interface for stimulating nerve roots in the cauda equina. A 16-channel stimulation system using four *Active Books* is demonstrated. Each *Active Book* has an embedded ASIC, which is responsible for initiating stimulus current to the electrodes. It also ensures device safety by monitoring temperature, humidity, and peak electrode voltage during stimulation. The implant hub was implemented using a microcontroller-based circuit. The ASIC in the *Active Book* was fabricated using XFAB's 0.6-µm high-voltage CMOS process. The stimulation system does not require an accurate reference clock in the implant. Measured results are provided.**

***Index Terms*—*Active Books*, humidity measurement, implantable stimulator, low power, networked ASICs, neurostimulation, reliability, scalable stimulation system, temperature measurement.**

I. Introduction

DAMAGE or degradation to the central and peripheral nervous systems due to injury or disease results in loss of neural function in various parts of the body. Neuroprostheses may assist in partial restoration of function and mobility using neurostimulation. It involves passing pulses of electrical current into muscle tissue or nerve branches, which cause activation or excitation of targeted muscles or neural tissues.

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The first neurostimulation systems were reported in the early sixties [1]. Since then they have developed into fully implantable devices employing wireless telemetry for the transmission of power and control signals [2], [3]. The most commercially successful neuroprosthesis to date, the cochlear implant, processes sound at different frequencies into amplitude modulated electrical pulses which stimulate multiple sites along the cochlea. The method has successfully restored hearing for thousands of patients [4]. Using a similar principle, limited sight can be restored by translating visual signals into multi-site electrical stimulation on the retina [5], [6]. Similarly, balance can be restored by converting head motion into frequency modulated current pulses to the vestibular organs [7], [8], [9], and locomotor functions, such as standing and walking, can be restored by coordinated stimulation on the spinal cord [10], [11], [12].

Stimulators with extremely high channel count have been reported, such as 232 channels for visual prosthesis [13], 64 channels for deep brain stimulation [14], 22 channels for cochlear stimulation [15] and 16 channels for spinal cord stimulation [16]. It is expected that an even higher channel count will be needed to achieve finer neuron-device interaction. There are two different approaches to address this: i) integrate as many stimulation channels as possible on a single ASIC, and ii) use a scalable system with networked ASICs where each ASIC addresses a fraction of the stimulating channels. While there is no immediate limitation in silicon technology on how many channels can be included on an ASIC, the number of stimulating channels per ASIC is usually limited by practical issues, such as the reliability of multiple interconnections to and from the stimulator ASIC [17]. For some neural applications, groups of stimulation sites may not be physically close. In such cases, cable management and implantation procedure is easier if stimulation sites in close proximity are grouped together and a stimulator ASIC is assigned to manage only the nearby sites.

The rest of the paper is organized as follows. Section II discusses current challenges as stimulator implants become smaller and feature many more channels. It provides a literature review on recent advances in scalable implantable stimulation systems for neurostimulation using networked ASICs. A detailed design example is presented in Sections III–V. The system architecture is described in Section III. Section IV discusses the circuit design of the key functional blocks, including the telemetry and ASIC. Measured results

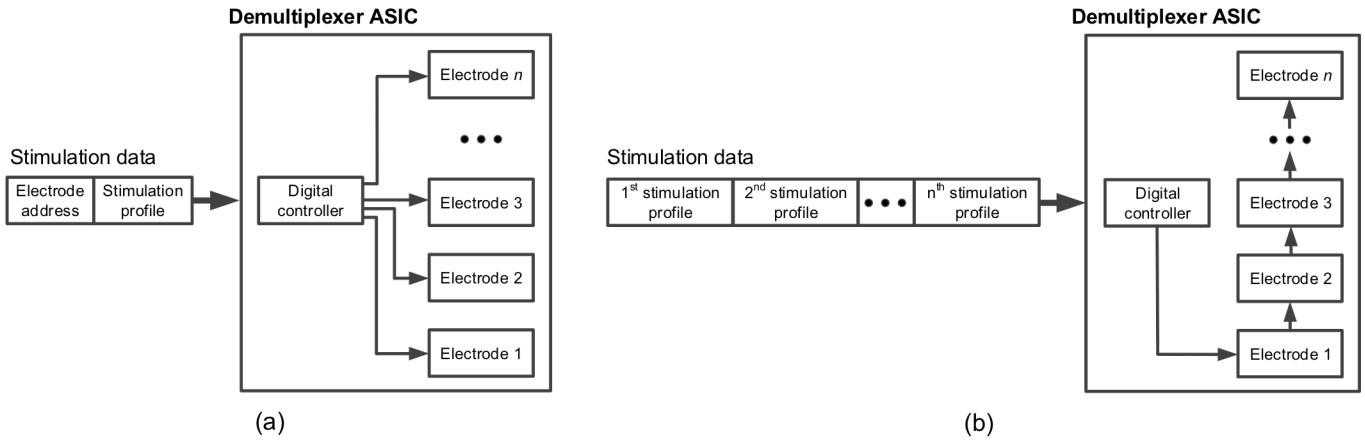

Fig. 1. Different methods of addressing electrodes: (a) parallel configuration; (b) series shift configuration.

are presented in Section V, followed by concluding remarks in Section VI.

II. Scalable Stimulation Systems Using Networked ASICs: Challenges and State-of-the-Art

A. Leads Count

As the number of stimulation channels increases the number of interconnect wires between a stimulator and an electrode array increases. The width of the interconnect cable containing the wires then becomes impractical to be safely implanted. For example, it is expected that a spinal cord stimulator on nerve rootlets in the spine would require 96 channels for more selective and direct muscle activation: 6 (i.e., L2 to S2 segments of the spine) × 8 (rootlets per nerve root) × 2 (sides) [18]. This would require 192 and 288 leads for dipole and tripole stimulators, respectively. High cable count is not only a significant challenge for surgeons to implant the cables safely [19], but also causes a significant percentage of implant failures [20], [21].

To overcome this problem a demultiplexer ASIC can be added to the electrode array itself [22]. Such a configuration is known as "active electrode" because it moves the demultiplexer from the stimulator (start of the interconnect cable) to the electrode array (end of the interconnect cable). There are two different forms of demultiplexing, direct demultiplexing and regenerative demultiplexing, depending on how the demultiplexer ASIC handles the input. Giagka *et al.* [11] presented a demultiplexer ASIC for driving epidural electrodes. One of the inputs to the ASIC is the stimulus current; other inputs include power and data to define which stimulation site the stimulus current accesses. The demultiplexing takes place directly from the input current. Although easy to implement, it is not possible in direct demultiplexing to provide different currents for different stimulation sites in the same demultiplexer ASIC. An alternative approach is to send only the data and power to the demultiplexer which works out the specification needed for stimulation from the input data, generates the necessary stimulus, and steers it to the chosen channel. It is at the demultiplexer ASIC that the stimulus current is regenerated. Since the data and power can be modulated together, the theoretical minimum number of input leads for this approach is two. In practice it is common to use dedicated power and data wires (which may include a separate clock wire, a demultiplexer specific enable wire and a wire for stimulation commands). The total number of input wires for a demultiplexer then varies between two and nine [9], [10], [11], [23], [24], [25], [26], [27], [28] which can fit into a helical cable and be implanted safely.

Demultiplexing compromises the flexibility of simultaneous stimulation. To the authors' best knowledge there is no reported neural stimulation application that requires all stimulation sites to be activated at the same time. Hence, most stimulators should be able to provide a certain level of demultiplexing.

B. Addressing Stimulating Electrodes

In a multi-channel stimulator, the stimulus currents flow through the selected electrodes, which are typically individually addressed. Two different configurations exist to address electrodes, parallel and serial shift, as shown in Fig. 1. In the parallel configuration, each electrode has an address. By specifying the target electrode's address, the controller can arbitrarily stimulate any site and thus any stimulation sequence is possible. The disadvantage of this method is the increase in the size of the data packet due to the extra overhead needed for address bits. It requires a higher data rate at the telemetry. If an implant system contains multiple demultiplexers, each ASIC needs to differentiate itself from others by a unique ID. This not only increases data rate, but also complicates the electronics design as each ASIC needs to be programmed differently to set up the unique address ID.

The serial shift configuration has the stimulus data for all electrodes arranged in a predetermined fashion. Because the electrodes are sequentially addressed, each electrode address need not be in the data packet and the data rate is lower than in the parallel configuration. The implant system can drive more electrodes by appending the extra channels to existing channels. The disadvantage of the serial shift configuration is that flexible arbitrary stimulation is limited because the sequence in which different electrodes are addressed is fixed.

TABLE I
COMPARISON OF SCALABLE IMPLANTABLE NEUROSTIMULATION SYSTEMS USING NETWORKED ASICS

Reference	Application	Network Topology[ξ]	Stimulation DeMUX Type	ASICs per System	Channels per System	Inputs to Each ASIC	Methods for Addressing ASICs and Channels
[23], [24]	Cortical stimulation	Daisy chain	Regenerative	32	2048 (64 per ASIC)	2	ASICs cannot be individually addressed. By channel ID
[11]	Spinal cord stimulation	Daisy chain	Direct	3	12 (4 per ASIC)	3	By ASIC ID and channel ID
[25]	Retinal stimulation	Daisy chain	Regenerative	9	9 (1 per ASIC)	4	By ASIC ID and dedicated channel inputs
[9]	Vestibular stimulation	Star-shape	Regenerative	3	18 (6 per ASIC)	5	By dedicated ASIC inputs and channel ID
[10] and This work	Spinal cord stimulation	Star-shape	Regenerative	4	16 (4 per ASIC)	5	By dedicated ASIC inputs and sequential channel addressing
[28]	Cortical recording	Daisy chain	N/A	2	64 (32 per ASIC)	6	By ASIC ID and channel ID
[26]	Spinal cord stimulation	Star-shape for addressing. Daisy chain for stimulus current	Direct	9 + 1	27 (3-6 per ASIC)	8	By dedicated multiplexer inputs and channel ID
[27]	Functional electrical stimulation	Daisy chain	Regenerative	16	512 (32 per ASIC)	9	By sequential ASIC addressing and channel ID

[ξ] In the network topology, the daisy chain is a wiring scheme in which multiple ASICs are connected together in sequence or in a ring. All ASICs share the same input in a daisy chain. In a star-shape configuration, the input to individual ASICs from a central device has some wires common to all ASICs and some ASIC-specific wires.

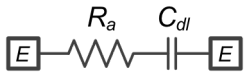

Fig. 2. Simple model of electrode impedance.

In the design example stimulation application in this paper (restoration of motor functions of lower limbs) the stimulation rate is less than 20 Hz and the longest stimulation phase for a stimulation site is only 1 ms. The serial shift configuration should, therefore, be sufficient and the extra time available between stimulations can be used for completing non-stimulation tasks, such as programming the stimulator ASICs.

Table I summarizes the performance of recent scalable stimulation systems, comparing their system architecture, demultiplexing type, number of channels, number of input connections required, and addressing methods.

C. Low Power Operation

In an implantable stimulator power is supplied by an implanted battery or a wireless link. In both cases it is important that the power consumption of the stimulator is kept low (it also reduces the possible heating of the implanted device). The power consumption of an active electrode is

$$P_{\mathrm{AE}} = V_{\mathrm{supply}}(I_{\mathrm{stim}} + I_{\mathrm{other}}) \qquad (1)$$

where V_{supply} is the supply voltage to the stimulator ASIC, I_{stim} is the stimulus current amplitude and I_{other} is any other current taken from V_{supply}. I_{stim} is mainly dictated by the physiological response of the neural tissue. I_{other} includes the current necessary for bias circuits, monitoring circuits and signal processing circuits. It tends to be very small compared with

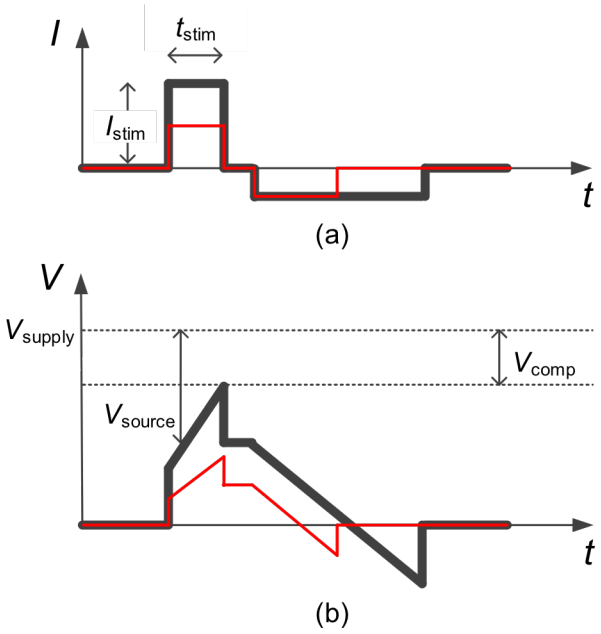

Fig. 3. Electrical neural stimulation waveforms: (a) a typical biphasic stimulus current; (b) a typical inter-electrode voltage. The black curve indicates the stimulus current and electrode voltage when the stimulus current is high while the red curve is when the stimulus current is low.

I_{stim} and optimizing I_{other} has only a small impact on P_{AE}. It is more effective to save power by minimizing V_{supply}.

Fig. 2 shows the lumped circuit model of the electrode-tissue impedance. The supply voltage for a stimulator ASIC is

$$V_{\mathrm{supply}} = I_{\mathrm{stim}}R_a + \frac{I_{\mathrm{stim}}t_{\mathrm{stim}}}{C_{dl}} + V_{\mathrm{source}} \qquad (2)$$

where t_{stim} is the duration of the stimulus current, V_{source} is the

TABLE II
COMPARISON OF STIMULATOR ASICS FEATURING DYNAMIC VOLTAGE SUPPLY

Reference	Stimulus Current	High Voltage Generation	Number of High Voltage Levels	Control Method	Frequency of Adjustment
[5]	4 – 992 µA	Shunt regulator	Limited (not specified)	By monitoring the gate voltage of the cascode transistor in the current generator circuit	Adjusted once in a stimulation cycle
[30]	2 – 504 µA	Switched-capacitor dc-dc converter	4	By monitoring the gate voltage of the cascode transistor in the current generator circuit	Adjusted continuously during the stimulation
[31]	Constant 40 µA	Charge pump	Continuous	By monitoring the exact stimulus current	Adjusted continuously during the stimulation
[33]	20 – 1000 µA	Zero-voltage switching	Continuous	By monitoring the voltage compliance of the current generator	Adjusted continuously during the stimulation
[32]	0 – 450 µA	Inductive dc-dc converter	Continuous	By monitoring the electrode voltage and the exact stimulus current	Adjusted continuously during the stimulation
[34]	80 – 2480 µA	Adaptive rectifier	8	By monitoring the maximum electrode voltage	Adjusted once in a stimulation cycle
This work	1 – 8 mA	Inductive dc-dc converter	8	By monitoring the maximum electrode voltage	Adjusted once in a stimulation cycle (on demand)

voltage drop across the current generator, R_a and C_{dl} are the access resistance and double-layer capacitance of the electrode impedance respectively. The minimum voltage for V_{source} is known as the compliance voltage, V_{comp}, which maintains the high output resistance of the current generator. During the early part of the stimulation (i.e., t_{stim}), C_{dl} begins charging. The electrode voltage is small, resulting in unnecessarily high power wastage at the current generator. As the stimulation progresses, the electrode voltage increases and more power is absorbed in the electrode. Therefore, for a constant supply voltage, the power efficiency is lower at the start of the stimulation and higher towards the end of stimulation. To achieve high power efficiency, for current-mode stimulation, it is desirable to regulate V_{source} so it remains at V_{comp} during the entire stimulation phase (i.e., the supply voltage adapts to the electrode voltage). A more radical approach is to remove V_{source} completely, changing the current-mode stimulator to voltage-mode or charge-mode [29]. While instantaneous adjustment of the supply voltage during the stimulation is possible it usually requires a complex monitoring circuit (for checking the bias voltage in a current generator circuit [5], [30], the instantaneous stimulus current [31], [32], the voltage compliance of a current generator circuit [33] or the electrode voltage [32], [34], and applying closed-loop feedback to adjust the supply voltage), which itself consumes power. Such systems with dynamic voltage supplies are useful for accommodating electrode impedance variation after implantation and adapting to different stimulus currents. Fig. 3 shows that for a given t_{stim}, a small stimulus current (red curve in the figure) requires a smaller supply voltage than a large stimulus current (black curve in the figure). An alternative approach used in the design example (Sections III-V) adjusts the supply voltage monitored at the end of the stimulation pulse to be just above the peak electrode voltage. It consumes only a fraction of the power required for continuous electrode monitoring. Table II lists different stimulator ASICs that employ dynamic supply voltages.

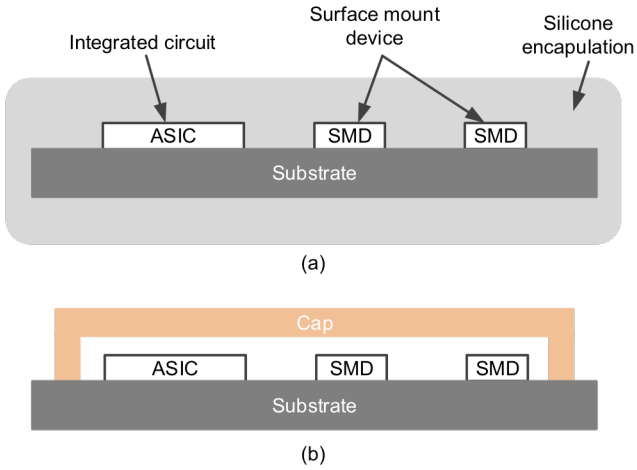

Fig. 4. Protection methods against water ingress: (a) silicone encapsulation; (b) hermeticic micropackage.

D. *Reliability of Small Implants*

As the size of implants reduces engineering challenges arise, requiring additional tests for monitoring the integrity of the ASIC.

1) Heat Dissipation: Conventional implanted devices, such as pacemakers, are relatively large. The electronic circuits are usually enclosed in a metal casing. Nowadays, it is common practice to use silicon microchip technology to integrate as much implant electronics as possible. The final size of the ASIC ranges from a couple of mm^2 to tens of mm^2. The power dissipation density from the surface of the ASIC becomes higher as implanted devices become smaller. Animal studies have shown that a maximum of 40 mW/cm^2 chronic heat flux can be tolerated for implantable devices, as this has been shown to lead to less than 1 ^oC temperature increase of the surrounding tissue [35]. Chronic temperature increases larger than this can harm the tissue [36], [37], [38]. A temperature sensor on the same ASIC as the stimulator circuits can help to

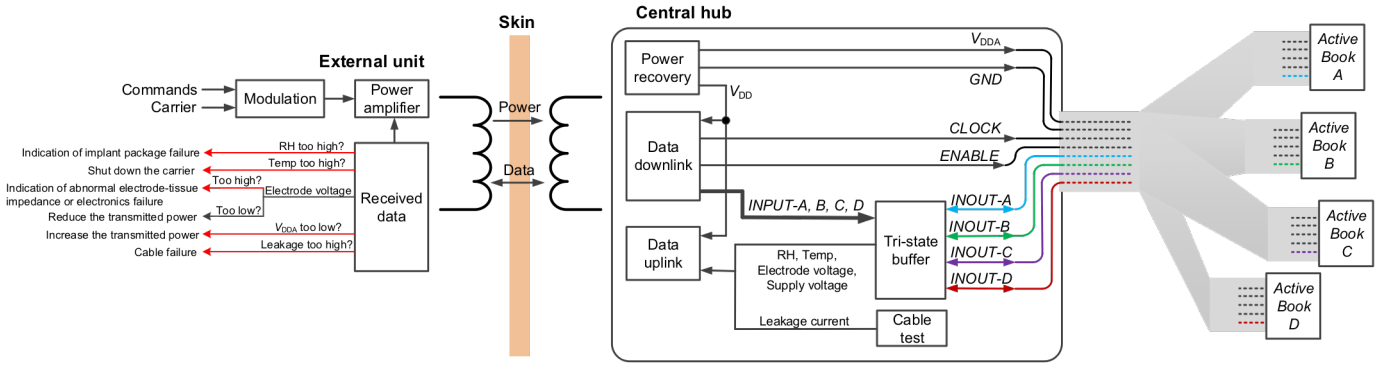

Fig. 5. Stimulation system using *Active Books*.

monitor the implant temperature for safety purposes.

2) Hermeticity of Implant Package: Implantable devices are surrounded by body fluid which is a corrosive environment and electronic circuits need to be protected by either a hermetic package or encapsulation, as shown in Fig. 4. Encapsulation protects the electronics with a conformal layer such as silicone rubber. Although the method is low cost and can be very reliable by careful design, there is no reported data on its effectiveness in protecting silicon microchips. Hermetic packaging is a much more popular method [39]. By maintaining them in a cavity [between the cap and substrate, see Fig. 4(b)] it isolates the electronic components from the body fluids. The hermeticity of a package is commonly evaluated by a helium leak test. Although effective in testing the package of large implants (internal volume > 1 cm^3), it suffers from limited sensitivity when testing micrometer-volume packages, which is currently the case for chip-scale implants [40]. While it may still be possible to produce sealed cavities that remain dry for decades inside the body, its hermeticity cannot be verified using conventional gas tracer methods. The introduction of humidity sensors inside micropackages makes it possible to continuously monitor the internal relative humidity. If the recorded humidity inside the package is higher than the predefined critical value, it indicates failure of the implant package.

III. Design Example – System Design

This design example is targeting stimulation of the lumbo-sacral nerve roots in the human cauda equina.. The goal is to develop an implant for restoring lower-body function to patients with paraplegia after severe spinal cord injury; for example, to enable exercising such as cycling and rowing, to control the bladder and to improve bowel evacuation. Tripolar electrode books are used to stimulate nerve roots/rootlets in the cauda equina (each root comprises fibres from several rootlets that emerge from the spinal cord). The leg muscles are innervated from levels L2 to S2, and as discussed in Section II-A, a distributed stimulating system of up to 96 channels is required. The design example employs *Active Books* [10], [18]. Each *Active Book* has an embedded ASIC. It provides stimulation pulses to the (book) electrodes and measures temperature, humidity and peak electrode voltage, which are used for safety monitoring. As a proof of concept, a 16-channel stimulation system using four *Active Books* is discussed. The number of supported channels can be increased with minimal change at the central hub, by adding more *Active Books*.

TABLE III
CORRESPONDING VOLTAGES DURING THE CABLE TEST

Step	V_{DDA}	*GND*	*CLOCK*	*ENABLE*	*INPUT-A*
1	18 V	0	0	0	0
2	0	0	5 V	0	0
3	0	0	0	5 V	0
4	0	0	0	0	5 V

TABLE IV
RELATION BETWEEN PEAK ELECTRODE VOLTAGE AND UPDATED V_{DDA}

Condition (range of peak electrode voltage)	**Updated V_{DDA}**
Eld > 17.25 V	0 V
17.25 V > *Eld* > 15.75 V	18 V
15.75 V > *Eld* > 14.25 V	16.5 V
14.25 V > *Eld* > 12.75 V	15 V
12.75 V > *Eld* > 11.25 V	13.5 V
11.25 V > *Eld* > 9.75 V	12 V
9.75 V > *Eld* > 8.25 V	10.5 V
8.25 V > *Eld* > 6.75 V	9 V
6.75 V > *Eld*	7.5 V

Fig. 5 shows the block diagram of the stimulation system in which power is supplied to the implant via an inductive link. The implant part comprises a central hub and four *Active Books*, each with an identical ASIC intimately connected. At the external unit, different commands can be deployed which either initiate desirable stimulation functions or instruct the integrated sensors to measure critical conditions at the *Active Book*. The command information is modulated on to a 10 MHz carrier, which drives a class-D power amplifier. The supply voltage for the class-D amplifier is adjustable according to the feedback information from the *supply-voltage sensor* at the ASIC.

At the central hub, the power recovery unit delivers two dc supply voltages, a low voltage V_{DD} for driving the electronics at the central hub and a high voltage V_{DDA} for driving the four ASICs. The amplitude of V_{DDA} is managed by the central hub based on the feedback information from the *peak-electrode-voltage sensor* in the ASIC. The data downlink demodulates

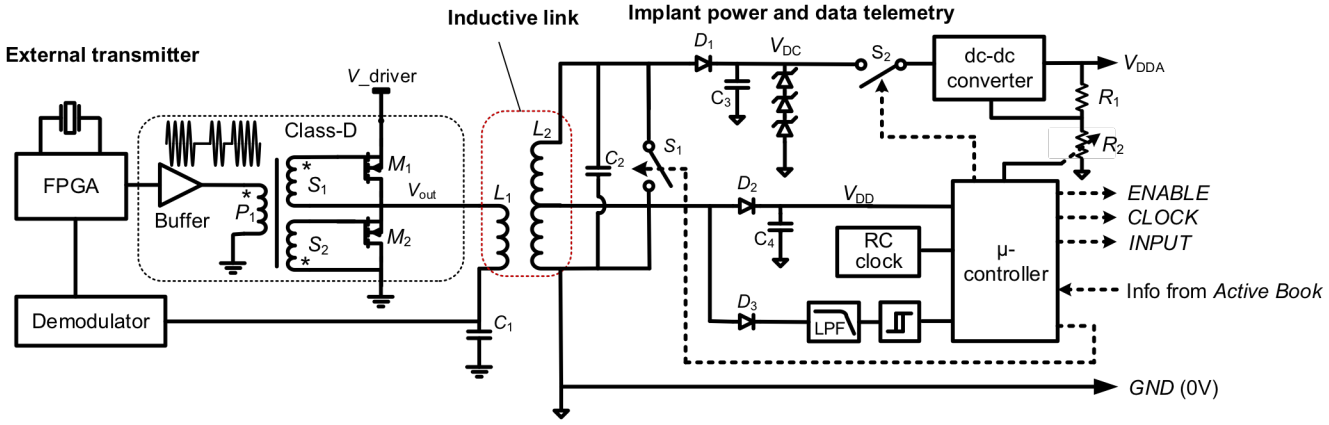

Fig. 6. The implant power and data telemetry.

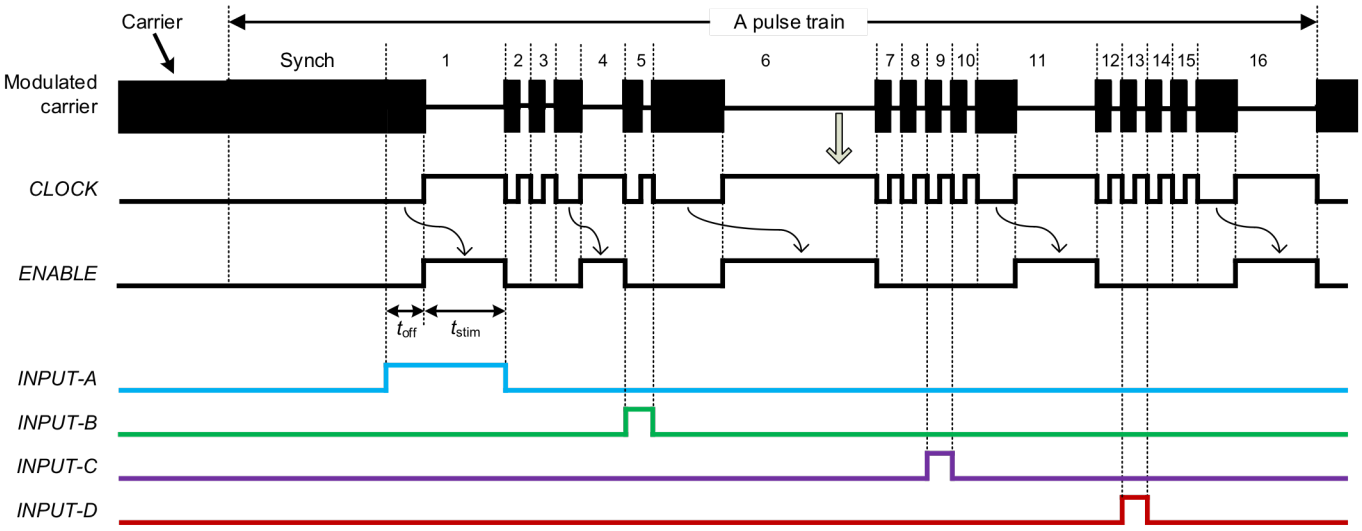

Fig. 7. Demodulation of *CLK*, *ENABLE*, and *INPUT-A*, *INPUT-B*, *INPUT-C* and *INPUT-D* from the modulated carrier over one pulse train.

the command information from the carrier and recovers one *CLOCK*, one *ENABLE* and *n INPUT* signals, where *n* depends on the number of *Active Books* driven by the central hub. Each ASIC is driven by a 5-wire cable (V_{DDA}, *GND*, *CLOCK*, *ENABLE* and *INPUT*). Except for the *INPUT* which is book specific, the remaining four signals are common to the other *Active Books*.

For forward and continuous operation of the ASIC, the proposed stimulation system must pass several tests as detailed in the following subsections.

A. Cable Test

Before any valid signals are sent to the ASIC, the central hub tests the leakage current of the cable of each *Active Book*. Table III shows the procedure for testing the cable of *Active Book* A. The signals V_{DDA}, *CLOCK*, *ENABLE*, and *INPUT-A* are turned high one at a time and the dc current between any of the two wires is measured. The same procedure can be repeated for testing cables of other *Active Books*. During the cable test, the ASIC is held in the quiescent mode, consuming very small current (nanoamperes). A high measured dc current indicates failure(s) at the cable (such as insulation failure) or at the ASIC (such as introducing a low-impedance path between wires). All cables need to pass the test before any one of the *Active Books* connected can be used.

B. ASIC Status Test

In addition to taking information from the central hub, the ASIC sends operating status information for monitoring purposes to the central hub. The *INPUT-X* wire is bidirectional (see *INOUT-X* in Fig. 5). Information to the hub includes the temperature of the ASIC, the relative humidity inside the ASIC's hermetic micropackage, the peak electrode voltage of a stimulating electrode, and the current V_{DDA} voltage, all measured by the sensors on the ASIC. The sensed information triggers appropriate actions at either the central hub unit or the external unit.

If the surface temperature of the ASIC in a given *Active Book* is higher than 41 ^{o}C, it will be shut down immediately and cannot be reactivated for thirty minutes. To shut down the ASIC, all five wires in the cable are switched off (turned to 0 V). After that, as long as the *INPUT* wire remains low, the ASIC is kept in its quiescent mode, consuming negligible current, independent of the signals at V_{DDA}, *GND*, *CLOCK* and *ENABLE*. A constant low at the *INPUT* wire after V_{DDA} has been turned on will isolate the ASIC in question, having no

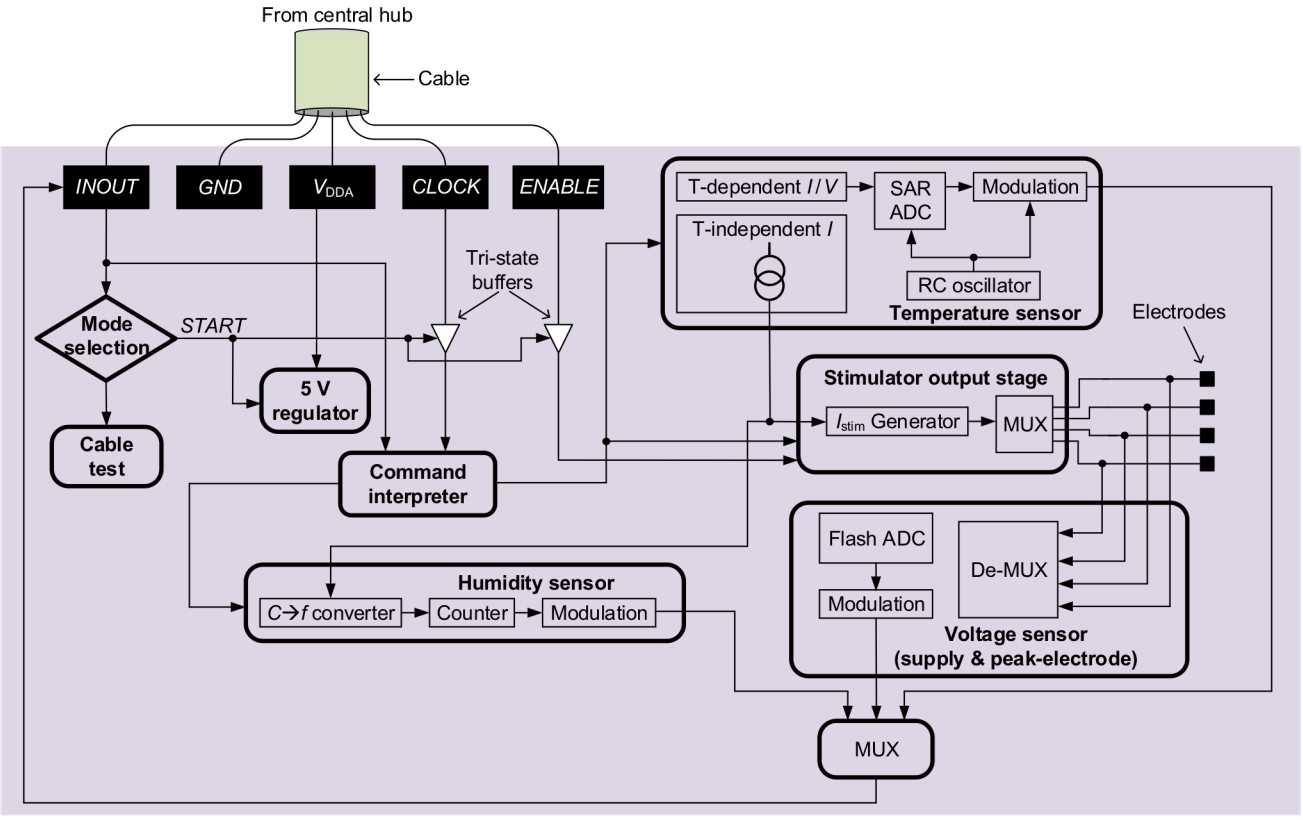

Fig. 8. Functional block diagram of the ASIC for *Active Books*.

further impact on heat dissipation.

If the relative humidity of the ASIC micropackage inside an *Active Book* is close to the predefined critical value (defined as the humidity beyond which the corrosion rate is unacceptable, significantly reducing the reliability of the device) the sensor information will be transmitted to the external unit, alerting the user/manufacturer to the failed or soon-to-fail micropackage.

Once the central hub receives the information on the peak electrode voltage of a stimulating anode, it reissues a new supply voltage should the peak electrode voltage be significantly different from the current V_{DDA}. Table IV shows the updated V_{DDA} for the electrode voltage (*Eld*) ranges. A lower supply voltage helps to save power, which would otherwise be wasted across the current generator. As a safety feature, if the peak electrode voltage is more than 17.25 V, it will be considered as dangerous as it is too close to the maximum possible V_{DDA}, i.e., 18 V. Possible causes include prolonged dc current which saturates the electrode to a near-the-supply voltage. The ASIC will subsequently be shut down, avoiding further damage to the electrode-tissue interface.

After implantation, there may be misalignment between the primary and secondary coils and a change of distance between the two coils, causing V_{DDA} variation due to change in coupling of the inductive link. The current V_{DDA} can be sensed by the *supply-voltage sensor* on the ASIC. The step sizes are the same as the *peak-electrode-voltage sensor*. The information is sent to the external unit, and the supply voltage for the power amplifier is adjusted accordingly, hence more or less power can be delivered to the central hub to generate an optimum V_{DDA}.

IV. Design Example - Circuit Design

A. Telemetry

Fig. 6 shows the implementation of the inductive link for sending the data and power transcutaneously from the external unit to the central hub. Components L_1, C_1 and L_2, C_2 are tuned to 10 MHz. Fig. 7 shows the transmitted signal over the telemetry using on-off keying (OOK) modulation. When no data is sent (i.e., sending all '0s'), the carrier signal remains continuous, charging up capacitors C_3 and C_4. When a '1' needs to be sent, the carrier stops for the duration of the '1'. The advantage of OOK is that its modulator and demodulator are relatively easy to implement compared with other shift keying methods, such as frequency shift keying (FSK) and binary phase shift keying (BPSK). The transmission of power is continuous as long as the carrier is on. The transfer of data has little impact on the overall transmitted power if the data rate is low. Two dc voltages, V_{DC} and V_{DD} are recovered at the full-length and mid-point of the secondary coil after rectification. V_{DC} is protected by three series 2.4 V Zener diodes (NXP, BZV55-B2V4) as a shunt regulator. V_{DD} is a low voltage used for driving the microcontroller and other peripheral circuits in the central hub. V_{DC} connects to a dc-dc converter (LT1615 by Linear Technology), which provides the high voltage supply, V_{DDA}, to the ASIC. V_{DDA} is defined by

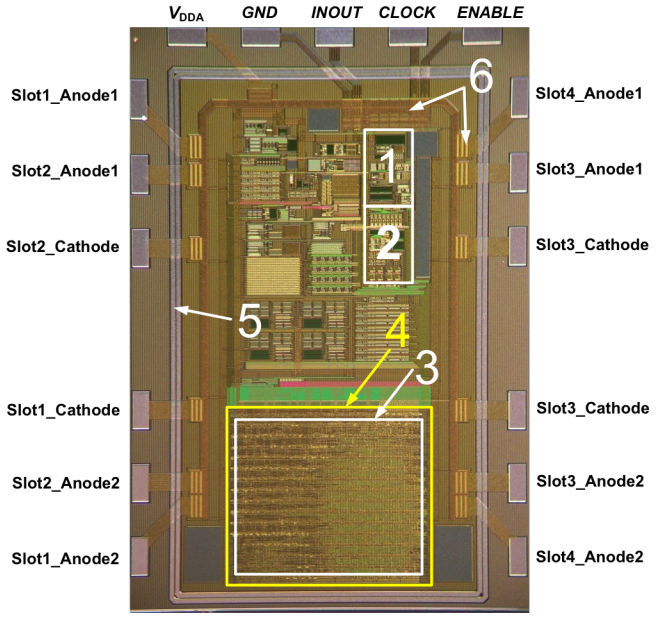

Fig. 9. Die photo of the ASIC. The marked areas show; 1: temperature sensor; 2: voltage sensor; 3: capacitive humidity sensor; 4: digital circuits, 5: seal ring for micropackaging, and 6: ESD for IOs.

$$V_{\mathrm{DDA}} = 1.23\left(\frac{R_1}{R_2}+1\right). \quad (3)$$

The amplitude of V_{DDA} is set by the microcontroller by choosing a suitable resistor ratio R_1/R_2.

To demodulate the data from the carrier, the microcontroller first checks whether the synchronization word matches the expectation (101101110111101). If not, the data will not be utilized. Each digit in the synchronization word lasts for one cycle (i.e., 1 µs) and can be sampled by a simple detector circuit whose frequency does not need to be accurate. If the synchronization word matches, the microcontroller recovers *INOUT*, *CLOCK* and *ENABLE* for driving the ASICs in the *Active Books*. *CLOCK* is recovered by passing the *TX* signal through an envelope detector (LP filter) and then inverted. The shortest interval between pulses (i.e., the off phase on the *CLOCK* line) is 10 µs, which is more than twice that of the longest continuous '1s' or '0s' in the synchronization word. The *ENABLE* signal is recovered by monitoring the off phase of the pulses on the *CLOCK* line. If the off phase is longer than 30 µs, the following on phase becomes *ENABLE* pulses. The generation of the *INOUT* series signals is straight forward as they turn high at the first, fifth, ninth and thirteenth pulse of the *CLOCK* line, respectively.

A significant benefit of the proposed communication protocol is that it does not need an accurate reference clock for sampling the data stream as all the timing information is built into the data signals. At the ASIC, all events are triggered by the rising or falling edge of the data wires. Hence, there is no need for a phase locked loop (PLL) circuit or a crystal to provide an accurate sampling clock. The duration of the stimulus pulse for each channel is defined by the corresponding pulse on the *ENABLE* line.

TABLE IV
ASIC FEATURES AND MEASURED PERFORMANCE SUMMARY

Parameter	Value
Technology	0.6 μm HV CMOS
Supply voltage	18 V
Die size	6.3 × 4.3 mm^2
IO pads	2 × power, 3 × data, 12 × electrodes
Channels	4 tripole
Stimulation - Stimulus current amplitude - Anode current ratio adjustment - Stimulus pulse duration	 1 mA, 4 mA or 8 mA ±20% in steps of 2% 2 µs to 1.07 ms
Temperature sensor resolution	0.12 °C
Humidity sensor resolution	~1%RH
Voltage sensor - Detectable range - Resolution	 0 – 18 V 9 steps

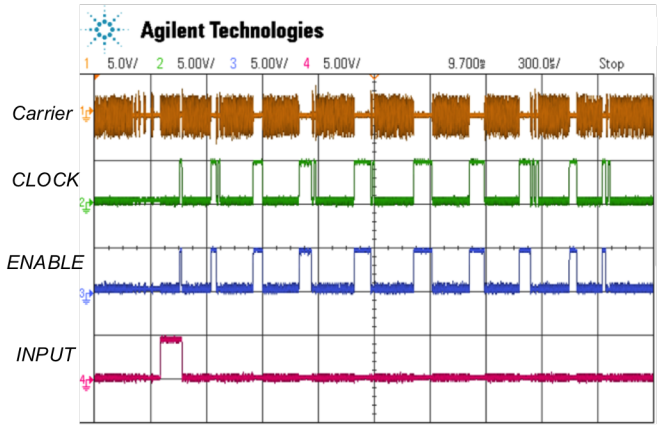

Fig. 10. Demodulation of *CLOCK*, *ENABLE* and *INPUT* signals from the RF carrier.

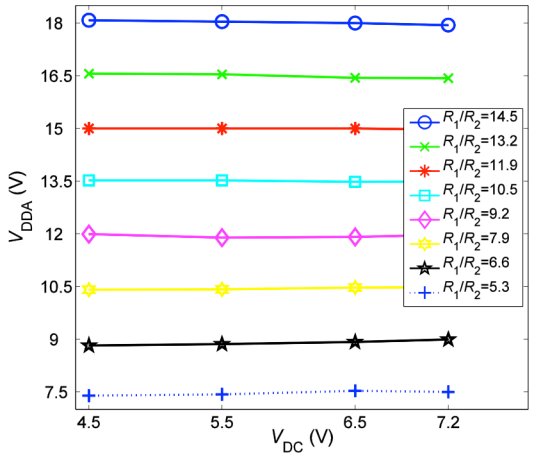

Fig. 11. V_{DDA} vs. V_{DC} for the dc-dc converter at different settings.

B. *ASIC Functionality*

Fig. 8 shows the block diagram of the ASIC for the *Active Books*. It works in the quiescent mode during the cable test and can be woken up by sending a pulse on the *INOUT* line while V_{DDA} is high. The ASIC drives four tripoles. A tripolar electrode configuration contains three electrodes: a central

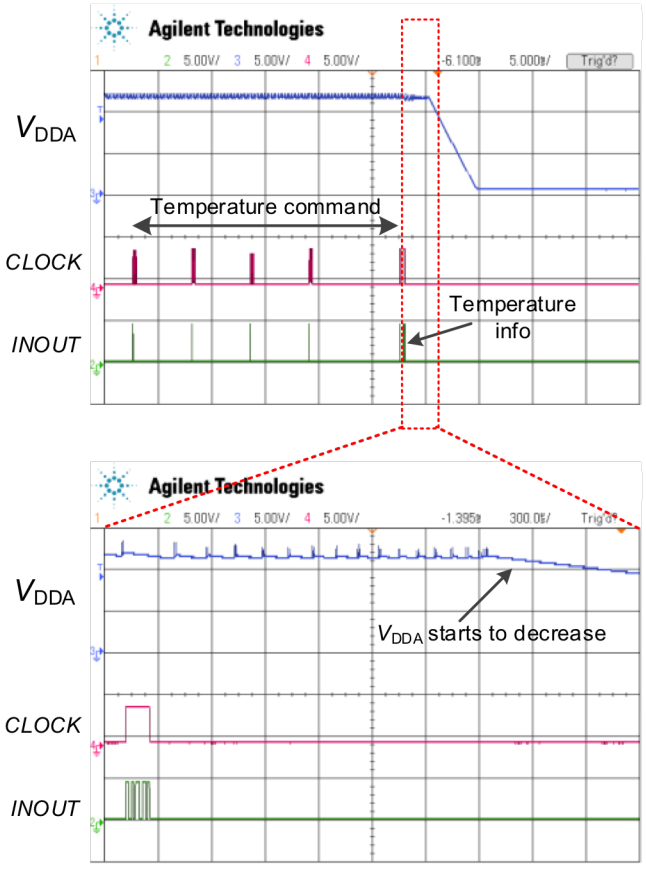

Fig. 12. Response of V_{DDA} to temperature information.

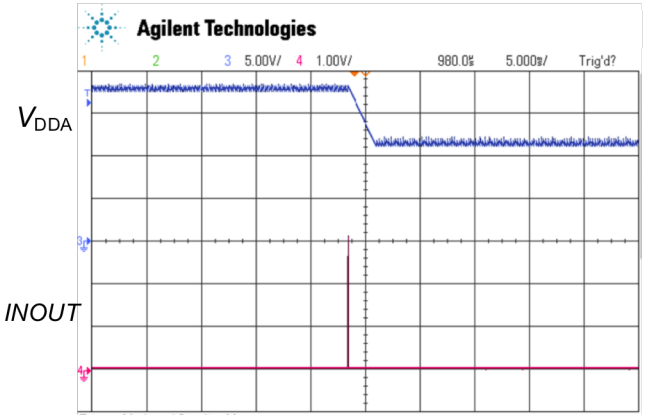

Fig. 13. Response of V_{DDA} to a peak electrode voltage between 9.75 V and 11.25 V.

cathode flanked by two outer anodes. The stimulus current which splits between two anodes can be adjusted to 0 mA, 1 mA, 4 mA and 8 mA. The current difference between two anodes can be programmed to ±20% in steps of 2%. There are four sensors on the ASIC, which can measure temperature, relative humidity, peak electrode voltage of any anode in a Book, and the current supply voltage. The ASIC is a development of the design described in [10] with additional functionality and sensors to enable measurement of temperature, humidity and peak electrode voltage for monitoring purposes and safety.

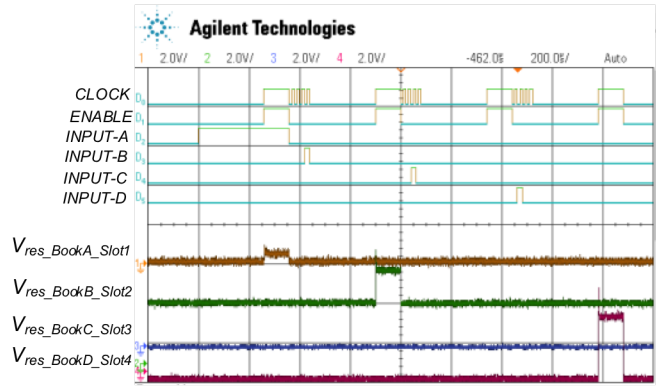

Fig. 14. Stimulus currents at corresponding slots in different books.

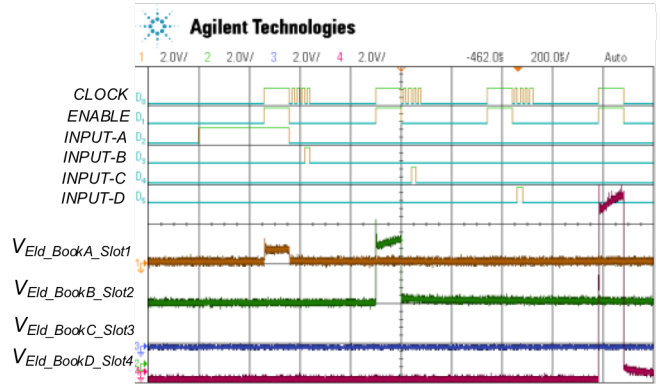

Fig. 15. Anode-cathode voltages of corresponding slots in different books.

V. Design Example – Measured Results

The ASIC was implemented using XFAB's 0.6-µm HV CMOS process. The ASIC has a total of 17 input-outputs (IOs) laid out in a predefined pattern for easy connection to the implant cable (containing 5 wires) and electrodes (3 electrodes per tripole × 4 tripoles = 12). Fig. 9 shows the die photo of the ASIC and Table V lists some of its features and measured performance. The central hub was built on a printed circuit board using off-the-shelf components. Four *Active Books* (each with an ASIC connected to a Book) were connected to the central hub via medical grade Copper cable.

Fig. 10 shows the demodulation of *INPUT-A*, *CLOCK* and *ENABLE* from the RF carrier. Fig. 11 shows the output voltage of the dc-dc converter which is independent of V_{DC}. V_{DDA} can be set to 18 V, 16.5 V, 15 V, 13.5 V, 12 V, 10.5 V, 9 V and 7.5 V by the microcontroller. The ratio R_1/R_2 used in the system is slightly higher than the theoretical calculation in (3). This is due to the limited power from the secondary coil that can be made available to the input of the dc-dc converter.

Fig. 12 shows the response of the system when the hub receives high temperature information from an ASIC. To simulate the high-temperature condition, the ASIC was placed in an environment temperature chamber, which was set to 41°C. The hub was placed outside the chamber and had an ambient temperature of 17°C. Fig. 12 shows the central hub supplies active V_{DDA}, *CLOCK* and *INOUT* signals before

being told the surface temperature of the ASIC. After sending a temperature-enquiry command to the ASIC and detecting its surface temperature at 41 ^{o}C, the central hub shuts down all five wires.

Fig. 13 shows the response of the system to the low anode voltage. The V_{DDA} started with 18 V. Then a *Measure_Slot1_Anode1* command was sent to the ASIC and it returned with '1101011' meaning the peak anode voltage was between 9.75 V and 11.25 V. The microcontroller reacted accordingly and instructed the dc-dc converter to provide a level of possible supply voltage (which was just above 12 V in this case).

Figs. 14 and 15 show the stimulation performance of the system with electrodes in physiological saline solution. Among 16 available channels, *Slot* 1 of *Book A*, *Slot* 2 of *Book B*, *Slot* 3 of *Book C* and *Slot* 4 of *Book D* were chosen for stimulation. Before the stimulation, the amplitude of the stimulus current on *Book A-D* was programmed to 1 mA, 4 mA, 0 mA and 8 mA, respectively. The width of the stimulation pulse, 100 µs in Fig. 14, was set by the width of the corresponding pulse on the *ENABLE* line. The stimulus current in each channel was monitored by a floating-input differential probe (Pico Technology TA044) measuring the voltage across a 420 Ω resistor placed in series with the cathode electrode. Fig. 15 shows the voltage between the cathode and one of the anodes in each stimulating channel. As evident from the figure, there is no noticeable crosstalk between different channels.

VI. Conclusion

Recent advances in scalable implantable stimulation systems using networked ASICs for use in applications with a large number of electrodes have been reviewed. As an example the detailed design has been presented of an implantable neurostimulation system for restoring lower limb functions in paraplegics after spinal cord injury. It comprises four *Active Books*, each with an ASIC intimately connected to twelve electrodes, an implanted central hub for controlling the *Active Books*, and an inductively coupled power and data telemetry. In addition to stimulation, the ASIC monitors temperature, humidity and electrode voltage levels. The information from the sensors on the ASIC and cable leakage current tests, ensure that the operation of the implant never exceeds prescribed safety limits. The implant architecture is scalable and a larger number of stimulating channels can be accommodated by using more *Active Books*.

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