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ScienceDirect

Energy Procedia 92 (2016) 661 – 668

Energy Procedia

6th International Conference on Silicon Photovoltaics, SiliconPV 2016

$Al_{0.2}Ga_{0.8}As$ solar cells monolithically grown on Si and GaAs by MBE for III-V/Si tandem dual-junction applications

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Abstract

$Al_{0.2}Ga_{0.8}As$ photovoltaic solar cells have been monolithically grown on silicon substrates by Molecular Beam Epitaxy. Due to the 4% lattice mismatch between AlGaAs and Si, Threading Dislocations (TDs) nucleate at the III-V/Si interface and propagate to the active region of the cells where they act as recombination centers, reducing the performances of the devices. In order to reduce the Threading Dislocation Density (TDD) in the active layers of the cells, InAlAs Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs) have been used. For one of the samples, in-situ Thermal Cycle Annealing (TCA) steps have additionally been performed during growth. For comparison purposes, reference $Al_{0.2}Ga_{0.8}As$ solar cells have been grown lattice-matched on GaAs. For the sample grown on Si without TCA, the TDD has been reduced from over $7\times10^{9}cm^{-2}$ at the III-V/Si interface to $3\times10^{7}cm^{-2}$ in the base of the cells. With TCA, the TDD has been reduced throughout the sample from over $3\times10^{9}cm^{-2}$ in the initial epilayers to $8(\pm2)\times10^{6}cm^{-2}$ in the base of the cells. For the best devices, the V_{oc} improves from 833mV on Si without TCA to 895mV using TCA, compared with 1070mV for the reference sample grown lattice-matched on GaAs. Similarly the fill factor improves from 73.7% on Si without TCA to 74.8% using TCA, compared with 78.4% on GaAs. The high bandgap-voltage offset obtained both on Si and GaAs indicates a non-optimal bulk AlGaAs material quality due to non-ideal growth conditions.

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Peer review by the scientific conference committee of SiliconPV 2016 under responsibility of PSE AG.

Keywords: III-V on silicon; AlGaAs solar cell; MBE; Threading dislocation density; Dislocation filter; Thermal cycle annealing

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Peer review by the scientific conference committee of SiliconPV 2016 under responsibility of PSE AG.
doi:10.1016/j.egypro.2016.07.037

1. Introduction

Integration of high quality III-V materials on a comparatively low cost silicon substrate is of high interest for photovoltaic applications. III-V on silicon enables the development of solar cells overcoming the ≈29% efficiency limit inherent to market dominant c-Si monojunction technology [1-2] by integrating a higher bandgap III-V top cell on a c-Si bottom cell acting as a substrate. Efficiency of 29.8±1.5% has been recently reported using a 4-terminal mechanically stacked GaInP/Si architecture [3]. Separate preparation of the III-V and Si subcells, before bonding or mechanical stacking, presents the advantage of optimal material quality for both cells. In counterpart it involves numerous fabrication steps, including a separation step of the III-V subcell from its growth substrate in a process akin to Epitaxial Lift-Off (ELO) [4-5]. This hinders the industrial potential of the technology, as substrate reuse after lift-off can be challenging, especially in the case of large industrial-size wafers.

An alternative pathway consists in the direct epitaxial growth of III-V materials on a Si substrate acting as a bottom cell. In the case of III-V/Si series-connected dual junction architectures, a bandgap of 1.7-1.8eV is needed for the III-V top cell [6-8]. As no nitrogen-free III-V material is lattice-matched to Si, a lattice-mismatched approach is required. Because of the difference of lattice parameters between the Si substrate and the III-V top cell, Threading Dislocations (TDs) nucleate at the III-V/Si interface and propagate in the epilayers to the active region of the top cell. There they act as recombination centers, reducing minority carriers diffusion length and lifetime and degrading the performances of the III-V subcell, in particular its V_{oc}. In order to obtain high efficiency III-V/Si devices, high III-V top cell material quality with a Threading Dislocation Density (TDD) in the 10^5-10^6cm^{-2} or lower is consequently needed [9].

Soga *et. al*. first demonstrated AlGaAs/Si tandem dual junction cells in the 1990s [10-11], using MOCVD growth of 1.61eV $Al_{0.15}Ga_{0.85}As$ on Si coupled with in-situ Thermal Cycle Annealing (TCA) steps to reduce the TDD in the AlGaAs top cell to 1.1×10^7cm^{-2}. Higher bandgap $Al_{0.22}Ga_{0.78}As$ cells, with better spectral matching to a Si bottom cell, were also grown. However high material quality proved challenging to attain with such a high Al content (22%) and the best reported TDD was twice as high at 2.1×10^7cm^{-2} [12].

Chen *et. al*. have recently demonstrated high quality AlGaAs monolithically grown on Si by MBE using Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs), leading to high-performance quantum dot lasers for silicon photonics applications [13-14]. In particular, a TDD in the 10^5cm^{-2} in the active region of the laser has been demonstrated using TCA steps in combination with SLS DFLs [14]. The same SLS DFL technique has been applied to 1.7eV $Al_{0.2}Ga_{0.8}As$ solar cells grown on Si, yielding a TDD of $1(\pm0.2)\times10^7$cm^{-2} [15]. In this paper, we report recent progress in the improvement of the growth sequence of such structures. In particular we present the impact of in-situ TCA steps, similar to the ones developed by Soga *et. al*. [10-12], in conjunction with DFLs on the performances of $Al_{0.2}Ga_{0.8}As$ solar cells grown on Si substrates.

2. Experimental methods

All growth runs were performed in a Veeco GEN930 solid-source Molecular Beam Epitaxy (MBE) reactor equipped with an infrared pyrometer and a substrate holder-mounted thermocouple to measure sample temperatures during growth. Reflection High Energy Electron Diffraction (RHEED) was used to in-situ characterize the samples surface evolution during growth runs. Three samples were grown: one on Si with TCA, one on Si without TCA and one reference sample lattice-matched on GaAs. TCA improves the material quality of the epilayers by increasing the mobility of TDs, thus enhancing the probability of self-annihilation of conjugated TDs. In order to avoid Anti-Phase Domains (APDs) formation due to polar-on-nonpolar epitaxy, n-type Si (100) substrates offcut 4° toward the [110] plane were used [16-17]. A standard n-type GaAs (100) substrate was used for the reference sample.

Structure of the samples grown on Si is presented in Figure 1. Subsequent to the AlGaAs nucleation layer, an AlAs/GaAs superlattice has been used to smooth out the growth surface followed by 4 InAlAs/AlAs SLS DFLs. The structure of the SLS DFLs has been described in a previous publication [15]. For the sample grown using in-situ annealing, TCA of the SLS DLFs has been performed 5 times, with the growth halted during annealing. Details on the TCA sequence used can be found in Ref. [14]. On GaAs, only the active layers of the cell – contacting layer, Back Surface Field (BSF), base, emitter, window and capping layer – have been grown on top of a 200nm GaAs buffer layer, without any TCA.

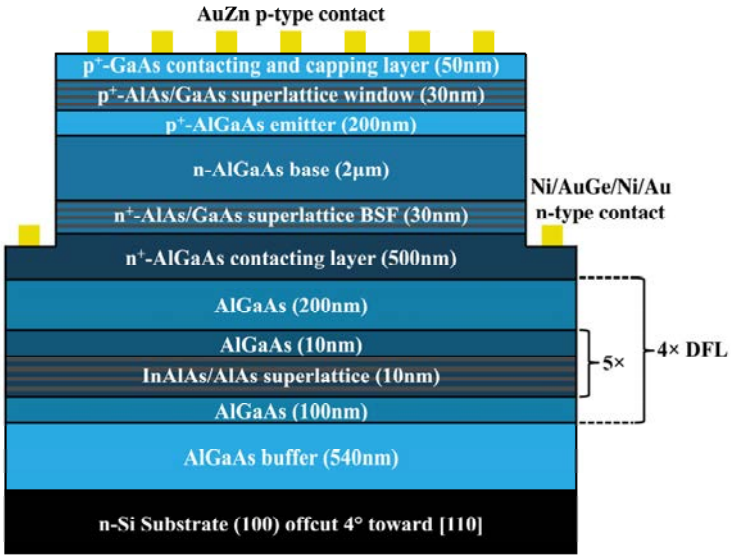

Fig. 1. Structure of the samples grown lattice-mismatched on Si. For the reference sample grown lattice-matched on GaAs, only the contacting layer, BSF, base, emitter, window and capping layer have been grown on top of an initial 200nm GaAs buffer.

Standard photolithography techniques were used for device fabrication. Access to the n-type bottom contacting layer and isolation of individual 3×3mm devices were first performed by mesa-etching using an H_2SO_4:H_2O_2:H_2O (1:10:80) selective etching solution. Contacts to the n-type and p-type regions were deposited by thermal evaporation. An Ni/AuGe/Ni/Au (5nm/1000nm/30nm/200nm) architecture, annealed at 400°C for 60 seconds, has been used for the contact to the n-type region before deposition of the 200nm-thick AuZn contact to the p-type region. Given the high shadowing due to the 3.14mm^2 front grid contact, current densities and efficiencies reported here correspond to the 5.86mm^2 active area of the devices. No anti-reflection coating was applied on the devices. The 50nm-thick top GaAs contacting and capping layer was not etched in order to protect the aluminum-rich oxygen-sensitive underlying layers. Consequently this capping layer is responsible for a non-negligible parasitic absorption, contributing to a current density loss evaluated at around 6mA.cm^{-2}.

Structural properties of the samples have been investigated using Transmission Electron Microscopy (TEM). Samples were prepared for cross-sectional TEM using mechanical polishing followed by ion-milling in a Fischione 1010 ion mill. An FEI Titan 80-300S TEM at 300keV, fitted with a CEOS image corrector, was used to perform the observations. Photoluminescence spectra of the samples were acquired in steady-state at room temperature using a Nanometrics RPM2000 rapid photoluminescence mapping system. Current density vs. voltage (J-V) curves were measured under illumination at 25°C with a Keithley 2400 sourcemeter coupled with ReRa Tracer 3.0 software. The light source used was a calibrated AM1.5G spectrum LOT solar simulator equipped with a filtered xenon lamp.

3. Results and discussion

Figure 2 presents cross-sectional TEM images of the samples grown lattice-mismatched on Si with (a) and without (b) TCA. TCA provides a substantial improvement in material quality, with a reduction in TDD of about 2 to 3 times throughout the sample, compared with the sample grown without TCA. In particular, for the sample grown with TCA, the TDD has been reduced from 3×10^9cm^{-2} at the III-V/Si interface to $3(\pm0.2)\times10^7$cm^{-2} after the 4th DFL and $8(\pm2)\times10^6$cm^{-2} in the base of the cells. Without TCA, the TDD is reduced from 7×10^9cm^{-2} at the III-V/Si interface to $8(\pm0.2)\times10^7$cm^{-2} after the 4th DFL and $3(\pm0.2)\times10^7$cm^{-2} in the base of the cells. Figure 3 shows the evolution of the TDD throughout both samples.

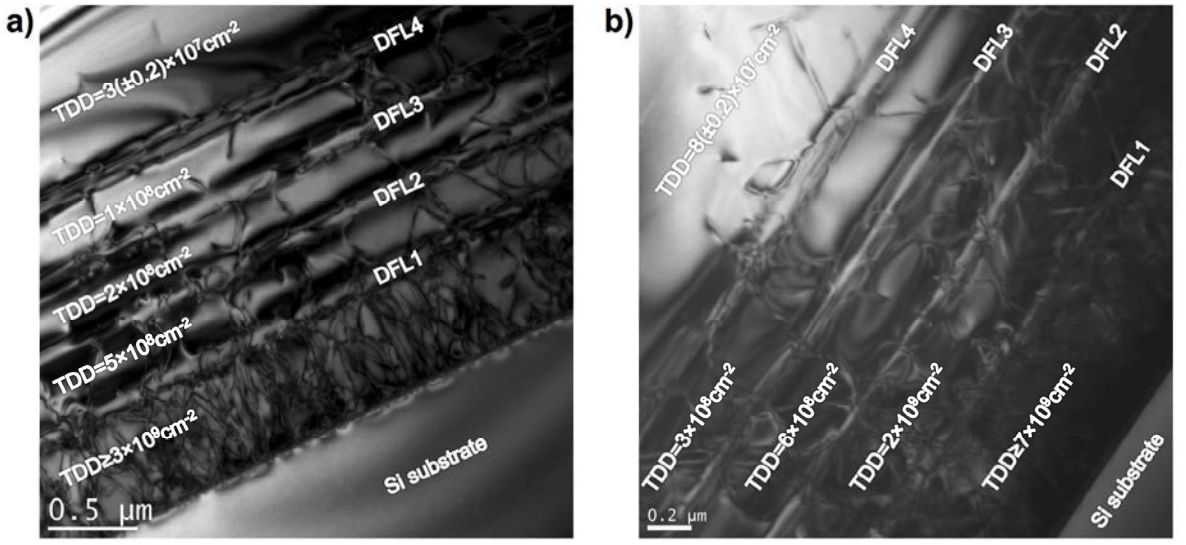

Fig. 2. TEM images of the samples grown lattice-mismatched on Si with (a) and without (b) Thermal Cycle Annealing (TCA) steps. A Threading Dislocation Density (TDD) 2 to 3 times lower has been measured throughout the sample grown with TCA.

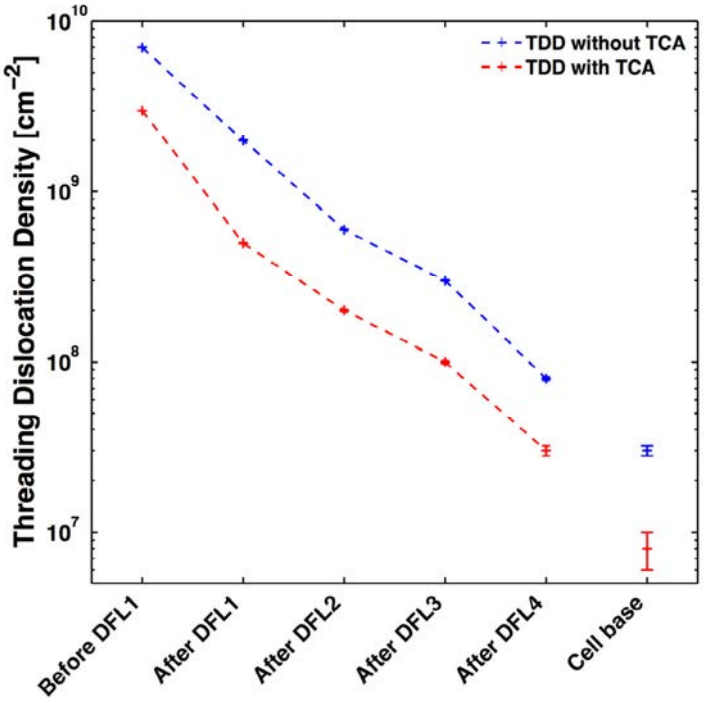

Fig. 3. Evolution of the Threading Dislocation Density (TDD) in the samples grown lattice-mismatched on Si with (red) and without (blue) TCA.

Photoluminescence spectra of the 3 samples are displayed on Figure 4. As expected, the sample grown lattice-matched on GaAs exhibits a higher intensity, with a peak at 729.4nm. Samples grown on Si with and without TCA present lower intensities, with peaks at 738.5nm and 740.6nm representing 42.4% and 29.6% of the peak intensity on GaAs, respectively. The difference in intensity is in agreement with the difference of TDD calculated from TEM, as TDs reduce the band-to-band radiative recombination probability. The difference in peak wavelength indicates a higher bandgap of exactly 1.70eV for the sample grown lattice-matched on GaAs, versus 1.68eV and 1.67eV for the samples grown on Si with and without TCA, respectively. An incomplete relaxation of the materials grown lattice-mismatched could possibly explain this difference in bandgap, although more work is needed to confirm this hypothesis.

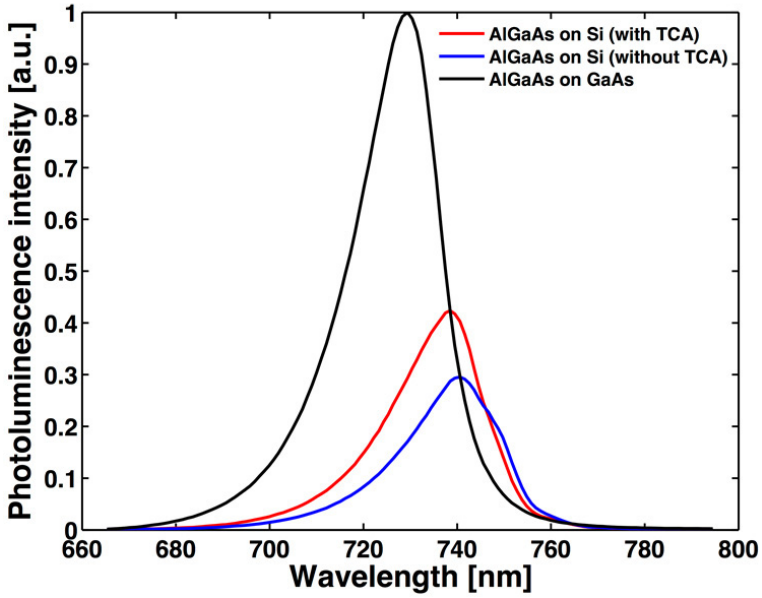

Fig. 4. Normalized photoluminescence spectra of the samples grown on Si with TCA (red), without TCA (blue) and on GaAs (black).

Figure 5 shows J-V curves of the best devices fabricated from each sample, acquired under illumination. The best cell grown on GaAs exhibits a slightly higher J_{sc}, at 6.22mA.cm^{-2}, compared with the best cells grown on Si with and without TCA, at 5.95mA.cm^{-2} and 5.93mA.cm^{-2}, respectively. A longer diffusion length, due to the absence of TDs on GaAs, could potentially explain this difference. Further work is needed to verify this hypothesis.

For all the samples, the best J_{scs} measured are comparatively small in regard with the J_{sc} target value of around 20mA.cm^{-2} required for current-matching with a future Si bottom cell. The two main causes of these low J_{scs} are related to the fabrication process of the cells. First, no Anti-Reflection Coating (ARC) or surface texturing have been applied to the cells, leading to a highly reflective specular front surface with an estimated reflectance of over 30%. Secondly, in order to protect the underlying AlAs/GaAs superlattice window from oxidation, the p-type 50nm-thick GaAs top contact and capping layer has not been etched. This contacting and capping layer is thus responsible for a non-negligible parasitic absorption, leading to a J_{sc} loss evaluated to around 5 to 6mA.cm^{-2}.

In order to avoid these parasitic reflection and absorption, future cell designs are planned to incorporate an ARC as well as a state-of-the-art AlInP window layer, instead of the current AlAs/GaAs superlattice window layer. As a result the GaAs capping and contacting layer may be selectively etched, using the AlInP window layer as an etch-stop. This should result in a drastic improvement in J_{sc}, from the present 6mA.cm^{-2} to between 15 and 18mA.cm^{-2}. Further improvement of the cell architecture and the growth parameters, in particular to optimize the diffusion length of minority carriers in the base and the absorption in the highly-doped emitter, should yield current density values high enough for current-matching with a potential Si bottom cell.

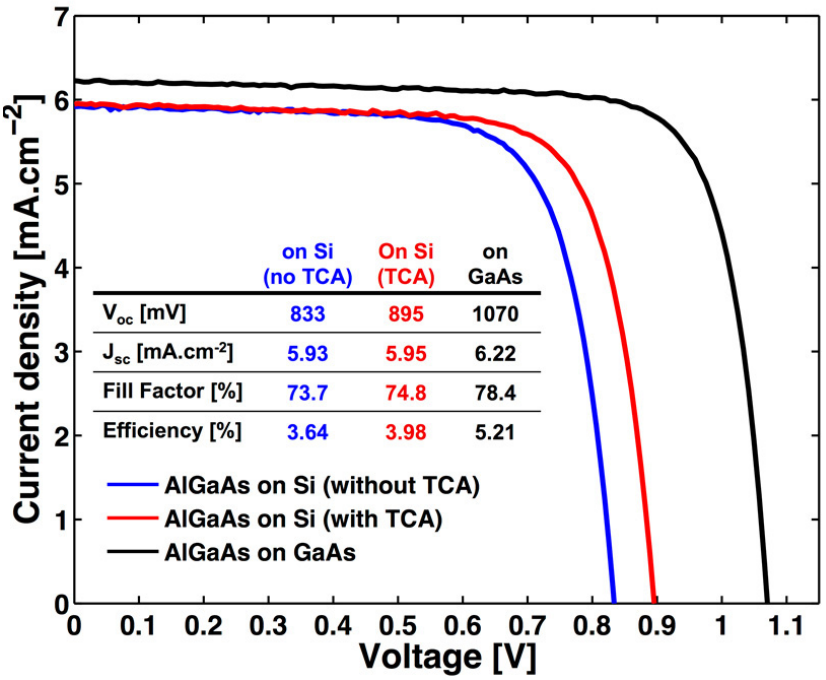

Fig. 5. J-V curves, acquired under AM1.5G spectrum illumination, of the best devices grown on Si with TCA (red), on Si without TCA (blue) and on GaAs (black). Cells parameters are also indicated.

Due to the presence of TDs in the active region of the cells, the samples grown on Si exhibit lower V_{ocs} than the reference cell grown on GaAs. However, the cell grown with TCA exhibits a non-negligible voltage recovery with a V_{oc} of 895mV, compared to 833mV without TCA and 1070mV on GaAs. This improvement of V_{oc} is in agreement with the higher photoluminescence peak intensity and the lower TDD exhibited by the sample grown with TCA.

An improvement of the fill factor has also been measured, from 73.7% without TCA to 74.8% with TCA, compared with 78.4% on GaAs. Most of this difference in fill factor, in particular between the two samples grown on Si, can be related to the difference in V_{oc}, as there is a direct correlation between open-circuit voltage and fill factor [18]. Moreover, for the samples grown on Si, the dominant recombination pathway corresponds to non-radiative recombinations in the depletion zone, associated with an ideality factor n=2. The overall ideality factor of the cells is thus increased in the presence of a non-negligible TDD, leading to a lower fill factor. This explains the gap in fill factor between the samples grown lattice-mismatched on Si and the sample grown lattice-matched on GaAs.

For all the cells, the bangap-voltage offset, defined as $W_{oc}=E_g/q-V_{oc}$, is high compared to the semi-empirical ≈0.4V expected from high performance III-V solar cells. High W_{oc} values indicate a high dark saturation current. Although this result is expected for TD-rich cells grown lattice-mismatched on Si, a high W_{oc} value of 630mV for the reference cell grown lattice-matched on GaAs suggests issues with the structure or the material quality of the cells. High W_{oc} values have been similarly reported in previous work [14]. As the cell structure consists of a state-of-the-art p-n junction III-V solar cell including a window layer and a Back Surface Field (BSF), the design of the devices is probably not at fault. Material quality of the bulk AlGaAs, leading to a high defect density on top of potential TDs, is more likely responsible for the low voltage performances of the devices. As high Al content AlGaAs growth is challenging, with in particular a strong sensitivity to potential oxygen contamination [19], these results are not fully unexpected. Optimization of the background conditions and of the growth parameters is thus needed to achieve high material quality AlGaAs on Si and on GaAs, enabling high performance devices.

4. Conclusion

$Al_{0.2}Ga_{0.8}As$ solar cells, with a bandgap suitable for a top cell in III-V/Si tandem dual junction architectures, have been grown on Si and GaAs substrates. To reduce the Threading Dislocation Density (TDD) of the samples grown lattice-mismatched on Si, Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs) have been used. For one of the samples, in-situ Thermal Cycle Annealing (TCA) of the DFLs has also been performed. Without TCA, the TDD has been reduced from $8\times10^{9}cm^{-2}$ at the III-V/Si interface to $3(\pm0.2)\times10^{7}cm^{-2}$ in the active layers of the top cell. For the sample grown with TCA, the TDD has been further reduced from $3\times10^{9}cm^{-2}$ in the initial epilayers to $8(\pm2)\times10^{6}cm^{-2}$ in the base of the cells. As expected, the sample grown with TCA exhibits higher photoluminescence peak intensity than the one grown without TCA, reflecting the higher material quality achieved using TCA. The photoluminescence peak intensity is however still 57.6% lower than one achieved on GaAs. Similarly, a V_{oc} recovery is demonstrated using TCA, from 833mV to 895mV. However, low AlGaAs bulk material quality, on Si as well as on GaAs, is hindering the performance of the devices. In particular high bandgap-voltage offsets – defined as $W_{oc}=E_g/q-V_{oc}$ – of 630mV, 784mV and 840mV have been respectively measured on GaAs, Si with TCA and Si without TCA. Optimization of the background condition and growth sequence is thus needed to improve the AlGaAs bulk material quality and achieve high performance devices.

Acknowledgements

This work is supported by Total SA. H. Liu would like to thank The Royal Society for funding his University Research Fellowship. The authors acknowledge the support of the National Science Foundation of the U.S. (EPSCoR Grant # OIA-1457888).

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