An Improved Wideband CMOS Current Driver for Bioimpedance Applications

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***Abstract*— A wideband, CMOS current driver for bioimpedance measurement applications has been designed employing nonlinear feedback. With the introduction of phase compensation, the circuit is able to operate at frequencies higher than the pole frequency of the output transconductor with minimum phase delay. Moreover, it isolates the poles required for stability from the high frequency characteristics of the output transconductor. The circuit has been developed in a 0.35-µm CMOS technology. It operates from ±2.5 V power supplies and can deliver multifrequency (multisine) currents to the load. Simulation results show that for a 1 mAp-p output current, the phase delay is below 1º for frequencies up to 3 MHz, rising to 1.5º at 5 MHz.**

I. INTRODUCTION

Multifrequency bioimpedance applications including electrical impedance spectroscopy (EIS) of biological tissues (e.g., for cancer detection) and electrical impedance tomography for imaging require wideband, accurate current drivers. The upper frequency limitations of the current driver and the stray capacitances while generating current into the tissue via electrodes, are two major complications to consider [1]. The upper frequency limitations are the phase delay and reduction in output impedance. Small phase delay is an important factor in accurate bioimpedance measurements using synchronous and magnitude/phase detection systems [2]. Placing the current driver close to the electrodes can reduce the effect of the stray capacitors, but some effect will still remain.

In [3], a single-ended nonlinear feedback CMOS current driver was introduced capable of isolating the poles required for stability from the high frequency characteristics of the output transconductor. However, its performance at high frequencies was limited by increased phase delay in the output current. To overcome this, an improved wideband current driver based on [3] is presented here that operates in a fully-differential configuration. As such, it can be used in applications such as tetrapolar EIS where floating loads are desired. With the introduction of a phase compensation circuit the current driver is able to operate at frequencies close to the pole frequency of the output transconductor with appreciable phase reduction. Another important aspect of the phase compensation is that the output impedance of the current driver remains (largely) constant throughout the entire range of operational frequencies (40 kHz–5 MHz). In addition, the new configuration of the sense resistors (R_s) for measuring the output current (I_{drive}) provides a more compact configuration compared to the current driver in [3].

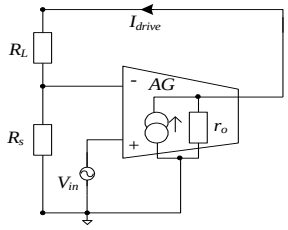


Fig. 1. Basic linear feedback circuit.

The rest of the paper is organized as follows. Section II outlines the operating principles of feedback-based current drivers including the architecture of the new fully differential nonlinear feedback driver. The integrated circuit design of the proposed current driver is presented in Section III. Section IV discusses the simulation results and multifrequency operation of the current driver. Section V concludes the paper.

II. CURRENT DRIVER FEEDBACK CIRCUITS

A. Linear Feedback Current Driver

The linear current feedback that forms the basis of the proposed current driver is shown in Fig. 1 [3], [4]. The output current is given by

$$I_{drive} = \frac{V_{in}}{R_s} \frac{1}{1+\frac{1}{AGR_s}\left(1+\frac{R_L+R_s}{r_o}\right)} \tag{1}$$

where A is the voltage amplifier, and G a transconductor, R_s is the sense resistor, R_L is the load resistor, and r_o is the output resistance of G.

For $r_o >> R_L + R_s$ and $AGR_s >> 1$

$$I_{drive} = \frac{V_{in}}{R_s}. \tag{2}$$

The load R_L in (1) contributes to an added inaccuracy such that the output resistance can be defined as

$$R_{out} = AGR_s r_o . \quad (3)$$

At high frequencies due to low frequency dominant pole in (3), the output impedance is not resistive but approximately a capacitance, C_p, defined as

$$C_p = \frac{1}{\omega_d R_s AG r_o} \quad (4)$$

where ω_d is the dominant pole. The value of C_p can be in the order of 2–10 pF in addition to any added stray capacitances.

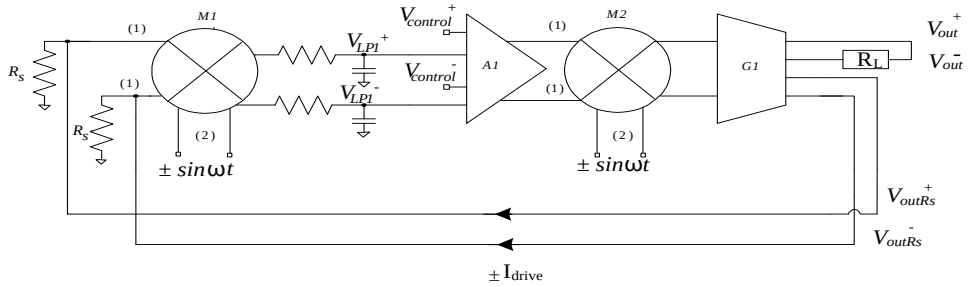


Fig. 2. Block diagram of nonlinear current driver.

B. Nonlinear Current Driver With Phase Compensation

The fully-differential current driver in Fig. 2 has the advantage that the dominant pole does not affect its high frequency operation (at the expense of a longer transient response). By using two identical sense resistors, R_s, the output current, I_{drive}, is dependent on the matching of the ratio of two resistors rather than the absolute value of one resistor, hence improving accuracy.

The amplitude of the differential current I_{drive} is set by the dc control voltages, $\pm V_{control}$, while its frequency is dictated by the frequency of the differential $sin\omega t$ input signals at terminals (2) of multipliers *M1* (which can be either an analog or switch multiplier) and *M2*. The two identical low cut-off frequency RC low pass filters attenuate the harmonic components at the output of multiplier *M1* to well below the dc output component ($\pm V_{LP}$), which is then compared to dc control voltages and amplified by *A1*. The *M2* analog multiplier multiplies a dc voltage from *A1* with the sinωt ac signal to provide an amplitude controlled ac output signal. Among the two differential outputs of the transconductor *G1* one is used to drive the load (R_L) while the other is used for feedback via R_s. The dc component of the output of a switch multiplier (simpler than an analog multiplier) *M1* is $(2/\pi)(V_p/2)$, where V_p is the peak voltage of the ac signal across R_s. Since the same equations as in the circuit in Fig. 1 apply to this current driver, the analogous loop gain of the circuit in Fig. 2 is $(2/\pi)AGR_s$ due to the ac-dc conversion at the integrator.

If $\frac{2}{\pi} AGR_s >> 1$, then (2) becomes

$$I_{drive(peak)} = \pi \frac{V_{control}}{R_s} . \quad (5)$$

The output of the current driver in this configuration is defined by the output resistance, r_o, of the transconductor *G1*.

In this design C_p becomes negligible as the poles of transconductor *G1* are at high frequencies and no longer include the low frequency dominant pole. The accuracy of the conversion of ac signal to dc signal is affected by the phase delay at the two inputs of multiplier *M*1, which translates to an added inaccuracy in I_{drive}. As such, the ac-dc transfer is reduced by a factor of $cos\Phi$, where Φ is the phase delay. To extend the accuracy of I_{drive} at high frequencies its phase delay must be minimized.

Fig. 3 shows a circuit that considerably reduces the phase delay of I_{drive} to beyond the pole frequencies of (*M*1, *G*1) and (*M*2, *G*2). The upper circuit with *M1* and *M2*, is the basic current driver generating current into the load as in Fig. 2. The lower circuit in Fig. 3, which is almost identical to the upper circuit but with multipliers *M3* and *M4* driven by $cos\omega t$ and zero control voltage, provides the necessary delay compensation. The compensation circuit (lower circuit) senses the amplitude of the out-of-phase component of the voltage across R_s and generates an amplified version of it. The outputs of both circuits are added and feedback nearly cancel out the out of phase components. The output of *G2* is always at 90° to *G*1 at all frequencies [5]. The other important feature of the phase compensation is that the output impedance of the current driver does not degrade at high frequencies.

III. Integrated Circuit Design

The circuit schematic of each sub-block of the new current driver is shown in Fig. 4. Multipliers *M1* and *M3* are based on the classic CMOS switch multiplier operated by non-overlapping clocks, *CLK* and *CLK'*, as in Fig. 4(a). The integrator pole is at 10 Hz frequency and uses a passive RC filter (off chip due to its large area). The amplifier *A* is based on the differential difference amplifier (DDA) [Fig.4 (b)] where transistors M1−M4 form two differential pairs whose output currents are summed at the drains of the diode-connected transistors M5 and M6. All the current mirrors have a ratio of 1:1. Transistor pairs M15-M15A and M16-M16A provide common mode feedback (CMFB) that can be controlled by voltage V_b. The open loop gain of the DDA is 470 V/V. The four-

quadrant multiplier [Fig. 4(c)] is based on two squarers using flipped voltage followers [6]. There are four pairs of squarer transistors (M1-M6) with associated flipped voltage followers. Relatively large transistor dimensions of W = 10 µm and L = 5 µm are used to allow a gate voltage swing of ±0.5 V into the squarer transistors. The transconductor G in Fig. 3 has been merged into the multiplier *M2* and *M4*. The output currents from the multiplier (I_1-I_4) are mirrored to current amplifiers via four current mirrors in the middle of Fig. 4(c) with a ratio of 1:10. The difference of the sum of output currents is achieved via a four-input current amplifier represented by M16A-M16D [7]. The four identical current amplifiers are responsible for two differential outputs; one to the load and the other for feedback. The multiplier transconductance is 1.6 mA/V. Conventional CMFB [7] is added at the output to stabilize the output common mode variation resulted from a floating load. The simulated overall loop gain of the current driver is about 480 V/V.

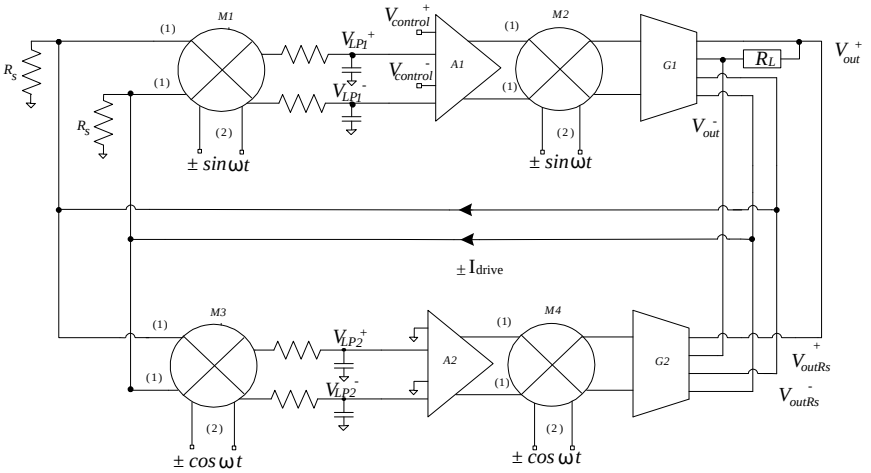


Fig. 3: Block diagram of current driver with its corresponding phase compensation.

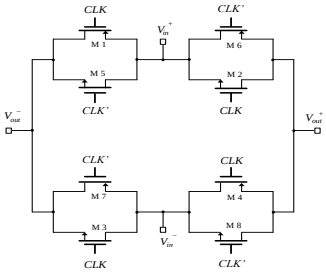


Fig 4 (a): Switch multiplier.

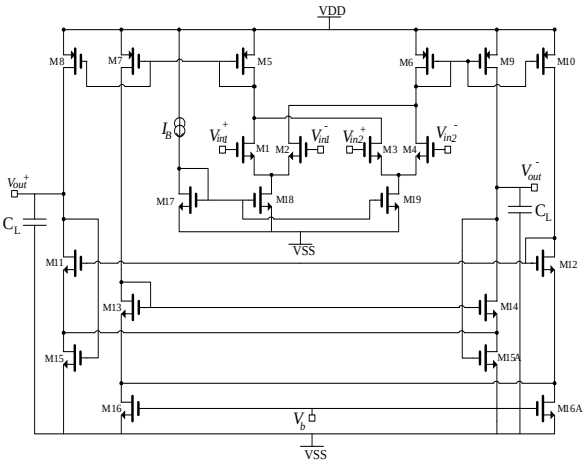


Fig. 4 (b): Differential difference amplifier (DDA).

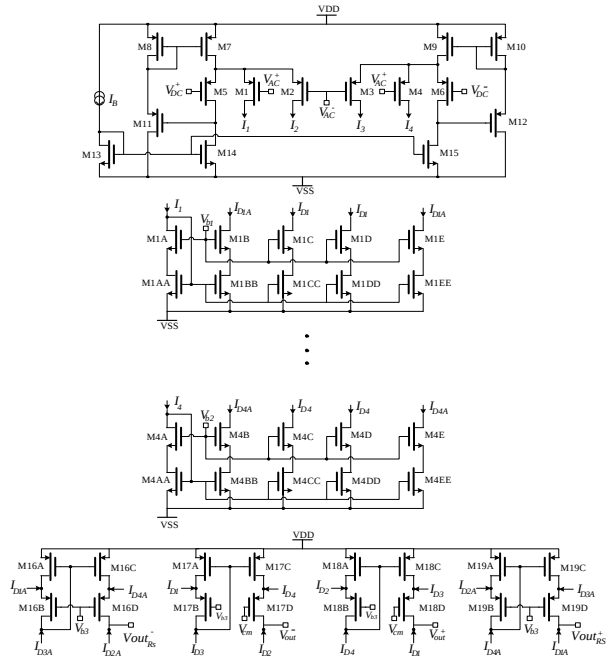


Fig. 4 (c) : Four quadrant analog multiplier and current amplifier.

IV. Simulation Results

The system has been designed in a 0.35-µm CMOS technology with ±2.5 V supply voltages. The variation of the amplitude of I_{drive} with $V_{control}$ is shown in Fig. 5. The sense resistors are 1000 Ω each .The current changes phase by 180° with the polarity of $V_{control}$. Fig. 6 demonstrates the I_{drive}

amplitude and phase variations over a wide frequency range for a current amplitude of 1 mA, with and without phase compensation. The current driver can be configured to operate with multifrequency (multisine) by connecting in parallel extra current drivers (with their corresponding phase compensation). The summed currents flow through the load and sense resistors. Fig. 7 shows the results for a dual frequency current driver at two frequencies of 500 kHz and 2 MHz. The DFT of the sum of the two equal currents of 500 µA across the load is seen at 500 kHz and 2 MHz. The accuracy of the currents is about 0.5%. The phase compensation does not affect the multifrequency operation. Table I show a comparison with previous current drivers in terms of bandwidth, phase delay and output impedance.

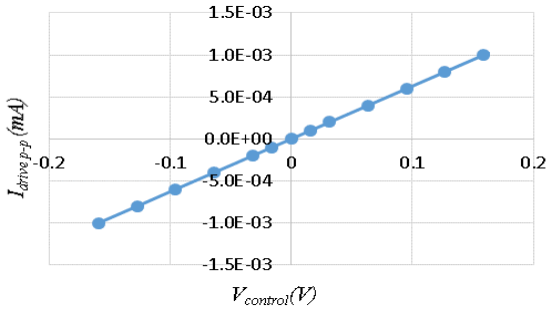
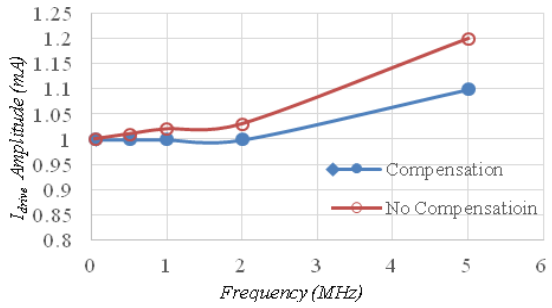
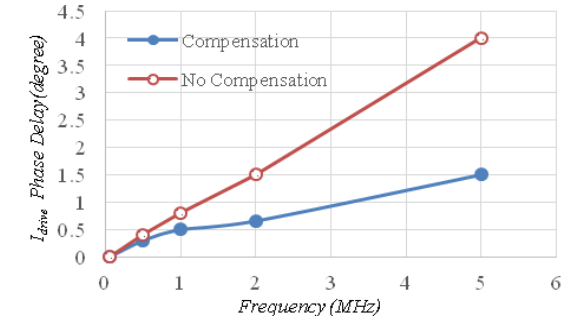


Fig. 5 : I_{drive} vs. $V_{control}$ measured at 100 kHz.



(a)



(b)

Fig. 6: Simulated results with and without compensation: (a) output current, (b) output phase.

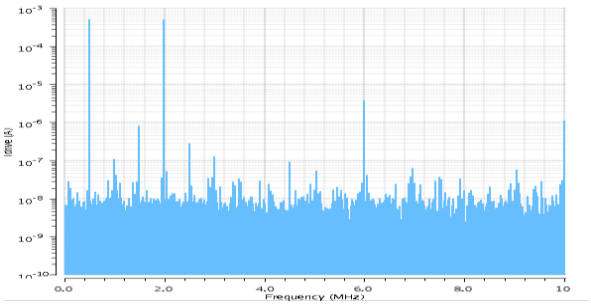


Fig. 7: Two sine waves at 500 kHz and 2 MHz with compensation. I_{drive} = 500 µA.

TABLE I. COMPARISON WITH OTHER WORK

	[1]	[3]	[4]	This work
Bandwidth	10 kHz - 1 MHz	10 kHz - 1 MHz	10 kHz - 1 MHz	40 kHz - 5 MHz
Phase Delay	3.6° at 1 MHz	16° at 1 MHz	9.5° at 1 MHz	1.1° at 4 MHz
Output Impedance	> 500 kΩ at 500 kHz	360 kΩ at 1 MHz	< 500 kΩ at 1 MHz	2 MΩ at 4 MHz

V. CONCLUSION

An improved wideband multifrequency current driver for bioimpedance applications has been proposed. The circuit is capable of operating at high frequencies near the pole frequency of the transconductor with minimum phase delay. The circuit has been designed and simulated in a 0.35-µm CMOS technology. The circuit is currently being laid out for tape out in November 2015 and measured results will be presented at the conference.

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