Dual-Mode CMOS Analog Front-End (AFE) for Electrical Impedance Spectroscopy (EIS) Systems*

Virgilio Valente, Dai Jiang and Andreas Demosthenous

***Abstract*— This paper presents the operation of a dual-mode wideband CMOS analog front-end (AFE) for electrical impedance spectroscopy. The chip combines two current-readout (CR) channels and four voltage-readout (VR) channels suitable for both bipolar and tetrapolar EIS analysis. The chip addresses the need for flexible readout units for real-time simultaneous single-cell and large scale tissue/organ analysis. Postlayout simulations show that the VR channel is capable of wideband operation up to 12 MHz with noise floor as low as 16.4 nV/Hz$^{1/2}$. A 2-bit control allows to select between a high-frequency low-gain channel and a bandwidth-limited high-gain channel. Each VR channel occupies an area of 0.48 mm^2.The CR channel is capable of 80 dB of dynamic range, by converting currents between 1 nA to 10μA, while achieving a noise floor of 1.4 pA/Hz$^{1/2}$. An automatic gain control (AGC) unit can be enabled in order maintain the sensor signal within the ADC dynamic range. Each CR channel occupies an area of 0.21 mm^2. The chip consumes between 290 μA and 690 μA per channel and operates from a 1.8V supply. The chip will be part of a fully flexible and configurable dual-mode EIS systems for impedance sensors and bioimpedance analysis.**

I. Introduction

Electrical impedance spectroscopy (EIS) is conventionally adopted for the monitoring of corrosion, batteries and device characterization. Over the last years EIS has gained widespread interest in electrochemical and biomedical research as a tool to study the electrical and physical properties of biological interfaces and provide valuable diagnostic information about potential pathological conditions of biological cells, tissues and organs. EIS is applied to the measurement of tissue impedance for disease and cancer detection [1], [2] or adopted for imaging purposes, as in electric impedance tomography [3]. In the field of electrochemical analysis, EIS can be employed to interrogate functionalized biosensors to detect changes in impedance due to the presence of target analytes, including enzymes, antibodies and DNA [4].

The main benefit of EIS stems from its non-invasive and non-destructive nature, based on the application of small voltage or currents to the biological environment, which have very little impact on the measured properties [5].

Latest advances in CMOS technology have permitted the integration of complex, multi-channel EIS systems as part of low-cost electroanalytical platforms [6]. Current EIS systems can provide simultaneous analysis of several biological parameters by combining on-chip electrode arrays and different sensing modalities on the same chip.

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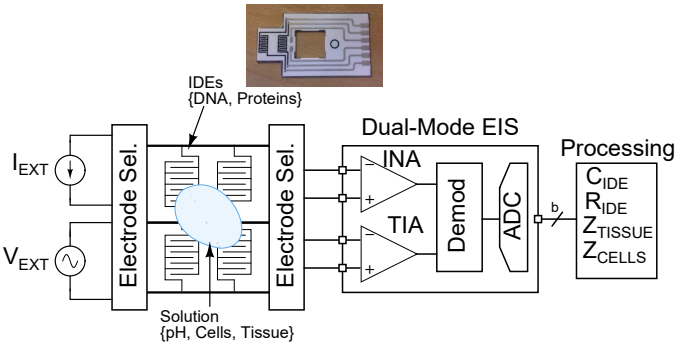

Fig. 1. Dual-mode EIS system. The system can be interfaced to a set of IDEs for both bipolar and tetrapolar spectroscopy measurements. Inset: Commercial dual interdigitated electrodes (IDEs).

In order to further improve the flexibility of integrated EIS systems, a CMOS EIS chip can be designed for dual-mode impedance sensing with the ability to interface to multi-target electrochemical sensors, for blood and fluid and single-cell analysis, and arrays of bioelectrodes for tissue and organ analysis. Current-mode and voltage-mode readouts, integrated on the same chip, can provide an adaptable platform to correlate single-cell biosensor studies with large-scale tissue or organ analysis for real-time cancer detection, imaging and characterization.

Fig. 1 shows the concept of a dual-mode EIS interfacing to a number of interdigitated electrodes (IDEs). The setup can be used to combine bipolar and tetrapolar measurement configurations. The electrodes can be either functionalized, in order to detect specific analytes, or combined to monitor impedance changes in the biological environment. Changes in impedance of the electrodes can be monitored by exciting one or more electrodes with a small voltage, reading out the current flowing through the electrodes and computing the electrode resistance or capacitance. Concurrently the interface impedance can be monitored by applying a differential current through two electrodes and measuring the voltage across two alternate electrodes.

A major component of a fully-integrated multi-target EIS system is the analog front-end (AFE) interface. As part of a low-cost wearable or implantable accurate bioimpedance measurement system, the AFE should be designed for low-noise (nV/Hz$^{1/2}$ or pA/Hz$^{1/2}$), high dynamic range (>80 dB), wideband operation (up to few MHz) and programmability.

This paper presents the operation of a multi-channel dual-

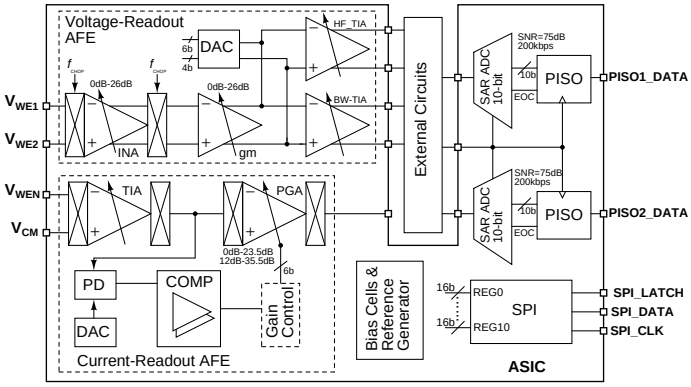

Fig. 2. Chip architecture.

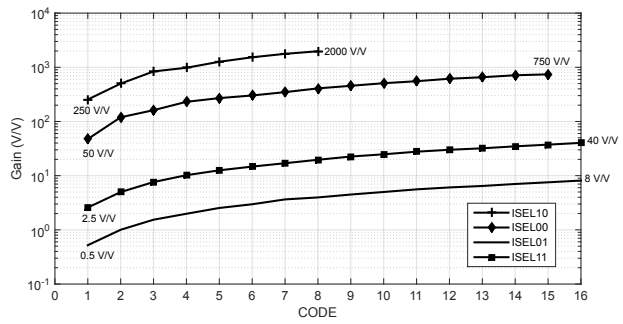

Fig. 3. Gain range of the VR buffer. The values reported are the design target values. Actual simulated values are reported in Table I

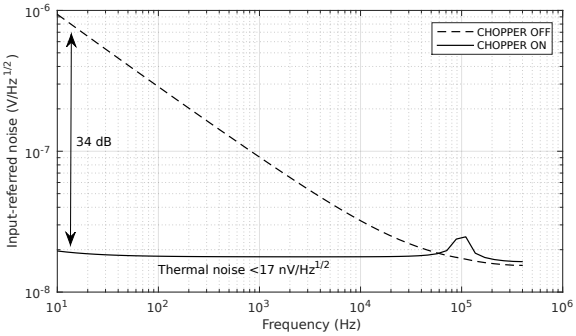

Fig. 4. Noise spectral density of the VR AFE IA with chopper disabled and enabled.

mode AFE for electrochemical and bioimpedance analysis. The system integrates current and voltage readout channels for bipolar and tetrapolar impedance measurements. The preliminary design of the AFE blocks was presented in [7]. This paper describes the full operation of the chip with postlayout simulations. The paper is organized as follows. Section II provides a description of the multi-channel dual-mode EIS AFE chip. Section III presents the simulated operation of the chip with a summary of the key performance parameters. Section IV concludes the paper.

II. System Architecture and Performance

The architecture of the EIS AFE chip is shown in Fig. 2. The chip allows for fully differential voltage readout (VR, 4 channels) of signals up to 12 MHz and single-ended rail-to-rail output current readout (CR, 3 channels). Two of the CR channels are equipped with an automatic gain control (AGC) unit that allows to extend the signal dynamic range. The AGC comprises a peak detector (PD), a relaxation-current DAC, two comparators, which detect the input signal level and a control logic unit (off-chip) that automatically sets the PGA voltage gain.

In the VR mode, the user can select between bandwidth-limited low-noise operation (up to 50 kHz) or high-frequency recording (up to 12 MHz). Each channel has programmable gain stages, bandwidth and enable signals that allow to turn off entire sections of the chip to save power. The chip can be operated by a microcontroller thanks to the on-chip serial-to-peripheral interface (SPI) using only three wires. The SPI consists of eleven 16-bit registers that control the chip enable signals, gain, bandwidth, channel selection and offset trimming. The analog output of each channel is buffered internally and available at pinout. Two 10-bit on-chip successive-approximation ADCs are available for digitization with a sampling frequency up to 150 kHz. The output of each ADC is converted to serial data via 2 parallel-in-serial-out (PISO) interfaces.

A. AFE

A dual-mode AFE comprises four fully-differential voltage-readout channels and two single-ended current-readout channels equipped with an automatic gain control (AGC) unit to extend the current dynamic range.

1) Voltage Readout (VR): Each VR channel comprises of a buffer amplifier stage with variable gain between 0 dB and 26 dB [7], followed by a similar buffer stage split in a bandwidth-limited (*BW*) and a high-frequency (*HF*) path. The *gm*-stage of the second-stage buffer is common to both paths, whereas the transimpedance amplifier (TIA) stages are designed with different gain and bandwidth specifications (see Fig. 2). The BW-limited channel is designed to have a high gain between 50 V/V and 2000 V/V, whereas the high-frequency channel has a lower gain between 0.5 V/V and 8 V/V. The gain ranges obtained during postlayout simulations are shown in Fig. 3. The gain range can be selected by changing the control signal, *ISEL*.

The simulated gain ranges are reported in Table I. The maximum deviation of the gain from the designed values were simulated to be 0.5 dB for ISEL00, 0.97 dB for ISEL10, 0.36 dB for ISEL10 and 0.26 dB for ISEL11. The VR buffers are chopper-stabilized in order to reduce the low-frequency, (*1/f*), noise. The chopper frequency is set to 100 kHz. A programmable 5-bit second-order passive filter is used to attenuate the high-frequency components resulting from chopping. The cut-off frequency of the filter is set to 35 kHz ±40%, tunable via a 5-bit capacitor array consisting of 500 fF unit capacitors.

Fig. 4 shows the simulated noise profile of the VR buffers with the chopper enabled and disabled. In the former

case, a 34dB reduction of noise is achieved. The noise floor was simulated to be below 17 nV/Hz$^{1/2}$. Detailed simulated results are reported in Table I.

Due to the large gain range that the VR AFE provides, an offset trimming unit was included. This is based on the use of current-steering DACs which unbalance the current in the g_m-stage input pair, in order to reduce the output offset voltage to zero. One 4-bit DAC biased with a 750 nA current is used for offset coarse calibration and a 6-bit DAC biased with a 10 nA current is used for fine calibration. The offset calibration unit is designed to compensate for $\pm$20 mV offsets.

2) Current Readout (CR) with AGC: The CR channel comprises a resistor-feedback (RESF) transimpedance amplifier (TIA) followed by a programmable-gain amplifier (PGA). The use of a RESF topology over a capacitive feedback (CF) topology was used as a compromise between a lower noise performance provide by the CF topology in contrast to the need for fast clocks or large capacitors to achieve a low gain in the order of kΩ. The gain of the TIA stage can be set to 10 kΩ, 50 kΩ or 100 kΩ. This allows to achieve an overall current-readout dynamic range of 80 dB, as shown by the results of postlayout simulations reported in Fig. 5. These results were obtained by running transient simulations with transient noise sources enabled and sweeping the input current between 100 pA and 1 mA and calculating the derivative of the resulting TIA output voltage. The lower and upper bounds of the TIA gain are determined by the noise level and the amplifier saturation level, respectively.

A chopper-stabilized opamp was used to implement the TIA.

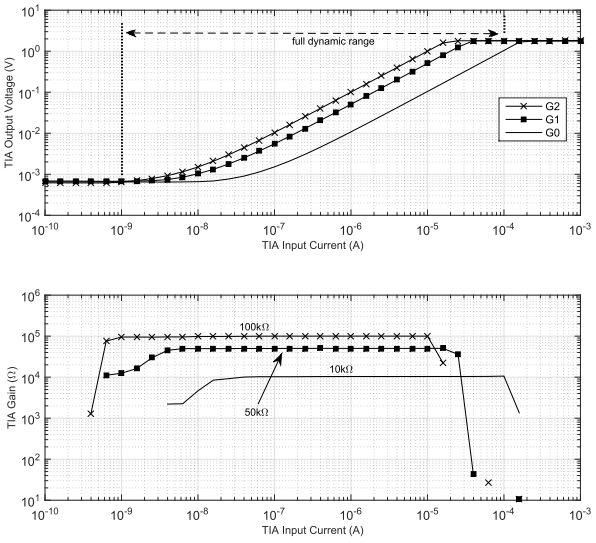

Fig. 5. TIA dynamic range at different gain settings.

The chopper frequency was set to 100 kHz. Fig. 6 shows simulated noise profiles of the TIA with enabled and disabled chopper. A 7dB improvement in noise performance was achieved with the chopper enabled. The simulated thermal

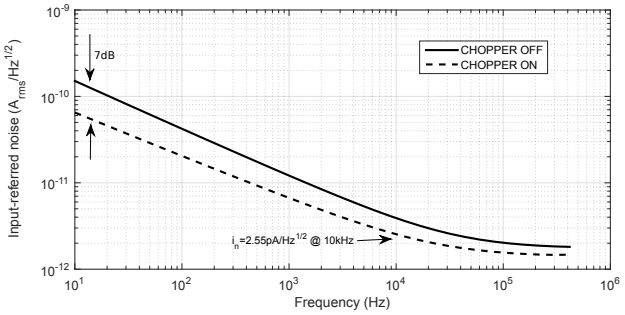

Fig. 6. Simulated input-referred noise of the TIA. When chopping is enabled the low-frequency noise reduces by approximately 7 dB.

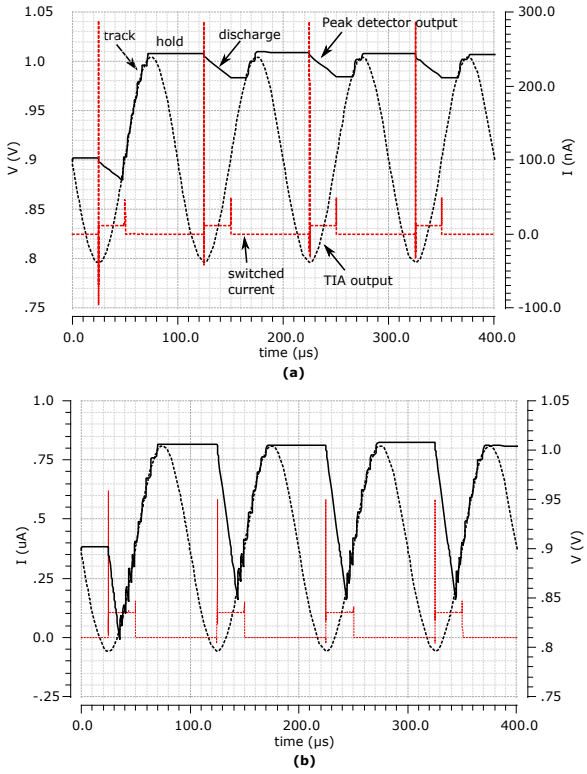

Fig. 7. Transient simulation of the adaptive PD unit at 10 kHz. The relaxation current is set to (a) 10nA and (b) 100nA and switched at the same frequency as the input signal with a 25% duty cycle. The output capacitor of the PD (external) is 300pF.

noise floor was in the order of 2.5 pA/Hz$^{1/2}$.

The CR AFE is equipped with a novel adaptive peak detector (PD), which allows to track the amplitude of the input signal and readily interface with a control logic circuit to adjust the amplitude of the TIA (coarse) or the PGA (fine) to keep the output signal within the ADC dynamic range. In order to accommodate for changes in input amplitude and frequency (consistent with an EIS analysis), the peak detector includes an active switched current DAC, which allows to control 3 operation phases: input tracking, holding the peak voltage on a capacitor and discharge the capacitor before the next cycle. The transient behavior of the adaptive PD is shown in Fig. 7 for a 10kHz input signal. The output

capacitor is 300pF and the switch current is set to 10nA (Fig. 7(a)) and 100nA (Fig. 7(b)).

The benefit of this architecture over conventional ones is twofold. Firstly, a large output capacitor can be used, which allows for a more accurate reading of the peak input voltage. In conventional PD architecture, a tradeoff exists between the value of the storing capacitor and the speed or tracking of the PD. Using a discharge switch to a reference voltage will decrease the bandwitdh of the PD. Passive discharge, on the other hand, would limit the response to the PD signals rapidly changing in amplitude. In addition, by using a programmable discharge current, the behavior of the PD can be made independent of the input frequency.

III. Chip Operation

The chip was designed in XFAB XH018 0.18μm 6-metal CMOS technology. It consists of 84 pads for a total area of 3.154-by-3.154 mm^2. The chip layout and the pinout are shown in Fig. 8. The performance of the chip was simulated in Cadence Spectre. The key performance parameters are summarized in Table I.

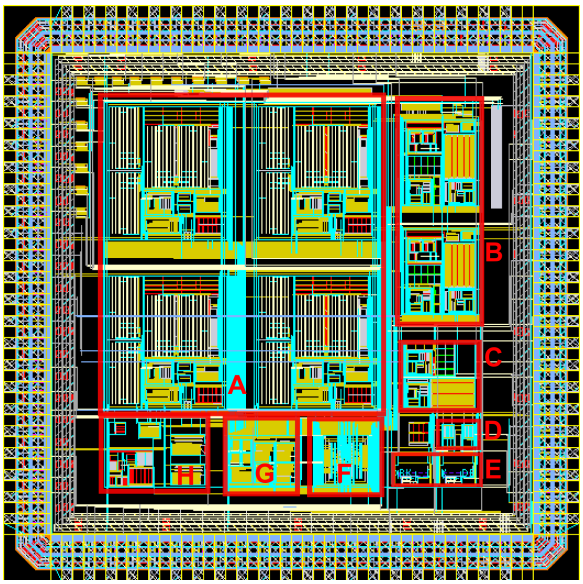

Fig. 8. Chip layout. **A**. 4-channel VR AFE. **B**. 2-channel CR AFE with AGC. **C**. CR AFE. **D**. PISO interface. **E** ADCs. **F**. SPI. **G**. Trimming DACs. **H**. Biasing cells.

The chip registers are programmed via a 3-wire SPI. Data is clocked in at a frequency of 1 MHz. A latch signal (SPI_LATCH) is used to write the data onto a register before the next register is addressed. At the end of the programming phase a signal can be applied to the interface and the output is available. Once the output is available it can be readout from the chip via the 10-bit ADC and the PISO interface, which converts the 10-bit output of the ADC into a data stream. An end-of-conversion (EOC) flag is used to clock the 10-bit PISO interface which streams out the data serially to a microcontroller.

TABLE I
Summary of Simulated Performance

PARAMETER	UNITS	VALUE
Technology	-	0.18μm CMOS
Number of pads	-	84
Chip active area	mm^2	4.2
Supply voltage	V	1.8
VR AFE		
Gain range	V/V	0.5 to 1975
BW LF	kHz	20 to 50
BW HF	MHz	6 to 12
CMRR	dB	100
Integrated noise	μV_{RMS}	17.6 (CHOPPER OFF)
(10 Hz - 100 kHz)	μV_{RMS}	5.5 (CHOPPER ON)
Thermal noise	nV/Hz$^{1/2}$	16.4
Max Current consumption	μA	690
CR AFE		
TIA Gain	Ω	10k, 50k, 100k
TIA Dynamic range	dB	80
PGA Gain range 1	V/V	1 to 15
PGA Gain range 2	V/V	4 to 60
TIA integrated noise	pA_{RMS}	292 (CHOPPER OFF)
(10 Hz - 100 kHz)	pA_{RMS}	202 (CHOPPER ON)
TIA thermal noise	pA/Hz$^{1/2}$	1.4
Max Current consumption (including AGC)	μA	530

IV. Conclusion

This paper has presented a dual-mode CMOS analog front-end suitable for voltage-mode and current-mode EIS. The operation of the chip and postlayout simulations of the individual units have shown its suitability for low-noise and wideband EIS measurements with large dynamic range.After silicon measurements the chip will be part of dual-mode EIS system and interfaced to screen-printed polymer-coated interdigitated electrodes.

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