Modelling the generation of Joule heating in defective thin oxide films

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***Abstract*—Thin oxide films are dominantly used as insulating materials in a wide range of CMOS electronic devices. Continuous scaling, governed by Moores Law, dictates that the thickness of oxides materials could be as thin as a few nanometers. Consequently, a generation of oxide defects, through field-driven and thermal-driven processes, presents a serious reliability challenge. On the other hand, a controllable formation of oxide defects in simple metal-insulator (oxide)-metal devices has recently attracted significant attention for the realization of Resistive RAMs (RRAMs) novel type of non-volatile memory technology that offers a low programming energy [1], a rapid switching [2], and a very high levels of integration [3]. In this paper we model the generating of Joule heating as a result of the current flow through a defective thin oxide layer. We use the representation of resistive network as well as the Fourier Heat Equation to simulate the oxide matrix and the heat flow. Our simulation demonstrates that temperatures generated by the Joule heating can easily reach the value of 900K or more after a few hundred microseconds. Precise control of the current flow timing is the key parameter to prevent the extensive heating and the oxide damage.**

***Index Terms*—RRAM, Resistor Network, Joule heating, Fourier Heat Equation, Semiconductors.**

I. Introduction

RRAM (Resistive Random Access Memory) represents a new type of non-volatile memory that relies on controllable and reversible resistance changes, typically in thin oxide films [4].

RRAMs are often seen as a subclass of so called memristive systems [5]. Term memristor was first postulated by Leon Chua in 1971 [6]. Memristor (Memory resistor), along with the capacitor, the inductor and the resistor, represents the 4th electrical component. It is a passive electronic element that makes a non-linear link of electric charge and magnetic flux. According to mathematical formulation of a memristor, memristors resistance is not constant, but it depends on a current that previously flowed through it. More specifically, the resistance of the memristor depends on the amount and direction of the electric charge.

Typically a RRAM cell has a MIM structure, where M stands for metal electrodes and I stands for a specially selected solid dielectric (i.e. thin substochiometric metal oxide). In normal circumstances, oxide does not conduct a DC current. However, if the oxide is biased to a high enough voltage, it will start to conduct. This phenomenon is called a dieletric breakdown. Phenomenologically, a dielectric breakdown represents a formation of conductive channels (conductive filamets) inside the oxide matrix. Dielectric breakdown is typically seen as a damage to electrical components that makes them faulty. On the contrary, this phenomenon is used in RRAMs where the formation of conductive filaments is controllable and reversable. Filaments are the effect of an agglomeration of oxide defects (typically oxygen vacancies) that ultimatly brige the two electrodes. Conductive filaments can support current flow through the oxide. Electronically, the formation of conductive filament is seen as a sharp decrease of oxide's resistance once the threshold voltage is reached. The process is called electroforming. Resulting resistance state is stable even without a voltage bias and it is typically called low resistance state (LRS). Crucially, it is possible to dissolve the conductive filament by inverting the voltage polarity (bipolar switching mode) or by allowing a higher current flow under a lower voltage bias (unipolar switching mode). This reverts the device into the so called high resistance state (HRS). Two resistance states are used to represent two logical states in nonvolatile memory applications. The potential applications of RRAM technology goes beyond non-volatile memories, more specifically RRAMs have been considered for logics [7] or novel neuromorphic applications [8], [9]. Review of the basic concepts of resistive switching materials can be found in [10], [11].

Many different compounds are used in RRAM devices including metal/semiconductor oxides such as hafnium oxide [12], titanium oxide [13], tantalum oxide [14], silicon oxide [15] and even some organic compounds [16] among the others.

Control of the heat generation is one of the most important factors when operating RRAM devices. We are assuming that the process of filament generation is directly related to Joule's heating. More specifically, Joule's heating impacts the electrical behavior of device and the changes of its resistance states. Considering the projected fabrication density it is very likely that the heating of a single cell affects behavior of a

neighboring cell or surrounding electronics.

II. Experimental Results

Figure 1. shows a unipolar switching obtained from the silicon oxide based RRAM device. Device has MIM structure, where two TiN electrodes sandwich the switching SiOx layer. SiOx layer is substoichiometric. XPS measurements indicate that x is roughly 1.3. More details about the fabrication process can be found elsewhere [17].

Red line in Figure 1. shows a voltage sweep of the pristine device. Sharp conductance increase is observed around 7 V that sets the device into the LRS. A current compliance of 3mA is applied to prevent a hard breakdown and irreversible device damage. This is the electroforming process. To obtain the reset process device is swept without the current compliance. Decrease of the device conductance starts around 2V and ends at around 3V with the resistance value somewhere between that the LRS and pristine state. This is the HRS. Subsequently device can be recovered to LRS at around 3.8 V with the 3 mA current limit applied again. Device can be cycled between LRS and HRS for many times repeatedly.

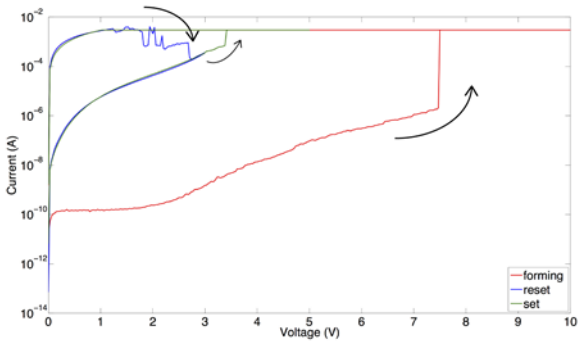

Fig. 1. Unipolar switching obtained from SiOx RRAM device. Red curve shows the electroforming process and the sharp voltage increase around 7V. Current compliance of 3mA is used to prevent a hard breakdown. Blue curve shows the reset process and the green curve shows the subsequent set process.

In order to construct our model of heat generation we use a specific configuration of the oxide defects inside the oxide matrix (Figure 2). Thickness of the modeled oxide is approximately 25nm. Oxide defects are sites that provide a current flow. We use data obtained from the results of the Monte Carlo ionic transport model for resistive switching. This model is based on Random Circuit Breaker Network Model [18] and the hopping of oxygen ions. More details about the model and the results can be found in [19].

A. Description of the algorithm for the simulation

Resistor Network (RN) is used to study and simulate microscopic processes during the resistance change inside the oxide material. RN is shown in Figure 2. This network models the structure of an insulator (metal-oxide). Every node in the network represents an oxygen atom or a defect site (an oxygen vacancy). Equivalent resistance between the adjoining sites can have two values: R1 and R2 (R1>>R2). Resistor has value R2 if it is placed between oxygen vacancies, otherwise it has value R1.

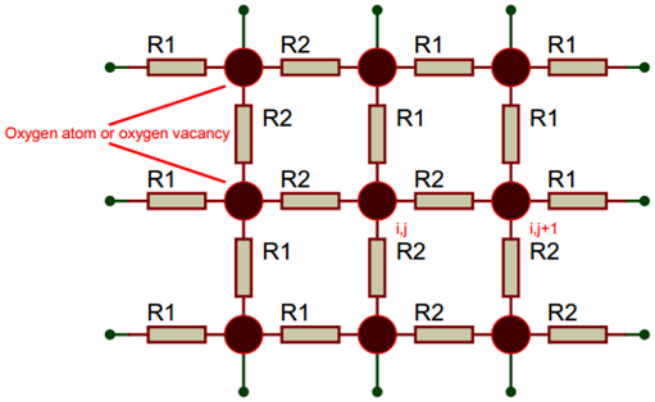

Fig. 2. Ilustration of Resistor Network (after [18]).

B. Modelling the heat generation

Temperature of individual resistors in RN is calculated as follows:

$$T = T_0 + k \cdot I(i,j,k,l) \cdot (V(i,j) - V(k,l)) \tag{1}$$

where:

- $T_0 = 300K$ - initial temperature
- $k = 10^6$ - coefficient of proportionality
- $I(i,j,k,l)$ - current that flows through the branch which is located between the (i,j) node and (k,l) node in Resistor network.
- $V(i,j)$ - voltage potential of (i,j) node in RN.

Furthermore, we use Fourier heat equation to perform simulation of heat flow through the insulator, whereby the equation has the following form:

$$\rho C \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q + h(T_{ext} - T) \tag{2}$$

It describes the heat transfer process for plane and axisymmetric cases, and uses the following parameters:

- Density ρ
- Heat capacity C
- Coefficient of heat conduction k
- Heat source Q
- Convective heat transfer coefficient h
- External temperature T_{ext}

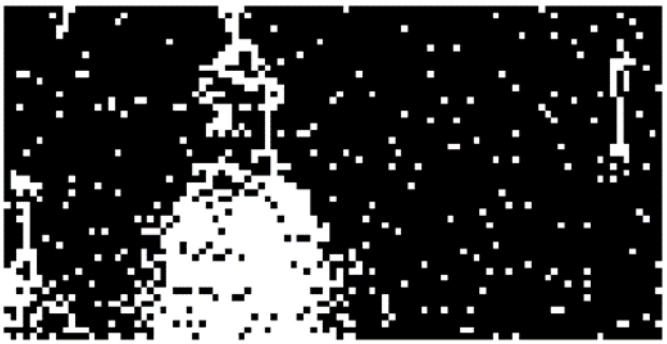

Fig. 3. Oxide configuration in LRS. Data obtained from [16]. White dots represent the defect states that support current flow. Black areas represent the pristine insulating oxide matrix.

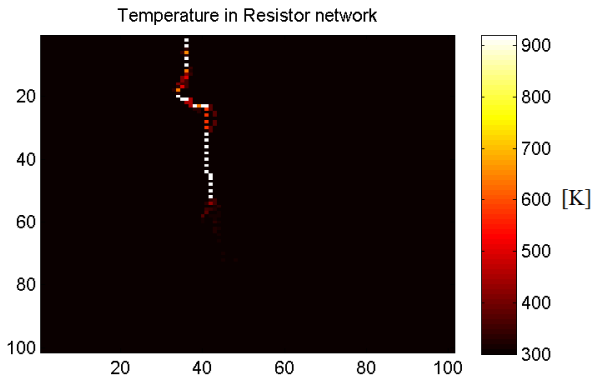

Fig. 4. Temperatures generated form each resistor in Resistor network using Eq1.

Figure 3. shows the LRS obtained from [19]. In this state oxygen defects build a steady path (conductive filament) from the top to the bottom electrode of the RRAM cell that supports a current flow. This current generates a Joule heating.

Figure 4. gives the temperatures of each resistor in RN at around 2V of applied voltage (just before the beginning of the reset process). It can be noticed that the most heated resistors are in the places where the path is thinnest. This is not surprising as the highest current will flow across the resistors connected in series. On the contrary, in areas where path expands, we have a parallel connection of a large number of resistors and therefore the current divides and heating is less. Figures 5 (a-f) shows the results of the heat propagation modelled using the Fourier heat equation (Eq 2) after 10ns, 100ns, 1us, 10us, 100us and 1ms, respectively. Values used for our model are summarised in Table 1.

TABLE I
SILICA - SILICON DIOXIDE (SIO2)

Property	*Minimum Value*	*Maximum Value*	*Units*
Density	2.17	2.65	Mg/m^3
Specific heat	680	730	$J/kg \cdot K$
Thetmal Conductivity	1.3	1.5	$W/m \cdot K$

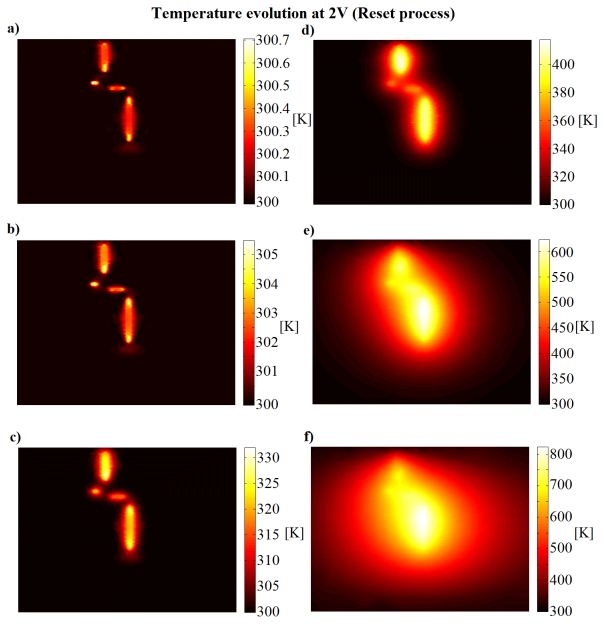

Fig. 5. (a) - (f) shows the results of the heat generation and propagation modelled using the Fourier heat equation (Eq 2) after 10ns, 100ns, 1us, 10us, 100us and 1ms, respectively at 2V of applied voltage.

We also consider the case when the applied voltage is 4V (set process). We do not impose any current compliance and we model the generated heat. Results are shown in Figure 6 (a-d).

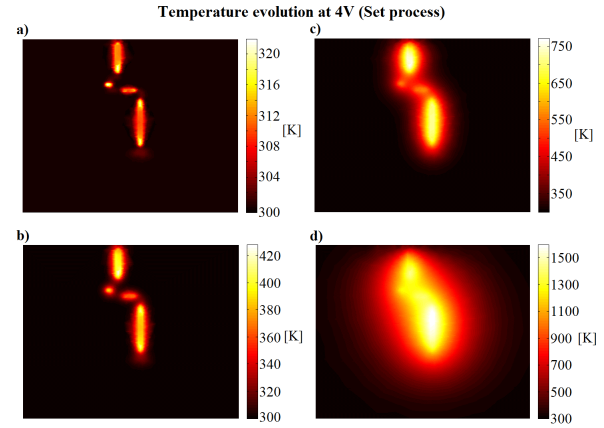

Fig. 6. (a) - (d) shows the results of the heat generation and propagation modelled using the Fourier heat equation (Eq 2) after 100ns, 1us, 10us and 100us , respectively at 4V of applied voltage.

It is apparent that generated temperature reaches values up to 900K in matter of a few hunderds microseconds in the case of the reset process. In the case of the set process, temperature could reach values as high as 1600K after only 100us. At such temperatures the generation of oxide defects is rapidly accelerated and the whole process could lead to formation of the thicker and stroger conductive filaments and ultimatelly to oxide melting. Permanent oxide damage prevents the recovery to HRS.

Consequently, the timing of the applied voltage is a critical parameter that needs to be precisely controlled. External circuitry, that imposes the current compliance, needs to have quick respond times, ideally in microsecond region, in order to prevent the rapid temperature increase. Current overshoots beyond the current compliance level, as the effect of parasitic capacitances, also needs to be taken into account.

III. Conclusion

Extensive heating leads to a degradation of oxide insulting properties via self-accelerated generation of oxide defects. This is typically followed by the increase of the leakage currents after which a breakdown of gate oxide represents a failure of an electronic component. On the other hand, a precise control of the heat generation is essential to achieve a more controllable breakdown (sometimes called a soft-breakdown). This yields an opportunity to reversibly switch the resistance of thin oxide layers. RRAM technology, based on resistance switching of various oxide films, provides a promising route towards novel non-volatile memory devices, unconventional logic elements or neuromorphic systems. In this paper we modeled the Joule heating generation by adopting the resistor network model and we studied the heat propagation using the Fourier heat equation.

Our simulation highlights the importance of regulation of both the current levels and the operational times in order to prevent irreversible oxide damage due to the extensive Joule heating.

Our simulation can provide a useful tool to study the time evolution of the heat generation in thin oxides. This is an essential part in the formulation of the phenomenological models that examine the structural changes inside oxide materials as a result of applied electric bias. We envision that this study can be equally applicable on studies of gate oxides in FET transistors and resistance switching layers in case of RRAMs.

References

[1] Mehonic, Adnan, et al. "Resistive switching in silicon suboxide films." *Journal of Applied Physics* 111.7 (2012): 074507.

[2] Torrezan, Antonio C., et al. "Sub-nanosecond switching of a tantalum oxide memristor." *Nanotechnology* 22.48 (2011): 485203.

[3] Govoreanu, B., et al. "10 10nm 2 Hf/HfO x crossbar resistive RAM with excellent performance, reliability and low-energy operation." *Electron Devices Meeting (IEDM), 2011 IEEE International*. IEEE, 2011.

[4] Waser, Rainer, and Masakazu Aono. "Nanoionics-based resistive switching memories." *Nature materials* 6.11 (2007): 833-840.

[5] Strukov, Dmitri B., et al. "The missing memristor found." *nature* 453.7191 (2008): 80-83.

[6] L. O. Chua, IEEE Trans. Circuit Theory CT18(5), 507519 (1971).

[7] Borghetti, Julien, et al. "'Memristive' switches enable statefullogic operations via material implication." *Nature* 464.7290 (2010): 873-876.

[8] Jo, Sung Hyun, et al. "Nanoscale memristor device as synapse in neuromorphic systems." *Nano letters* 10.4 (2010): 1297-1301.

[9] Mehonic, Adnan, and Anthony J. Kenyon. "Emulating the electrical activity of the neuron using a silicon oxide RRAM cell." *Frontiers in neuroscience* 10 (2016).

[10] Ielmini, Daniele, and Rainer Waser, eds. *Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications*. John Wiley & Sons, 2015.

[11] Mehonic, A., and A. J. Kenyon. "Resistive Switching in Oxides." *Defects at Oxide Surfaces*. Springer International Publishing, 2015. 401-428.

[12] Kim, Yong-Mu, and Jang-Sik Lee. "Reproducible resistance switching characteristics of hafnium oxide-based nonvolatile memory devices." *Journal of Applied Physics* 104.11 (2008): 114115.

[13] Jeong, Hu Young, et al. "Microscopic origin of bipolar resistive switching of nanoscale titanium oxide thin films." *Applied Physics Letters* 95.16 (2009): 162108.

[14] Lee, Myoung-Jae, et al. "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5 x/TaO2 x bilayer structures." *Nature materials* 10.8 (2011): 625-630.

[15] Mehonic, Adnan, et al. "Electrically tailored resistance switching in silicon oxide." *Nanotechnology* 23.45 (2012): 455201.

[16] Verbakel, Frank, et al. "Reproducible resistive switching in nonvolatile organic memories." *Applied Physics Letters* 91.19 (2007): 192103.

[17] Mehonic, Adnan, et al. "Structural changes and conductance thresholds in metal-free intrinsic SiOx resistive random access memory." *Journal of Applied Physics* 117.12 (2015): 124505.

[18] Chae, Seung Chul, et al. "Random circuit breaker network model for unipolar resistance switching." *Advanced Materials* 20.6 (2008): 1154-1159.

[19] Mehonic, Adnan. *Resistive Switching in Silicon-rich Silicon Oxide* (Doctoral dissertation (2014), UCL (University College London)).