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Intrinsic resistance switching in amorphous silicon oxide for high performance SiO_x ReRAM devices

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ABSTRACT

In this paper, we present a study of intrinsic bipolar resistance switching in metal-oxide-metal silicon oxide ReRAM devices. Devices exhibit low electroforming voltages (typically −2.6 V), low switching voltages (±1 V for setting and resetting), excellent endurance of >107 switching cycles, good state retention (at room temperature and after 1 h at 260 °C), and narrow distributions of switching voltages and resistance states. We analyse the microstructure of amorphous silicon oxide films and postulate that columnar growth, which results from sputter-deposition of the oxide on rough surfaces, enhances resistance switching behavior.

1. Introduction

Redox-based resistive RAM (ReRAM) [1] is viewed as one of the most promising candidates for the next-generation of non-volatile memories owing to its fast switching times, low power consumption, non-volatility and CMOS-compatibility [2,3]. Other applications include power-efficient systems for neuromorphic engineering [4,5] and logic [6].

Resistance switching in silicon oxide-based ReRAM devices can result from a number of very different processes. We may divide these into those that are intrinsic properties of the oxide (e.g. valence change ReRAM) and those that require the indiffusion of conductive species such as metal ions – we may call these extrinsic processes (e.g. electrochemical metallization ReRAM) [7]. The body of the literature on intrinsic resistance switching in silicon oxide is rather limited – a situation that arises from the conventional belief that sub-hard breakdown silicon oxide is an inert electrical insulator. Some literature has even suggested that resistance switching in metal-free silicon oxide is not possible [8].

However, intrinsic switching has indeed been reported, and it generally can be classified into that occurring inside the oxide bulk ("bulk switching"), which depends critically on oxide microstructure and the availability of oxygen [9–11], and switching at internal pores and edges ("surface switching") of the oxide, which is only possible in vacuum or in devices that have been hermetically sealed [12,13].

In this study, we demonstrate excellent intrinsic bulk switching properties for SiO_x (x ~ 1.6) ReRAM devices. More specifically, our devices exhibit low electroforming voltages (typically −2.6 V), low switching voltages (±1 V), high uniformity in switching voltages and resistance states, high endurance (>10^7 cycles), and good state retention (>10^4 s) at room temperature, and after 1 h at 260 °C.

We postulate that the roughness of the bottom oxide-electrode interface affects the microstructure of the oxide and enhances the columnar growth, which results in favourable switching properties.

2. Fabrication and methods

Metal-oxide-metal ReRAM devices were fabricated on silicon substrates with a top layer of 4 μm of thermal oxide (SiO_2). 280 nm of Mo was deposited onto the SiO_2 layer by sputtering. This served as the bottom electrode.

The switching oxide was deposited by reactive magnetron sputtering (Kurt Lesker PVD75), in which an undoped silicon target was used to sputter the SiO_x thin film onto the substrate in an oxygen-rich environment. The sputtering conditions were: RF power 110 W, Ar:O_2 ratio was 1:1 and Capman pressure was 3 mTorr. In total, 35 nm of SiO_x was deposited onto the bottom Mo layer. After this was deposited, a thin (3 nm) adhesion layer of Ti followed by 115 nm layer of Au was deposited by electron beam evaporation to serve as top electrodes. A shadow mask was used to define the electrode

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areas with individual electrode size varying from 200 μm × 200 μm to 800 μm × 800 μm.

Electrical characterization was performed using a Keithley 4200 semiconductor characterization system (the voltage sweeps were obtained using source measuring units, and the endurance testing using a pulse measuring unit). An ArC One characterization board was used to conduct the retention measurements. All electrical characterization was performed at room temperature, unless otherwise stated.

An FEI Helios focused ion beam (FIB) was used to prepare TEM cross-sections, and STEM imaging was carried out at 80 keV using an FEI Titan M/STEM. EELS analysis was performed using a Gatan Imaging Filter (GIF) and a collection semi-angle of 30 mrad. XPS measurements were performed using a Thermo Scientific K-Alpha with a monochromated Al source at 10^{-8} Torr.

3. Results and discussion

Fig. 1 shows the switching performance obtained from typical SiO_x ReRAM devices (electrode size 400 μm × 400 μm). Firstly, we swept the voltage bias to electroform the oxide (i.e. to transition from the pristine to the low resistance states) with 1 mA of current compliance (CC). We then proceeded to cyclically reset (transition from the low resistance state (LRS) to the high resistance state (HRS)) and set the device (transition from the HRS to the LRS). The device electroforms at around −2.6 V and, significantly, it electroforms only in the negative sweep (i.e. a negative potential applied to the top electrode), which excludes the field-induced migration of Ti cations from the top electrode - an extrinsic (ECM) mechanism. Post electroforming, the device shows bipolar switching with low switching voltages; from −0.9 V to −1.1 V to set

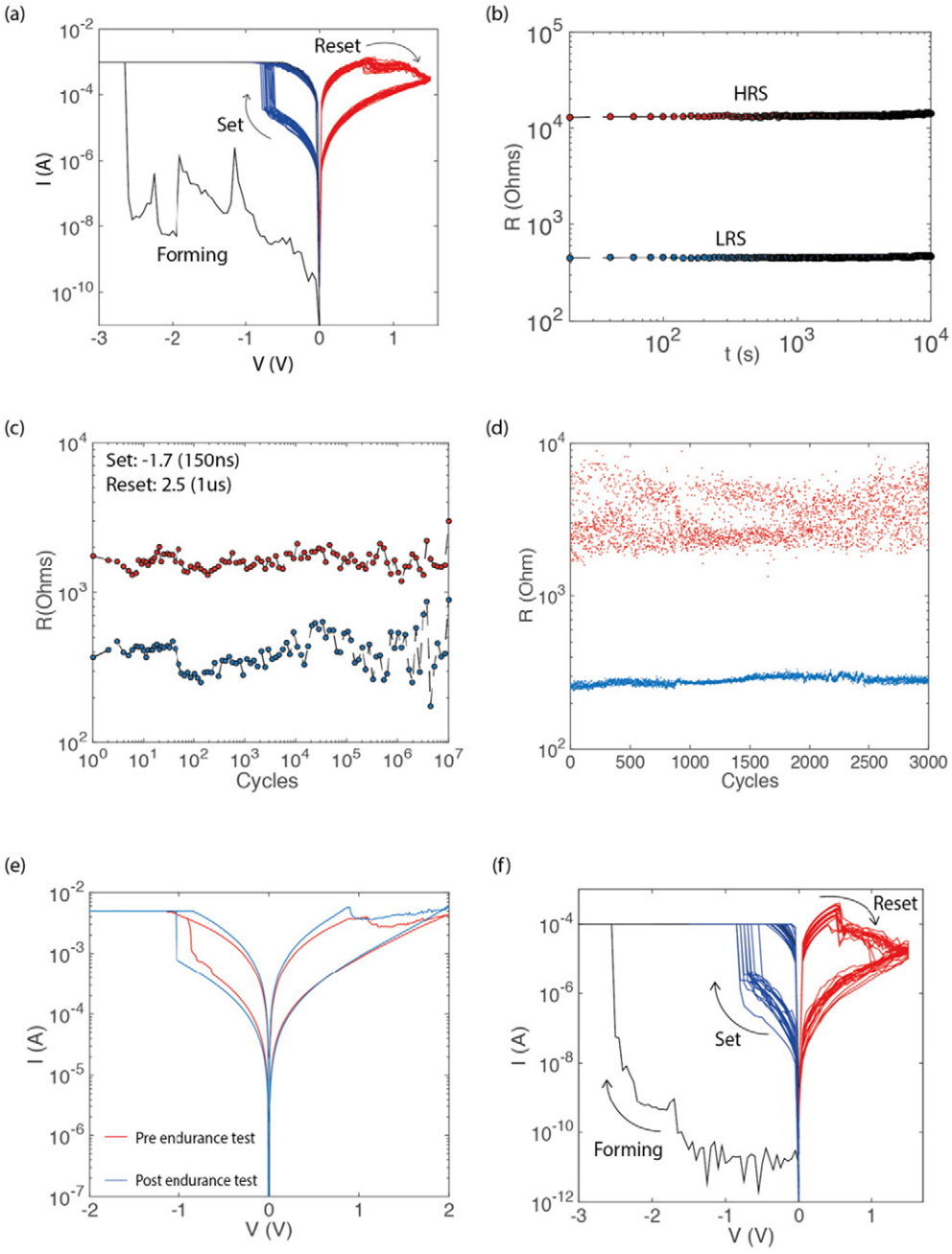

Fig. 1. Electrical characterization of silicon oxide-based ReRAM devices. (a) Device electroforms at around −2.6 V, sets at around −0.9 V and resets at around 1.3 V (with a CC of 1 mA). (b) Device shows no degradation of either resistance states during the 10^4 s retention test at room temperature. (c) Device shows endurance for 10^7 cycles (10 samples per decade). (d) 3000 switching cycles, recording every single cycle. (e) IV switching curves prior and post- endurance test, confirming the device functionality post 10^7 cycles. (f) IV switching curves with a lower CC of 100 μA. The device sets around −0.65 V and resets around 1.1 V.

and from 0.85 V to 1.3 V to reset (Fig. 1a). We cycle the device in this way to achieve a good compromise between low switching voltages, high cycling endurance and sufficient contrast between the LRS and the HRS. A complete reset process can be obtained by sweeping the devices to 2 V, in which case the contrast between the two resistance states is much larger (Fig. S1 in Supplementary information). The device does not electroform in the positive sweep. (Fig. S2 in Supplementary information). This is consistent with the theory of valance change ReRAMs, in which, to electroform the device, the negative bias should be applied to the electrode with the higher work function (lower oxygen affinity) – which in our case is the Au electrode.

These voltage values are lower than those previously reported for intrinsic SiO_x ReRAM devices – such as 5 V/1.2 V/−1.5 V [14]; −5 V/−3 V/3.5 V [11] and 20 V/3 V/8 V [12,13] for the electroforming/set/reset voltages, respectively.

Fig. 1b shows the retention test for 10^4 s at room temperature. No degradation of either LRS or HRS is observed. To further analyse device retention at temperatures required for solder reflow, we heated up the devices to 260 °C for 1 h and tested the resistance states after the device had cooled down to room temperature (approximately 15 min following the heating). The device was set to the LRS with a current compliance of 1 mA, and the HRS was achieved by voltage sweep to 2 V and consequent complete reset process. The resistances, before the device heating, were 681 Ω for the LRS and 31.6 MΩ for the HRS. After heating the device, the HRS change was negligible, while the LRS resistance was 5.4 kΩ. Interestingly, the opposite trend is observed for SiO_x electrochemical metallization cell RRAM devices [15]: the LRS state is unchanged while the HRS resistance changes by approximately an order of magnitude.

Fig. 1c shows the endurance test for 10^7 cycles, where the resistance states are measured using a logarithmic spacing. Fig. 1d shows 3000 cycles recording every cycle. For the endurance test the following pulses were used: −1.7 V, 150 ns to set, 2.5 V, 1 μs to reset and 0.1 V, 200 ns to read. Small fluctuations of resistance states at the end of the endurance test are the result of a slight increase of the reset current combined with the internal current limit of 10 mA for the Keithley PMU. IV curves (Fig. 1e) confirm the functionality of the device after 10^7 cycles, and the slight increase of the reset current. The endurance of 10^7 cycles without device failure is to the authors' knowledge the highest endurance reported for intrinsic SiO_x ReRAM devices. Note that the device can also operate with a lower current compliance (100 μA or lower). In this case, the reset currents are typically much lower, while the switching voltages remain comparable to those when the high current compliance is used. This is shown in Fig. 1f. However, we note that the speed of a DC current limit (SMU Keithley 4200) is relatively slow (in the ~100 μs range) and significant current overshoots are expected during the forming process, as well as during the set process. Consequently, this effect will introduce variability during the switching, which is most pronounces for lower operational currents due to slower current integration and sensing. Following the forming voltage, the first reset process typically exhibits a significantly higher reset current than those of the following resets. This is a direct effect of the current overshoot. We, therefore, include an analysis of the uniformity of the switching voltages and of the resistance states of our devices, which show good uniformity in spite of the limitations of the measurement apparatus.

For the device electroformed with a current compliance of 1 mA, the cumulative probability plots of switching voltages are shown in Fig. 2a and b. The device shows a tight distribution of switching voltages (calculated from the 110 I/V sweeps) – more specifically a spread of 0.27 V for the set voltage and a spread of 0.21 V for the reset voltages, calculated from the 10% to 90% cumulative probabilities. The relative standard deviation (σ/R) for the LRS is 0.43 and for the HRS is 0.35. For the device electroformed with a current compliance of 100 μA, the cumulative probability plots are shown in Fig. 2c and d (calculated from the 50 I/V sweeps). The spread of the set voltage and the reset voltages is 0.2 V and 0.1 V, respectively, and the relative standard deviations are 0.53 for the LRS and 1.03 for the HRS. These are slightly higher than those reported for the SiO_x electrochemical metallization cell RRAM devices [15], but it should be noted that in this study the authors use a 1T1R configuration that mitigates the problem of current overshoots.

Additionally, we analysed the uniformity of the forming voltages over 20 separate devices. Pristine devices were swept to a maximum voltage of −6 V. Out of 20 devices, 18 devices successfully electroformed (90% yield). The spread for the electroforming voltages of 2 V (from −1.5 V to −3.5 V) is calculated from approximately 10% to 90% probabilities (Fig. 2c). We believe this can be further improved by engineering the roughness of the bottom interface between the oxide layer and the electrode. This, together with a detailed study of the effect of the interface roughness, will be the subject of our further study.

Fig. 3 shows normalised O1s and Si2p XPS spectra (the latter normalised to the O1s signal). The estimated stoichiometry of the SiO_x film is around $x = 1.6$. The position of the Si2p peak, around 102.8 eV, corresponds to the Si^{3+} oxidation state of silicon. It has been suggested that this configuration introduces intrinsic interfaces into the amorphous SiO_x matrix, making it rich in dangling bond defects [16].

To understand the excellent switching properties – more specifically the low electroforming/switching voltages and the enhanced endurance – we used scanning TEM (STEM) to study the microstructure of the oxide layers.

Fig. 4a shows a cross-sectional bright field STEM images of the device. Firstly, we observe that the interface between the oxide and the electrodes shows significant roughness (on order of 5 nm) and speculate that this has a critical influence on switching properties.

It is known that sputtered materials that are deposited at lower temperatures exhibit columnar growth [17]. Additionally, the rougher electrode surface might promote atomic shadowing during oxide deposition and result in enhanced columnar growth. This is apparent in Fig. 4a, where columnar growth is clearly observed (indicated by the red arrows) in the form of bright vertical streaks. These streaks have an approximate spacing of 20 nm, and correspond to regions of low intensity in the High Angle Annular Dark Field (HAADF) image in Fig. 4b. Regions of low intensity in the HAADF image correspond to regions of low atomic number [18], and suggest the presence low-density intercolumnar boundaries.

This is consistent with our previous study in which the tops of these columns are observed using scanning tunneling microscopy with enhanced conductivity around the edges of the columns [9,19]. We also noted earlier, from our XPS results, that the configuration of the silicon atoms in our sample suggests the presence of defect-rich intrinsic interfaces [10]. We therefore speculate that the edges of the columns provide favourable sites for oxygen movement and filament formation due to their defect-rich nature. Consequently, enhanced columnar growth will promote easier electroforming as well as lower switching voltages. Another important effect of the interface roughness is the enhancement of the local electric field. This can lead to increased electron injection and hence increased rate of creation of Frenkel pairs, consisting of oxygen vacancies and oxygen interstitial ions, with oxygen interstitial ions characterised by low migration barriers of around 0.2 eV [20,21].

We see no evidence of significant Ti diffusion into SiO_x layer, as shown in the bright field STEM image in Fig. 5a and the EELS Ti elemental map in Fig. 5b.

4. Summary and conclusion

We presented the electrical characterization of an intrinsic SiO_x ReRAM devices and analysed the microstructure of the oxide layer. Our results suggest that improved switching properties are a consequence of a rougher oxide-metal interface. We believe there are two possible triggers that can act simultaneously. Firstly, rougher oxide-

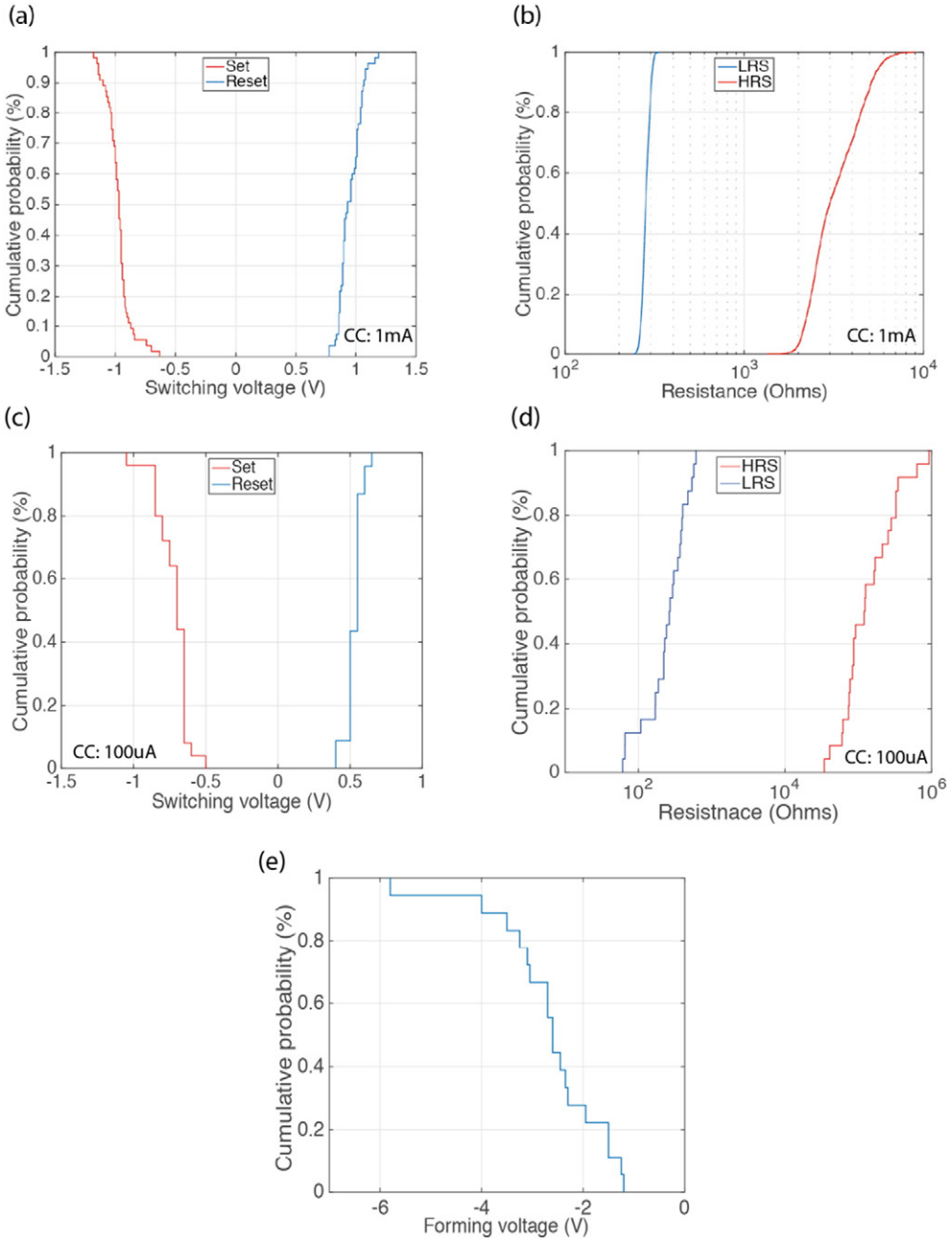

Fig. 2. Cumulative distributions of (a) the set and the reset voltages (with a CC of 1 mA) (b) the low resistance states and the high resistance states (with a CC of 1 mA) (c) the set and the reset voltages (with a CC of 100 μA) (d) the low resistance states and the high resistance states (with a CC of 100 μA) (e) the forming voltages for 20 separate devices.

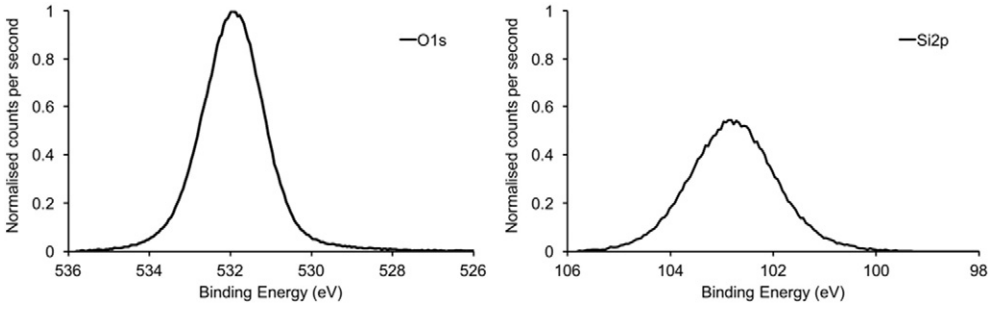

Fig. 3. O1s (left) and Si2p (right) normalised XPS spectra (normalised to the O1s signal) of the SiO_x film.

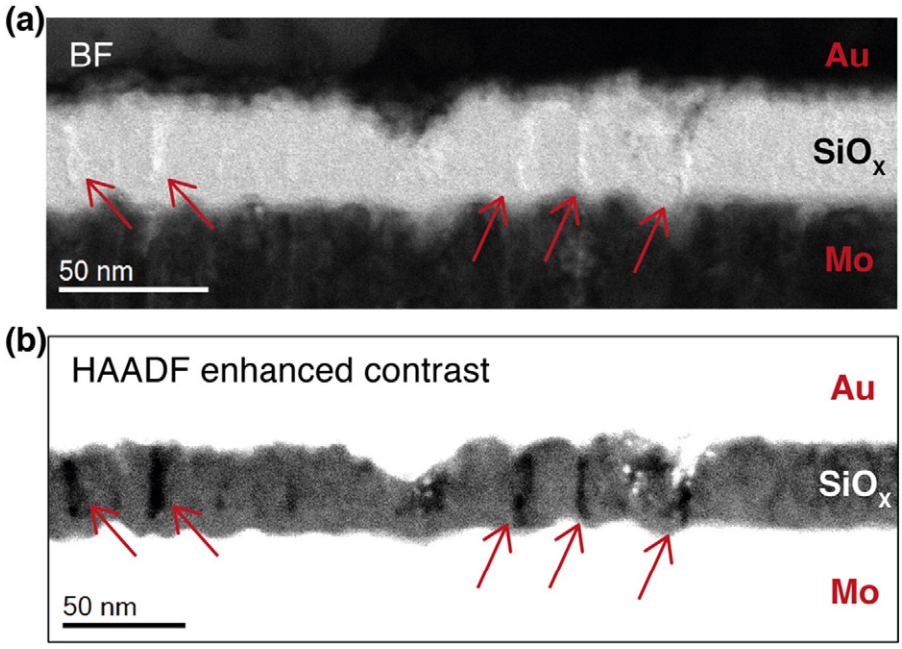

Fig. 4. (a) Bright field STEM and (b) Intensity-clipped HAADF images of the same device, showing columnar oxide growth. The red arrows indicate the columnar growth of the oxide film.

electrode interface causes atomic shadowing during deposition that promotes columnar growth. The edges of the columns provide defect-rich sites where vacancy formation and oxygen ion mobility can be enhanced. Secondly, as electron injection is believed to be the mechanism for the generation of Frenkel defects, the enhancement of the local electric field due to the rough interface can lead to more electrons being injected. The results provide a route to further optimisation of silicon oxide-based ReRAM devices.

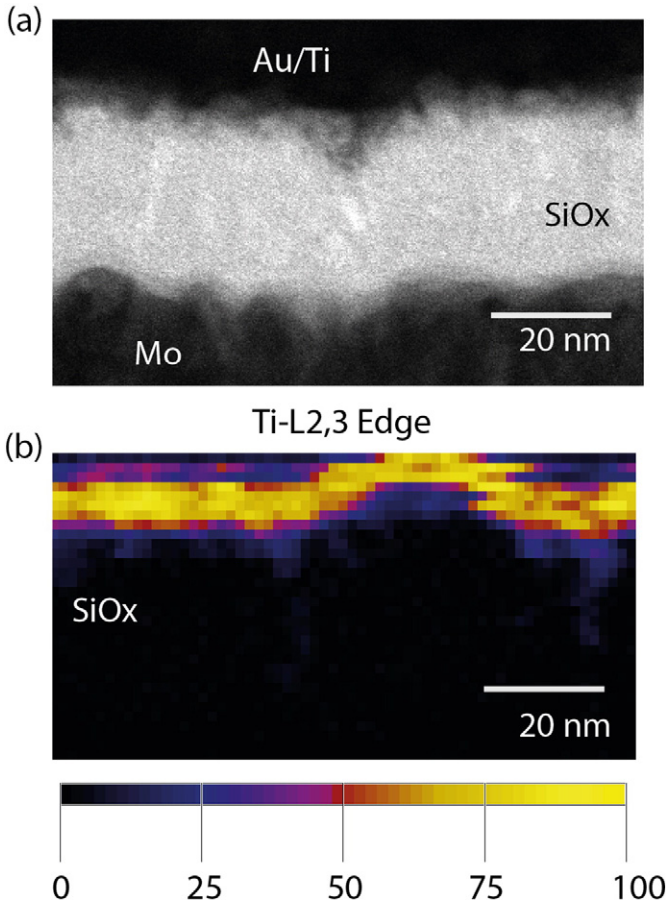

Fig. 5. (a) Bright field STEM and (b) EELS elemental map (Ti-L2,3 edge).

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Appendix A. Supplementary data

Supplementary data to this article can be found online at http://dx.doi.org/10.1016/j.mee.2017.04.033.

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