Compact Pixel Architecture for CMOS Lateral Flow Immunoassay Readout Systems

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***Abstract*—A novel pixel architecture for CMOS image sensors is presented. It uses only one amplifier for both integration of the photocurrent and in-pixel noise cancelation, thus minimizing power consumption. The circuit is specifically designed to be used in readout systems for lateral flow immunoassays. In addition a switching technique is introduced enabling the use of column correlated double sampling technique in capacitive transimpedance amplifier pixel architectures without the use of any memory cells. As a result the reset noise which is crucial in these architectures can be suppressed. The circuit has been designed in a 0.35-µm CMOS technology and simulations are presented to show its performance.**

Keywords—Capacitive transimpedance amplifier; CMOS image sensors; correleted double sampling;

I. INTRODUCTION

Infectious diseases especially in developing countries are among the top causes of death. The lack of medical staff and properly equipped health care centers only worsen the situation. The development of point-of-care (POC) diagnostic tests to monitor and detect infectious diseases in early stages is therefore extremely important. Since many proteins are biomarkers of diseases, diagnostic tests for the detection of proteins are in high demand [1].

Lateral flow immunoassays (LFIAs) are very popular and well established biosensors for the detection of proteins. Their many advantages such as lightweight, low cost, high sensitivity and specificity, good stability and the requirements of small volumes of samples makes them ideal for POC diagnostics especially in developing countries. LFIAs are preprocessed strips with immobilized labels. Fig. 1(a) shows a LFIA and an example of the reaction that takes place when influenza A nucleoprotein is detected. When the sample is applied at the end of the strip it moves due to capillary action along its entire length. If the sample contains the analyte of interest it will react with the immobilized labels of the strip generating two color lines which are visible to the naked eye. The intensity of these color lines is related to the concentration of the analyte present in the sample [2]. For quantitative analysis an external electronic reader is needed to interface with the LFIAs and measure the intensity of the color lines. The reader must have low power consumption in order to perform thousands of measurements from a single battery, high sensitivity, low noise and detection capabilities under low light illumination since detection in very low concentrations results in low intensity color lines.

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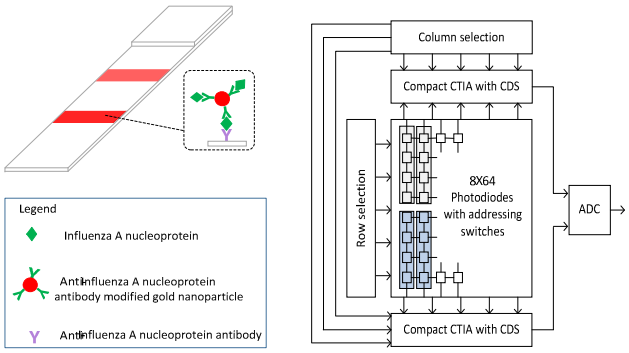

(a) (b)

Fig. 1. (a) LFIA during the detection process of Influenza A nucleoprotein and (b) CIS architecture specifically design to be used as a readout for LFIAs.

Current electronic readers are usually based on either mobile phone cameras or off-the-shelf components [3]. However, both of these solutions result in the development of readout systems that are not optimized specifically for this application. Consequently the various readers have high power consumption due to excess use of pixels in the CMOS image sensors (CISs), low noise performance and poor low-light operation.

In this paper a CIS specifically designed to be used in readout systems for LFIAs is proposed for the first time. A novel pixel architecture (Fig. 1(b)) is presented that achieves low-light illumination, low power consumption and low noise.

II. CONVENTIONAL CIS PIXEL ARCHITECTURES

Commonly used pixel topologies are the 3T-APS (3-transistor active pixel sensor), 4T-APS (4-transistor active pixel sensor) and CTIA (capacitive transimpedance amplifier). The 3T-APS topology is the simplest topology of the three and has a high fill factor. However, due to the fact that the photocurrent is integrated on the capacitance of the photodiode it has low sensitivity. On the other hand in the 4T-APS topology the photocurrent is integrated on a small floating drain capacitor and therefore high sensitivity can be achieved. Furthermore this topology benefits from the use of charge transfer gates since it decouples the read and reset operations allowing the use of the correlated double sampling (CDS) technique. CDS is a technique that is usually used in CIS for the attenuation of reset noise, offset, pixel array fixed pattern noise (FPN) and flicker noise. However, the 4T-APS has reduced performance in low-light illumination producing delaying images due to slow

charge transfer from the photodiode to the floating drain capacitor. Even though this can be overcome with various techniques, it usually results in affecting the sensitivity performance [4]. On the other hand the CTIA topology has high sensitivity that depends on a feedback capacitor which can be very small. However, both 3T-APS and CTIA architectures have their read and reset operations coupled to the integration period and therefore the CDS cannot be performed unless in-pixel memory cells are used.

In conventional CTIA architecture (Fig. 2(a)), during the reset period, the reset transistor S_{rst} is closed and the input and output of the amplifier are connected. The reverse bias across the photodiode is defined through the virtual ground potential of the amplifier. During the integration period the reset switch opens and the input and output of the amplifier are connected through the feedback capacitor (C_{fb}) [5]. The photocurrent (I_{ph}) is integrated on C_{fb} as

$$V_{CTIA} = \frac{1}{C_{fb}} \int I_{ph} dt \qquad (1)$$

CIS suffers from multiple noise sources like fixed-pattern noise (FPN), shot noise, dark current noise, reset noise and readout noise, which can affect its performance especially in low-light illumination [6], [7]. The FPN is due to mismatches of active transistors and can result in an output variation from pixel to pixel [8], [9], while the reset noise or *kT/C* noise is from the random fluctuation at the integration node of carriers [6]. CDS is commonly used for the attenuation of FPN and reset noise. It is usually implemented at the end of each column in an array of pixels. This technique operates by calculating the difference between the signal before (reset signal) and after integration from the same pixel in the same frame. In 3T-APS and CTIA architectures in pixel memory cells are required in order to realize this technique [10]. However, the use of in pixel memory cells can result in reduction of fill factor and signal loss. Instead a modification of CDS, the delta reset sampling (DRS) technique, can be used [11]. This calculates the difference between the integrated signal of the first frame and the reset signal of the next frame. Therefore the DRS can only suppress the FPN and flicker noise while it doubles the reset noise. This is due to the fact that the two subtracted signals belong to two different frames [9]. However, in the CTIA topology the reset noise is dominant due to the small size of the C_{fb} [12]. Consequently the suppression of the reset noise is very important.

In this paper two different architectures that implement the CDS technique with CTIA topology are proposed. The first architecture is based on conventional CTIA and sample and hold circuits. However, here it is shown that an alternative switching pattern allows the implementation of CDS in CTIA without the use of any memory cells. The CDS circuit can be placed at the end of each column in a rolling shutter CIS. Therefore the pixel's reset noise can be suppressed, while the signal is not affected by loss due to memory cells.

Next a novel pixel architecture that integrates in-pixel CTIA with CDS in a reconfigurable manner is proposed, using only one amplifier and one memory cell. This topology is specifically advantageous in the targeted application since it features very low power consumption. Fill factor improvement is achieved with the use of a sharing technique. This can be implemented so that four photodiodes can share the same processing circuit. Fig. 1(b) shows the sharing technique, where 4 pixels are grouped together.

III. Pixel Design And Results

A. CTIA with CDS in smart switching configuration

The first proposed topology (Fig. 2(a)), is implemented using CTIA with a column parallel switched-capacitor difference circuit. Even though this implementation seems similar to existing topologies it has an alternative switching configuration as shown in Fig. 2(b), which enables the use of the CDS technique in CTIA architectures without employing memory cells. Consequently the advantages of the use of the CDS technique over the DRS can be exploited even in a CTIA topology.

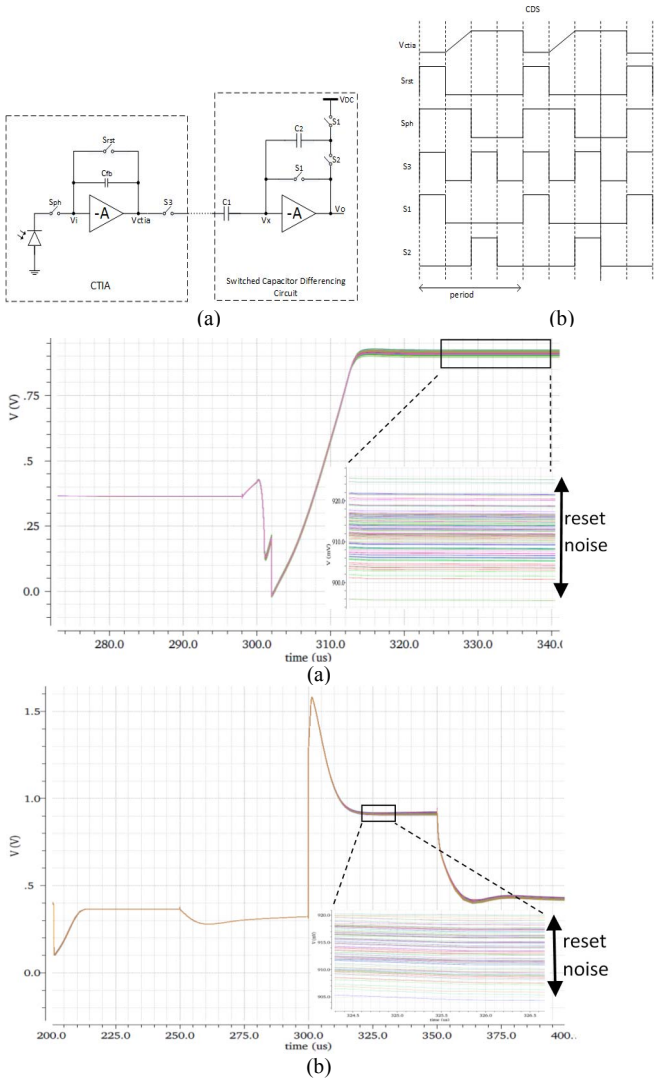

Fig. 3. (a) Transient noise analysis of CTIA with conventional CDS switching pattern and (b) transient noise analysis of CTIA with proposed switching pattern.

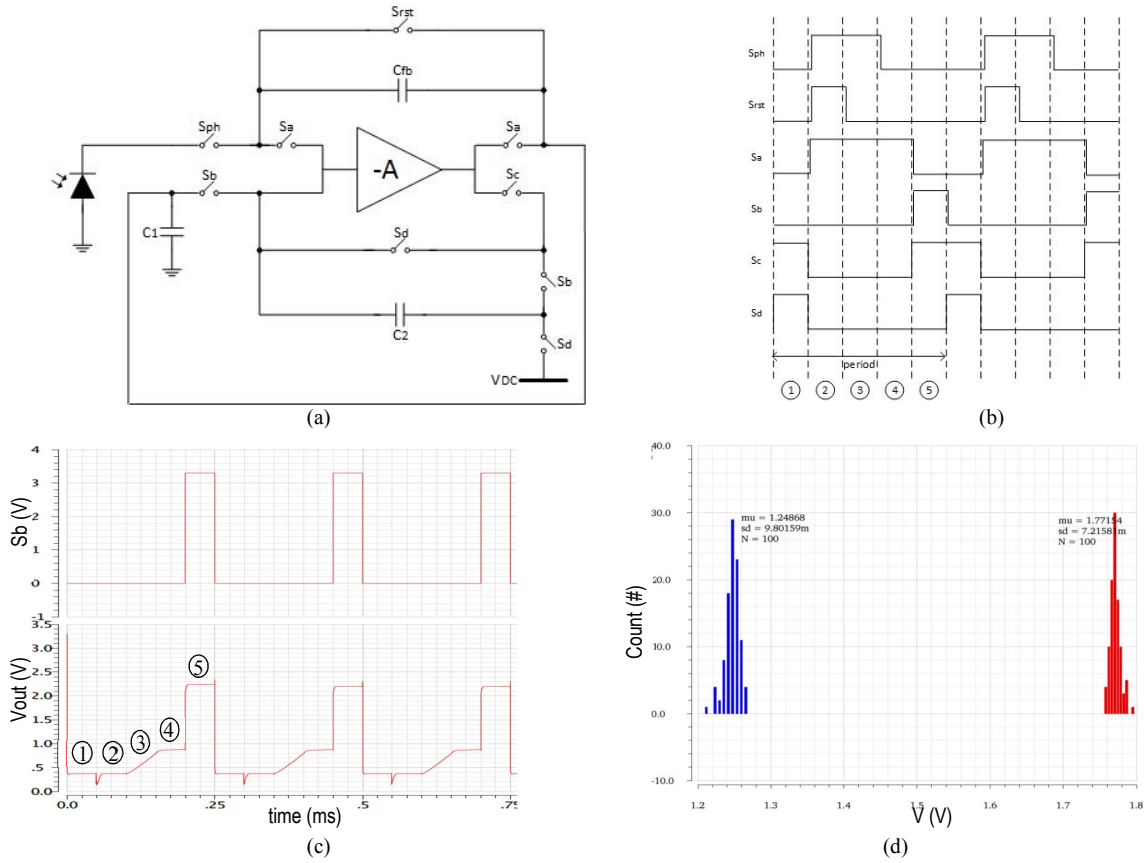

Fig. 4. (a) Novel pixel topology, that performes CTIA and CDS using only one amplifier. (b) Timing diagram for two frames. The circle number indicates the 5 different phases that are performed during one frame. (c) Simulated transient voltage at the output of the proposed topology. The circle numbers shows the output variation during the 5 phases that are required in order to complete 1 frame operation. (c) with blue is indicating the output distribution at phase 4 (after the completion of integration) and with red the output distribution at phase 5 (after the completion of CDS).

The operation of the CDS system is divided into two phases [13]. In the first phase the reset signal is sampled into the capacitor C_1 while the C_2 capacitor is reset.

$$Q_{rst} = (V_{rst} - V_x)C_1 - (V_x - V_{DC})C_2 \quad (2)$$

In the second phase the integrated signal is sampled onto the C_1 capacitor. Hence the difference of the two charges is transferred to C_2:

$$Q_{int} = (V_{int} - V_x)C_1 - (V_x - V_o)C_2 \quad (3)$$

Assuming that C_1=C_2, and Q_{rst}=Q_{sig}

$$V_o = V_{rst} - V_{sig} + V_{DC} \quad (4)$$

Therefore the output signal of the CDS stage is the integrated signal minus the reset signal plus an offset dc voltage. In this case the offset voltage was chosen to be 2.7 V, which is the highest output voltage expected in the amplifier. In this way any negative output values regardless of the photocurrent level are avoided.

The use of the proposed switching technique rather than the conventional allows the subtraction of the reset signal from the integrated signal of the same frame and consequently the reset noise is suppressed. In order to illustrate the suppression of reset noise, the architecture in Fig. 2(a) was realized twice. The first time was implemented with the conventional switching pattern that performs DRS technique and the second time with the proposed switching pattern, Fig.2 (b). The simulation results of 100 transient noise analyses at the output of the two CTIAs architectures are shown in Fig. 3. The output voltage variation of the DRS approach is between 896mV to 926mV, while the output voltage variation of the proposed switching pattern is between 905mV to 920mV. Which shows the reduction of reset noise distribution at the output of the proposed switching pattern architecture.

B. Novel in-pixel CTIA with CDS

A new compact in-pixel CTIA with CDS architecture is also proposed. It is realized by sharing one amplifier between the different phases, reducing power consumption. One capacitor (C_1) is used as a memory cell (Fig. 4(a)). Extra switches enable the appropriate charge transfers in each phase. The size of capacitors C_1 and C_2 are equal. The principle of operation of this topology is similar to that in Fig. 2 and is divided into five phases according to the switching pattern in Fig. 4(b). First C_2 is reset. Second S_{ph} and S_{rst} are closed setting the reverse bias across the photodiode. The reset charges are transferred and saved onto C_1. Third the S_{rst} opens allowing the photocurrent to integrate onto C_{fb}. Fourth the S_{ph} opens keeping the output voltage of the

amplifier constant. In this phase the integrated signal is sampled onto C_1, and fifth the difference of the two charges is transferred to C_2. The transient output voltage of this topology is shown in Fig. 4(c). The circle numbers represent the five phases of operation. At the fifth phase the output obtained satisfies (4). Since both the integration and the reset signal which are subtracted belong to the same frame, the reset noise is removed. Even though there is additional sampling noise due to C_1 (5), this can be smaller compared to the reset noise, because this capacitor can be much larger than C_{fb}.

$$\overline{U_{n1}^2} = \frac{kT}{C_1} \tag{5}$$

For C_1=100 fF, $\overline{U_{nc1}}$ is 0.2 mV_{rms}, which is three times smaller than the reset noise: $\overline{U_{ncfb}}$ is 0.64 mV_{rms} for C_{fb}=10 fF.

Monte Carlo analysis of the structure in Fig. 4(a), was performed in order to demonstrate the reduction of FPN, which is related to mismatches and process imperfections. The results are shown in Fig. 4(d), where pixels output distribution after the subtraction of reset signal from the integrated signal (phase 5) is reduced compared to the distribution before the subtraction (phase 4).

The proposed CIS will be used as a readout system for LFIAs. It has an 8×64 pixel array. Every four consecutive photodiodes of the same column share the same processing circuit. The proposed structure in Fig. 4(a), is placed in two rows before and after the pixels array, see Fig. 1(b) and therefore it does not affect the pixels fill factor. The processing circuits is chosen to be shared between 4 photodiodes, to avoid the charge signal from the photodiodes output being affected by disturbances in a long column line [14]. The amplifier is a single input, single output cascode common source amplifier, operating in weak inversion with 10nA biasing current and 3.3V supply voltage. Weak inversion was chosen to achieve very low power consumption of the CIS. The photodiode size is 20μm × 20μm and the integration time can vary from milliseconds to microseconds depending on the photocurrent level. The switches were implemented as complementary switches in order to reduce charge injection, which can produce non-light related charge in the output [11]. The total power consumption of this in-pixel CTIA with CDS topology is 34.84 nW compared to the power consumption of 101.24nW of the topology in Fig. 2(a). However, the latter has one phase less than the in-pixel CTIA with CDS and therefore the CIS can operate faster, which in the targeted application is not relevant.

IV. Conclusion

In this paper two different approaches to implement CDS technique in CTIA architectures are proposed. The first approach is based on new alternative switching configuration, which enables the use of CTIA with CDS using a column parallel switch capacitor difference circuit without the use of any memory cell. As a result the reset noise is suppressed compared with conventional topologies. The second approach is based on the proposed compact architecture that has an in-pixel CTIA combined with CDS technique. It exploits the advantages of CDS while it uses less than half the power consumption of conventional architectures. This is because it uses only one amplifier for both CTIA and CDS. The CIS will be used in readout devices for LFIAs. In the targeted POC diagnostics application low power consumption, low-light operation and noise are crucial. Table I summarizes the performance of the CIS.

TABLE I. Performance Summary of CIS With In-Pixel CTIA And CDS

Parameter	***Value***
Technology	0.35μm CMOS
Number of pixels	8x64
Pixel fill factor	23%
Photodiode size	20x20μm^2
Power Supply	3.3V
Power Consumption (per pixel)	34.84nW
Integration Capacitance (C_{fb})	10 fF
Integration time	≈40μs-4ms

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